TSTE25 Power Electronics

Laboratory Compendium

Arvind Balachandran
Lars Eriksson
Tomas Jonsson

Vehicular Systems, Linköping University

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Contents

Overview

The TSTE25 Power Electronics course consists of three laboratory sessions and four hand-in assignments.

Examination Criteria for the Laboratory Sessions

For the laboratory sessions, the examination criteria require students to submit a written report through the submissions tab in Lisam. This report should contain the following:

- Preparatory tasks.
- Plots as specified in the hand-ins.
- Answers to the questions presented in the hand-ins.

Note that each hand-in should have its dedicated report. In other words, there should be a separate report for each of the four hand-ins.

Planned Laboratory activities

The planned activities for the laboratory sessions are detailed as follows:

Lab 1 Hand-in 1.

Lab 2 Hand-in 2 and Hand-in 3.

Lab 3 Hand-in 4.

Hand-in 1

Step-up and Step-down Converter

The lab contains assignments related to dc/dc step-down and step-up converters. The simulation will be done using MATLAB/SIMULINK (SIMSCAPE) where the setup will be constructed as part of the task. To define the circuit parameters some design calculations shall be performed. The theory related to DC/DC converters is found in [1, 2, 4].

1.1 Preperatory assignments

This section contains the preparatory assignments that must be completed before the lab.

1.1.1 Step-down (Buck) DC/DC converter

In this task, a step-down (Buck) DC/DC-converter (the schematic is shown in Figure 1.1) shall be designed for the supply of 12 V resistive load of 240 W, from a DC-source of 36 V. The switching frequency shall be 10 kHz.

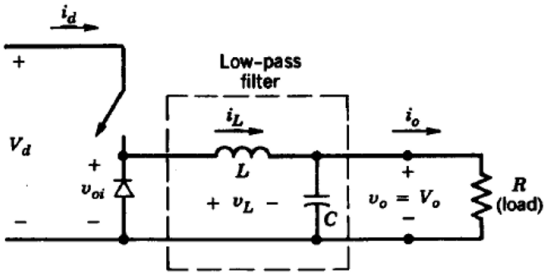

Figure 1.1: Step-down DC/DC converter.

Perform the following design steps:

1. Determine the duty cycle of the switch to obtain an output voltage of 12 V for 36 V voltage input.
2. Determine the load resistance and current corresponding to 240 W at 12 V.
3. Determine the minimum L to get a continuous inductor current at the rated load.

   Consider a current according to Figure 1.2 where the minimum ripple point is just touching zero.
4. Determine C to get a maximum peak-peak voltage ripple of 10% of the output voltage.
5. Determine the peak current in the inductor.

Note

Make a MATLAB script with the necessary formulas since this will be useful and speed up work during the Lab. In the lab conditions of the dc/dc converter.

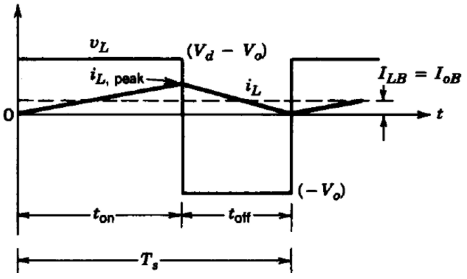

Figure 1.2: Conditions of a Buck converter at the boundary between continuous and discontinuous current.

1.1.2 Step-up (Boost) DC/DC converter

In this assignment, a step-up (Boost) DC/DC-converter (the schematic is shown in Figure 1.3) shall be designed and simulated for the supply of a 20 V resistive load of 50 W, from a DC-source of 5 V. The switching frequency shall be 10 kHz.

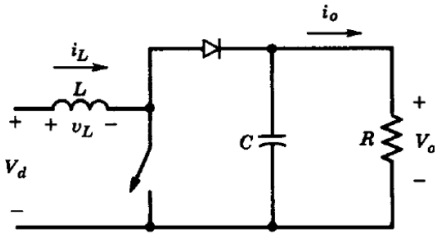

Figure 1.3: Step-up DC/DC converter.

Perform the following design steps:

1. Determine the duty cycle of the switch to obtain an output voltage of 20 V for 5 V voltage input.
2. Determine the load resistance and current corresponding to 50 W at 20 V.
3. Determine the minimum L to get a continuous inductor current at the rated load.

   Consider a current according to Figure 1.4 where the minimum ripple point is just touching zero.
4. Determine C to get a maximum peak-peak voltage ripple of 10% of the output voltage.
5. Determine the peak current in the inductor.

Getting Started

This lab will be performed through the simulation of converters using MATLAB, SIMULINK, SIMSCAPE. SIMSCAPE is an extension of SIMULINK, focused on modeling components and systems for power system applications. In addition to the guidance provided in MATLAB help for Simscape Power Systems, an introduction is found in [3].

The software is started by
Start, All Programs, Matlab, Matlab2021a in a Windows machine.
If you are using a Linux machine, then open the terminal, then type
`module add prog/matlab`,
then type
`matlab &`

It is recommended to set the "current folder" in MATLAB to your working directory, and a folder related to Lab 1.

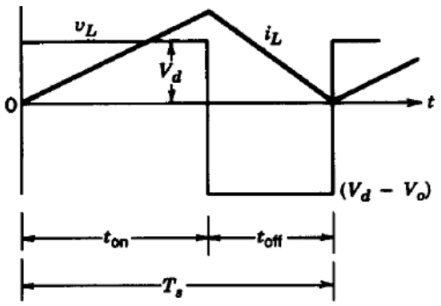

Figure 1.4: Conditions of a Boost converter at the boundary between continuous and discontinuous current.

1.2 Simulation: Step-down (Buck) DC/DC converter

In this assignment, a step-down DC/DC converter (the schematic is shown in Figure 1.5) shall be designed for the supply of a 12 V resistive load of 240 W from a DC source of 36 V. The switching frequency is 10 kHz. The inductance is determined in the preparation task (Section 1.1.1) corresponding to continuous operation at rated load for 36 V input. The output capacitance is also determined in the preparation task, corresponding to 10% output voltage ripple at rated load and 36 V input voltage.

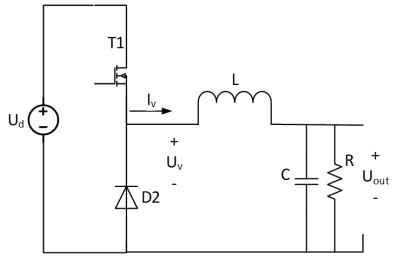

Figure 1.5: Step-down (buck) DC/DC converter.

Simulink setup

In this section, SIMULINK will be used to analyze the performance of the Buck converter. Electrical circuit blocks generally from the Simscape/Specialized Technology library shall be used. One does not have to follow the following procedure strictly, innovative solutions to model the step-down (buck) and step-up (boost) converters are highly appreciated.

Figure 1.6 shows the complete Simulink setup to allow the study of a step-down (buck) converter. The pulse width modulation (PWM) part is indicated by the blue area. Here the sawtooth carrier signal Vtri is created based on a standard block Sawtooth Generator which is found in Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Power Electronics/Pulse&Signal Generators. Since this block gives an output between -1 and $+1$, a conversion is done, i.e.,

$$\mathsf{Vtri} = 0.5 = (\mathsf{Sawtooth}_{\mathsf{out}} \cdot 0.5)\,.$$

The block Multiply-Add (HDL coder/HDL Operations) is used. The sawtooth carrier Vtri is then compared with the Constant D, which defines the duty cycle, to generate the gate pulse for the buck converter switch (T_1 in the schematic shown in Figure 1.5). The comparator is a block, Relational operator in Simulink/Logic and bit operations. A Data Type Conversion in Simulink/Signal Attributes of the gate pulse is required to fit the input (g) for the Buck Converter block in Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Power Electronics.

The Buck Converter block has its high voltage DC-side connections indicated by (+) and (-). The DC Voltage Source (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Electrical Sources) is connected. The blocks can be mirrored by right-hand clicking the block and selecting rotate and flip. The low voltage (switched) output, corresponding to U_v in Figure 1.5, is marked by (1).

The inductor is represented by a Series RLC Branch (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Elements). Connect the (+) of the Series RLC Branch towards the Buck

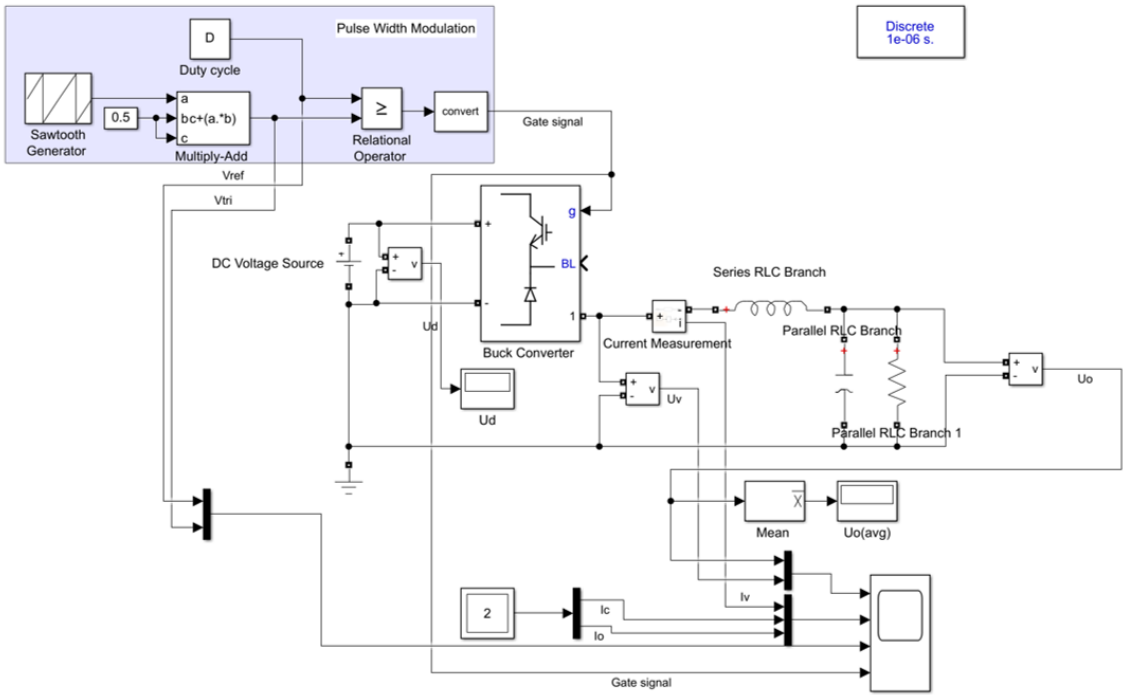

Figure 1.6: Step-down (buck) DC/DC converter setup in SIMULINK.

Converter block to get positive current flowing towards the load. The 12 V load resistor and filter capacitor are represented by two Parallel RLC Branch (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Elements). Connect the (+) input of the Parallel RLC Branch facing upwards (away from the ground) to get a positive branch voltage measurement. Ground (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Elements) is connected to the negative side, interconnecting both the high voltage and low voltage sides as shown in Figure 1.6.

A powergui block (Simscape/Power Systems/Specialized Technology/Fundamental Blocks) must be included to facilitate the solver. In the Model Configuration Parameters (shown as a cogwheel in SIMULINK), the solver options should be set to Fixed time step and ode4 (Runge-Kutta) solver is to be selected. Under additional parameters, the fixed time step shall be 1 μs (1e-6). The powergui Simulation type shall be set up for the Discrete-time step of 1 μs (1e-6).

Parameter definitions

The circuit and control parameters shall now be set up based on the results of the preparation task.

1. Set PWM frequency fsw to 10 kHz in the Sawtooth Generator block.
2. Setup the duty cycle of the MOSFET PWM switching.
3. Setup the Series RLC Branch inductance value L to get a continuous current at rated load at 36 V input voltage. The current shall just reach zero at the minimum spots.
   (a) Select the branch type as L.
   (b) Enter the calculated inductance value from the preparation task (in Section 1.1.1).
4. Setup the Parallel RLC Branch for the load resistance related to 240 W and the filter capacitor C to get a maximum peak-to-peak output voltage ripple of 10% from the preparation task (in Section 1.1.1).
   (a) Select the branch type as R or C.
   (b) Enter the calculated load resistance value as R.
   (c) Enter the calculated filter capacitance value as C.
   (d) Enable branch current measurement.

Measurement setup

To get a presentation of the circuit voltages and currents on a Scope some additional blocks are required:

1. Add a Voltage Measurement (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Measurements) to the DC voltage source.
2. Add a Voltage Measurement (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Measurements) to the output voltage across the parallel RLC branch.
3. Add a Current Measurement (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Measurements) in series with the inductor.
4. Add a Mux block to combine the PWM reference Vref and sawtooth signal Vtri on the same plot. Give names to the signals by clicking the lines before the Mux.
5. Add a Mux block to combine the voltages U_v and U_o on the same plot. Give names to the signals by clicking the lines before the Mux.
6. Add a Multimeter block (Simscape/Power Systems/Specialized Technology/Fundamental Blocks /Measurements) in order to pick up measurements from the two parallel RLC branches. On the left side available measurements are listed. Select measurements by pressing the arrow button as shown in Figure 1.7.

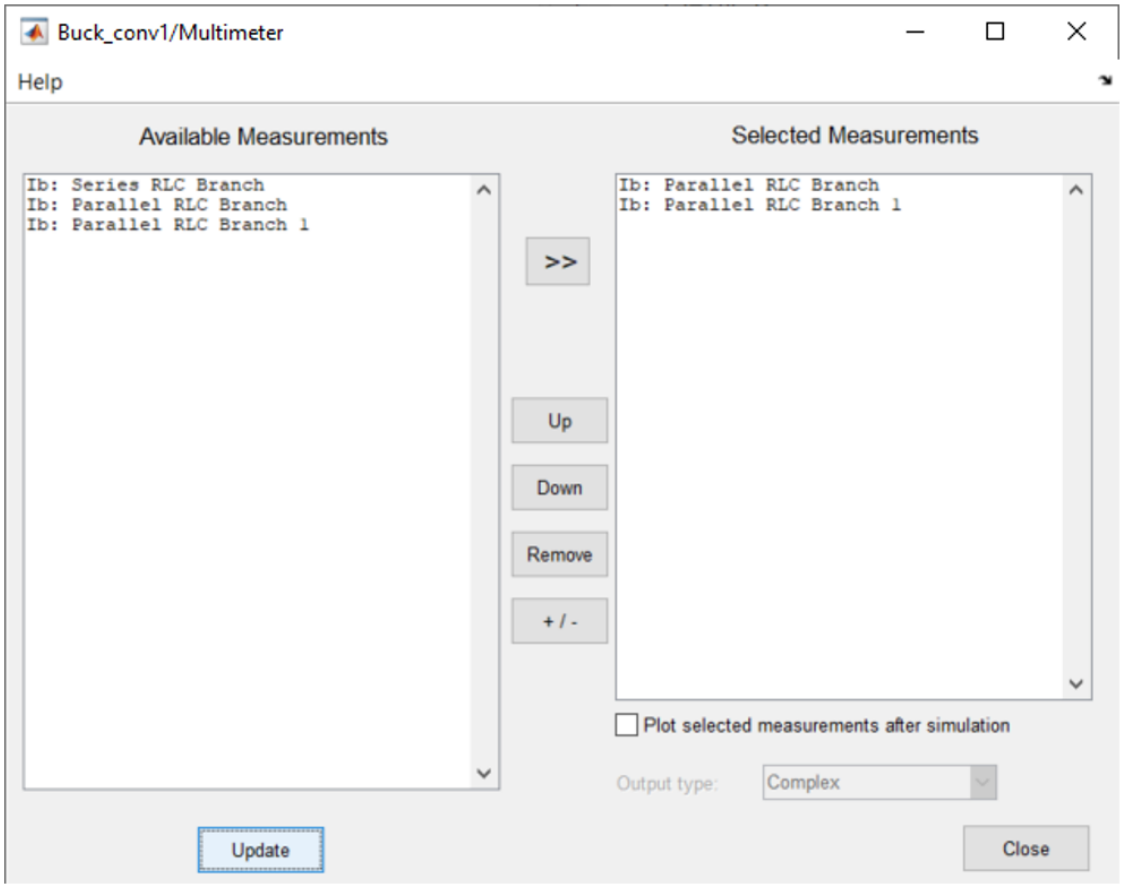

Figure 1.7: Multimeter block parameters

7. Add a Demux block to separate the branch current measurements from the Multimeter. Give names to the signals by clicking the lines. One is the capacitor current (I_c) and the other the load resistance output current (I_o).
8. Add a Scope for the 4 inputs (sub-plots)
   (a) Output voltages, before and after inductor. U_v and U_o, respectively.

(b) Inductor current (I_v), capacitor current (I_c) and output current (I_o).

(c) PWM Vref and Vtri.

(d) Gate pulses, G.

1.2.1 Case simulation results

Three cases shall now be studied, related to keeping 12 V constant output:

1. Input voltage $U_d = 36\,\text{V}$ (Same as preparation task).
2. Input voltage $U_d = 24\,\text{V}$ (Same as preparation task).
3. Input voltage $U_d = 36\,\text{V}$ Pout reduced to 120 W.

Set up the input voltage by editing the parameter of the DC Voltage Source. For each case, set the duty cycle (D) corresponding to 12 V average output voltage. Make simulation runs for the two cases for enough duration (0.01 s) to achieve stable steady-state conditions. The 2nd and 3rd cases use the same L and C as the 1st case, it is just the input voltage and duty cycle that is changed to maintain 12 V of the output.

The report should contain just one figure showing all three different cases with time plots of the following variables:

- Output voltage before the inductor, U_v.
- Output voltage after the inductor, U_o.
- Inductor current, I_L.
- Capacitor current, I_C.
- Load current (output current), I_o.
- Sawtooth (Vtri), and Duty cycle, D.
- Gase pulses, G.

A template for the required plots in the report is shown in Figure 1.8.

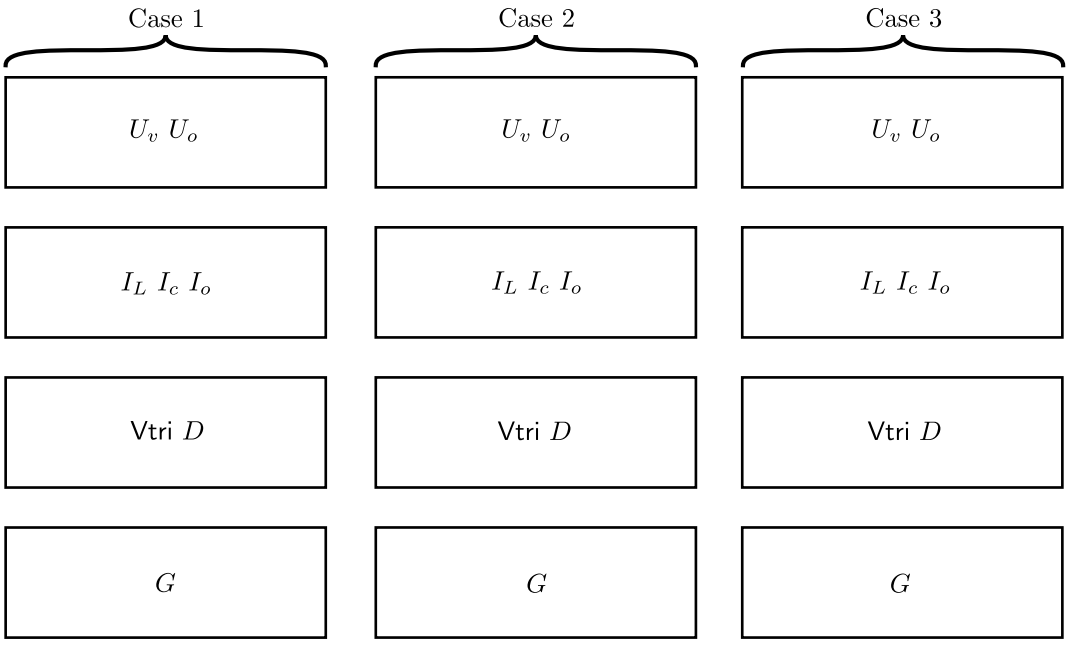

Figure 1.8: Example plot for hand-in 1.

Fill Table 1.1 with parameters and results for the three cases. For average and peak current I_v, only consider the steady state conditions. Neglect transients at the startup of the simulation. Answer the following questions:

Table 1.1: Buck converter results

		Case 1	Case 2	Case 3
U_d	V	36	24	36
U_{out}	V	12		
f_{sw}	kHz	10		
D	-			
P_{out}	W	240		120
R	Ω			
L	mH			
C	μF			
Average: I_L	A			
RMS: I_L	A			
Average: I_o	A			
RMS: I_o	A			
ΔU_o	V			

1. Compare and comment on the relation between gate pulses G, converter output voltage before (U_v) and after (U_o) the inductor, and PWM triangular (Vtri) and Duty cycle (D).
2. Is the inductor current continuous in all the cases?
3. Are the Average values of I_L and I_o similar? Why?
4. Are the RMS values of I_L and I_o similar? Why?
5. Plot the ratio of the output to input voltage (V_o/V_d) on the y-axis and the ratio of the output current to the peak inductor current ripple ($I_o/\Delta I_{L(pk.)}$) and using the SIMULINK model show the region where the converter operates in the discontinuous region.

Hints

Use the following MATLAB and SIMULINK commands for plotting the results.

`plot(X,Y)` plots vector Y versus vector X.

`subplot(m,n,p)` divides the current figure into an m-by-n grid and creates axes in the position specified by `p`. MATLAB numbers subplot positions by row. The first subplot is the first column of the first row, the second subplot is the second column of the first row, and so on. If axes exist in the specified position, then this command makes the axes the current axes.

`tiledlayout` definition is imilar to subplot.

To Workspace block logs the data connected to its input port to the workspace from a SIMULINK model.

1.3 Simulation: Step-up (Boost) DC/DC converter

In this assignment, a step-up DC/DC converter shall be designed and simulated for the supply of a 20 V resistive load of 50 W from a DC source of 5 V. The switching frequency is 10 kHz. The inductance is determined in the preparation task corresponding to continuous operation at rated load for 5 V input. The output capacitance is also determined in the preparation task, corresponding to 10% output voltage ripple at rated load and 5 V input voltage.

Simulink setup

Remember to make a copy of the buck model in order to keep this for future work. Figure 1.9 shows the complete Simulink setup to allow the study of a step-down (buck) converter The model for the boost converter can be built by modifying the buck converter setup since most components are the same, however the parameters may be different. The difference is the converter block which here is named Boost Converter in the library folder (Simscape/Power Systems/Specialized Technology/Fundamental Blocks/Power Electronics).

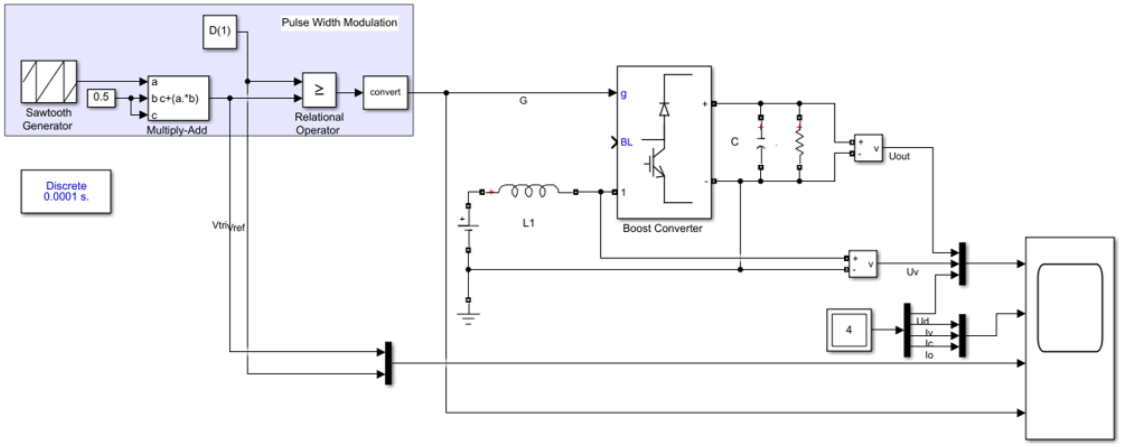

Figure 1.9: Step-up (boost) DC/DC converter setup in SIMULINK.

1.3.1 Case simulation results

Two cases shall now be studied, related to keeping 20 V constant output:

1. Input voltage $U_d = 5\,\text{V}$ and output power, $P_o = 50\,\text{W}$.
2. Input voltage $U_d = 10\,\text{V}$, and output power, $P_o = 50\,\text{W}$.
3. Input voltage $U_d = 10\,\text{V}$, and output power, $P_o = 200\,\text{W}$.

Setup the input voltage by editing the parameter of the DC Voltage Source. For each case, set the duty cycle D corresponding to 20 V average output voltage. Make simulation runs for the three cases for enough duration (0.01 s) to achieve stable steady state conditions. The 2nd and 3rd cases use the same L and C as the 1st case, it is just the input voltage and duty cycle that is changed to maintain 20 V of the output.

The report should contain just one figure showing all three different cases with time plots of the following variables:

- Output voltage before the inductor, U_v.
- Output voltage after the inductor, U_o.
- Inductor current, I_L.
- Capacitor current, I_C.
- Load current (output current), I_o.
- Sawtooth (Vtri), and Duty cycle, D.
- Gase pulses, G.

Fill Table 1.2 with parameters and results for the three cases. For average and peak current I_v, only consider the steady state conditions. Neglect transients at the startup of the simulation. Answer the following questions:

1. Compare and comment on the relation between gate pulses G, converter voltage after inductor (U_v) and output voltage (U_o), and PWM triangular (Vtri) and Duty cycle (D).
2. Is the inductor current continuous in all the cases?
3. Are the Average values of I_L and I_o identical? Why?
4. Are the RMS and average values of I_o identical? Why?
5. Are the RMS and average values of I_L identical? Why?
6. Plot the ratio of the output to input voltage (V_o/V_d) on the y-axis and the ratio of the input current to the peak inductor current ripple ($I_{in}/\Delta I_{L(pk.)}$) and using the SIMULINK model show the region where the converter operates in the discontinuous region.

Table 1.2: Boost converter results

		Case 1	Case 2
U_d	V	5	10
U_{out}	V	20	
f_{sw}	kHz	10	
D	-		
P_{out}	W	50	
R	Ω		
L	mH		
C	μF		
Average: I_L	A		
RMS: I_L	A		
Average: I_o	A		
RMS: I_o	A		
ΔU_o	V		

Hand-in 2

Gate Drive Analysis of Power MOSFETs

This chapter presents the SIMULINK model-based analysis of a MOSFET gate drive unit, and also the preparation tasks to be addressed before the lab.

2.1 Preperations: MOSFET switching performance calculations

In this section, the gate control of the MOSFETs in a full- or half-bridge circuit will be analyzed. For simplicity, the focus will be on the half-bridge, which is a building block in the full-bridge circuit.

> Note that the datasheets and other supporting documents are available in the Laboratory section on the course webpage https://isy.gitlab-pages.liu.se/fs/courses/TSTE25/.

The PWM gate pulses (G_1 and G_2) are converted into the final gate-source voltage for the two MOSFETs through the circuit shown in Figure 2.1. The purpose of the gate drive is to drive the MOSFETs (Q_1 and Q_2) with a gate current for the proper turn-on and turn-off. The MOSFETs are driven by the corresponding gate control voltages (V_{gg1} and V_{gg2}), switching between 15 V at turn-on and 0 V at turn-off, as defined by the inputs (G_1 and G_2) from the PWM control.

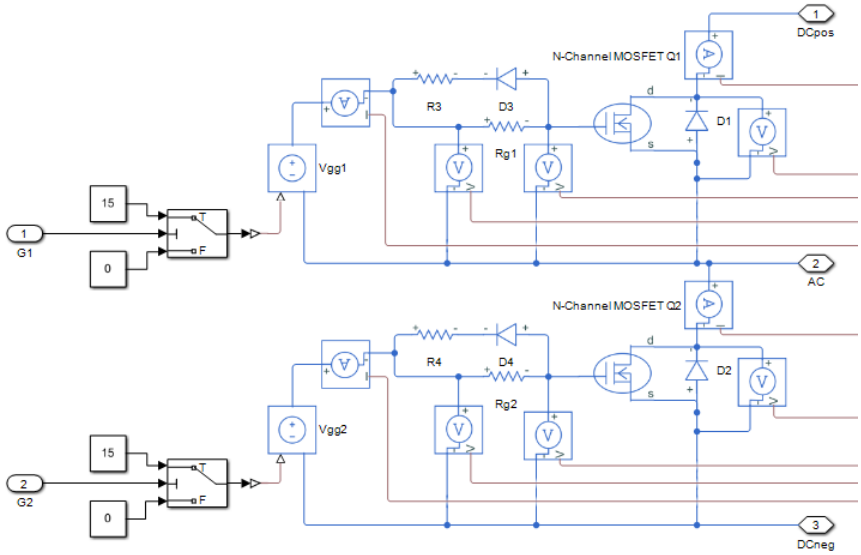

Figure 2.1: Gate drive simulation setup for the half-bridge.

The gate resistances during turn-on are defined by R_{g1} and R_{g2} and are typically between 150 Ω and 1 kΩ. The gate resistances are defined separately for turn-off, using diodes D_3 and D_4 which puts the resistors R_3 and R_4 in parallel to R_{g1} and R_{g2}. With $R_3 = R_4 = 10\,\Omega$, which is much smaller than R_{g1} and R_{g2}, the resistance of R_3 and R_4 will dominate during turn-off.

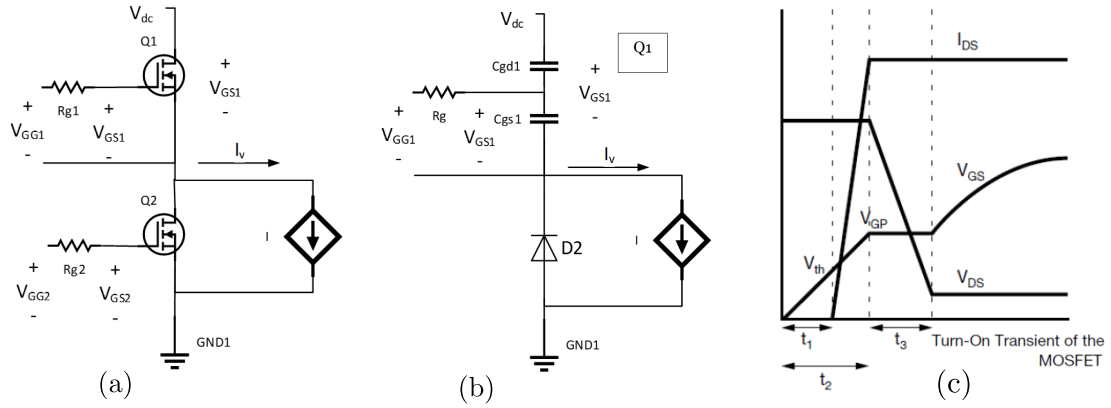

Figure 2.2: Half-bridge inverter circuit. (a) equivalent circuit diagram of the half-bridge inverter, (b) equivalent circuit when MOSFET Q_1 is turned on in the half-bridge inverter, and (c) simplified turn-on transient of the MOSFET.

A simplified equivalent circuit diagram is shown in Figures 2.2(a) and (b). Related to the design presented for the MOSFET-based half-bridge inverter, perform the following calculations of the turn-on switching dynamics of MOSFET Q_1. At the Q1 turn-on instant, transistor Q_2 has just been turned off. Since the output current is flowing out from the half-bridge, the diode D_2 associated with transistor Q_2 will conduct.

Consider the idealized turn-on waveforms as shown in Figure 2.2(c) based on the description in the application note [5]. Consider the following definitions of device capacitances, where values are found in the MOSFET datasheet [6].

1. $C_{iss} = C_{gs} + C_{gd}$, ($C_{ds}$ shorted).
2. $C_{rss} = C_{gd}$,
3. $C_{oss} = C_{ds} + C_{gd}$.

Consider $V_{gg} = 15\,\text{V}$ at turn-on and $V_{gg} = 0\,\text{V}$ at turn-off. Using the MOSFET datasheet in [6], fill Table 2.1.

Table 2.1: MOSFET capacitances.

C_{iss}	pF		at $V_{ds} = 25\,\text{V}$
C_{rss}	pF		at $V_{ds} = 25\,\text{V}$
C_{rss}	pF		at $V_{ds} = 0\,\text{V}$

Complete the following assignments and fill Table 2.2.

2.1.1 Turn-on delay

In this subsection, the MOSFET turn-on delay is calculated. The turn-on delay is defined as the time taken until the MOSFET drain current in the MOSFET becomes positive (t_1 in Figure 2.2(c)). This is also the time taken for the MOSFET gate-source voltage V_{gs} to reach the threshold voltage V_{th}. V_{th} can be obtained from the table called "SPECIFICATIONS/Dynamic" in the MOSFET datasheet [6]. The turn-on delay is given in [5] as

$$t_1 = -R_{g1} C_{iss} \ln\left(1 - \frac{V_{th}}{V_{gg}}\right). \tag{2.1}$$

Use the MOSFET capacitance C_{iss} for $V_{ds} = 25\,\text{V}$ as given by a graph in "Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage" in the MOSFET datasheet [6].

Complete the following tasks:

1. Calculate t_1 considering two values of R_{g1}, i.e, $150\,\Omega$ and $1\,\text{k}\Omega$ and fill Table 2.2.
2. Draw the equivalent circuit during the turn-on delay and use this equivalent circuit to derive the expression (2.1).

2.1.2 Drain current rise time

In this subsection, the rise time of the MOSFET drain current is calculated. In Figure 2.2(c), the rise time is $t_2 - t_1$, and t_2 is the time delay until $V_{gs} = V_{gp}$. Assume the plateau voltage $V_{gp} = 5\,\text{V}$ t_2 is calculated as [5]

$$t_2 = -R_{g1} C_{iss} \ln\left(1 - \frac{V_{gp}}{V_{gg}}\right). \tag{2.2}$$

The drain current rise time t_{ri} is

$$t_{ri} = t_2 - t_1. \tag{2.3}$$

Complete the following tasks:

1. Calculate t_{ri} considering two values of R_{g1}, i.e, $150\,\Omega$ and $1\,\text{k}\Omega$ and fill Table 2.2.
2. Draw the equivalent circuit during the turn-on delay and use this equivalent circuit to derive the expression (2.2).

2.1.3 Rate of change of drain-source voltage

In this subsection, the rate of change of MOSFET drain-source voltage (dV_{ds}/dt) is calculated. dV_{ds}/dt depends on the MOSFET capacitance C_{rss} which is a function of V_{ds} as shown in "Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage" in the MOSFET datasheet [6]. From the datasheet, C_{rss} at $V_{ds} = 25\,\text{V}$ and $V_{ds} = 1\,\text{V}$ were determined (in Table 2.1) and during turn-on, the MOSFET V_{ds} changes from 25 V to 1 V. Therefore, the average capacitance of C_{rss} based on 25 V and 1 V is used to determine dV_{ds}/dt. During the transition of V_{ds} (or dV_{ds}/dt), the gate-source voltage (V_{gs}) is equal to the plateau voltage (V_{gp}, assumed to be 5 V), and the relation between gate current (i_g), dV_{ds}/dt, and gate-drain capacitance (C_{rss}) is

$$i_g = C_{rss}\frac{dV_{ds}}{dt}, \quad \text{where } i_g = \frac{V_{gg} - V_{gp}}{R_{g1}}. \tag{2.4}$$

Complete the following tasks:

1. Calculate dV_{ds}/dt considering two values of R_{g1}, i.e, $150\,\Omega$ and $1\,\text{k}\Omega$ and fill Table 2.2.
2. Draw the equivalent circuit during the turn-on delay and use this equivalent circuit to derive the expression (2.4).

2.1.4 Gate-source voltage due to complimentary MOSFET turn-off

In this subsection, resulting V_{gs} for a MOSFET in off-state (say Q_2 in Figure 2.2(a)) when the opposite switch (Q_1) is turning on. Assume the V_{ds} of the MOSFET (Q_2) to be exposed by a positive dV_{ds}/dt, as calculated in Subsection 2.1.3. Furthermore, consider $V_{gg} = 0\,\text{V}$, since Q_2 is intended to be turned-off. However, as mentioned previously, during turn-off, the diodes D_3 and D_4 (see Figure 2.1) are in conduction, thus the forward voltage drop of the diode has to be considered (datasheet of the diode [7]). As a result, (2.4) new becomes

$$V_{gs} = V_{d4} + i_g R_4, \quad \text{where } i_g = C_{rss}\frac{dV_{ds}}{dt}. \tag{2.5}$$

Complete the following tasks:

1. Calculate V_{gs} of Q_2 considering $R_4 = 10\,\Omega$ and fill Table 2.2.
2. Draw the equivalent circuit during the turn-on delay and use this equivalent circuit to derive the expression (2.5).

2.2 Gate drive simulation tasks

The Simulink model Lab_2.slx can be found in the handin2 folder. The files are available from the course webpage https://isy.gitlab-pages.liu.se/fs/courses/TSTE25/.

Make measurements and analysis from SIMULINK as described below and present the graphs and analysis results in a lab report document. These measurements are related to the MOSFET switching waveform in Figure 2.2(c) and the corresponding performance calculations in Section 2.1.

Consider the following for before moving to the simulation tasks:

1. Two simulation runs will be made for different values of R_{g1} and R_{g2}, i.e., $R_{g1} = R_{g2} = 150\,\Omega$ and $R_{g1} = R_{g2} = 1\,k\Omega$.

2. Save the plots for each simulation and zoom to show the turn-on waveform according to Figure 2.2(c).

   - The Scope window can be copied in SIMULINK using File, Copy-to-Clipboard and then pasted into a document for the Lab report.
   - It is also possible to log the data to the workspace from the Scope by clicking on the cogwheel in the top-left corner of the Scope window, then go to Logging tab and tick the check box that has the text, Log data to workspace. Note that you have to re-run the simulation for the data to be saved onto the workspace.

   A file to plot the results is provided. Running the file Lab2_plots.m generates two matlab figure windows: Figure 10 shows the turn-on and turn-off transients for the switch Q_1 and Figure 11 for the switch Q_2. Furthermore, two .bmp files are created which can be used in the report.

3. Measurements in the Scope window can be done by selecting Cursor Measurements on the toolbar menu (rightmost icon, i.e., the icon with the ruler). Upon clicking (single click), two measurement lines will appear (1) and (2) which can be moved to the points defined below for measuring time durations. Remember to turn off the zoom first.

   On the right-hand side of the scope window, a drop-down table can be found with the list of signals selected for measurement. The value at times (1) and (2), as well as time difference (ΔT), amplitude difference (ΔY), frequency ($1/\Delta$T) and derivative (ΔY/ΔT), are shown.

The simulation tasks are as follows:

1. Set the value of R_{g1} and R_{g2}, i.e., $R_{g1} = R_{g2} = 150\,\Omega$ will be for case 1 and $R_{g1} = R_{g2} = 1\,k\Omega$ for case 2.

2. Measure the time delays t_1, t_2, and t_3 for the MOSFET Q_1 according to Figure 2.2(c). Select a switching event giving the highest MOSFET current level, i.e., the MOSFET is conducting current after the gate turn-on, **not** the diode (D_1). Here are some tips for measuring the variables in Table 2.2:

   (a) The starting point for t_1 and t_2 is the start of the V_{gs} rise.

   (b) The end of t_2 is the point where the current first reaches the flat current level, excluding over-shoots. The current rise time is

   $$t_{ri} = t_2 - t_1.$$

   (c) Measure the flat current level after the over-shoot, which is I_q for Q_1.

   (d) Measure V_{th}, i.e., the threshold level. This is the value of V_{gs} where the MOSET drain current starts to rise from 0 A.

   (e) Measure V_{gs} during the Miller plateau, this is the plateau voltage (V_{gp}).

3. Measure dV_{ds}/dt during the Miller plateau for Q_1 turn-on, for both MOSFETs Q_1 and Q_2, which is off. Measure for the maximum dV_{ds}/dt (steepest initial part) and average dV_{ds}/dt during the turn-on of Q_1. Fill in in Table 2.2.

4. Measure the V_{gs} of the MOSFET Q_2, which is off during the Q_1 turn-on interval. However, Q_2, increases momentarily during dV_{ds}/dt of Q_1 in the turn-on transient. Record the maximum V_{gs} reached for Q_2 and full in Table 2.2. Check how close to the V_{th} of MOSFET Q_2. Q_2 could turn on if the threshold level is passed.

5. Repeat the above steps with the other value of R_{g1} and R_{g2}.

Table 2.2: Simulated and analytical results of gate drive analysis for power MOSFET.

		Calculated Section 2.1		Simulated SIMULINK		
R_g	Ω	1000	150	1000	150	
V_{th} for Q_1	V					Gate threshold voltage
V_{gp} for Q_1	V					Miller gate voltage plateau
I_q for Q_1	A	-	-			MOSFET on-state current, i.e., the level after complete turn-on
t_1 for Q_1	ns					Time taken for I_q to start rising from 0 A
t_{ri} for Q_1	ns					I_q rise time
t_3 mean for Q_1	ns	-	-			Duration of Miller plateau
dV_{ds}/dt mean for Q_1	V/μs					Average dV/dt during Miller plateau
dV_{ds}/dt max for Q_1	V/μs	-	-			maximum dV/dt during initial steep part
dV_{ds}/dt max for Q_2	V/μs	-	-			maximum dV/dt during initial steep part
V_{gs}^{max} for Q_2	V					Disturbance of the off-state MOSFET

2.3 Excercises

A file to plot the results is provided. Running the file Lab2_plots.m generates two MATLAB figure windows: Figure 10 shows the turn-on and turn-off transients for the switch Q_1 and Figure 11 for the switch Q_2. Furthermore, two .bmp files are created which can be used in the report. In the figures (Figure 10 and Figure 11), the time $t = 0\,\text{s}$ indicates the instance of the transient, i.e., the instant at which the switch a positive or negative gate pulse is sent to either Q_1 or Q_2. The figures show the gate pulse (V_{gg}), gate-to-source voltage (V_{gs}), gate current (I_g), the drain current (I_q), and the drain-to-source voltage (V_{ds}) as a function of time for the two cases (Case 1: the external gate r4esistance, $R_g = 150\,\Omega$ and Case 2: $R_g = 1000\,\Omega$) for both the switches Q_1 and Q_2. Note that V_{gg} for both the cases for a switch (either Q_1 or Q_2) are identical. Using Figure 10 and Figure 11, answer the following questions:

1. Observing V_{gs}, I_g, I_q, V_{ds}, comment on the different between the two cases. For example: "I_g has a higher peak in case 2 than in case 2 because of some reason. I_q in case 1 has a longer rise time than case 2 because of some other or same reason" (Note: the comment above may not be correct as this is an illustration of an expected answer to the question).

2. Although the turn-on transients for the switch Q_1 are different for the two cases, the turn-off transients are similar, Why?

3. Observing the transients for the switch Q_2, at $t < 0$, i.e., when the gate pulse is zero, why is there a current through the switch, $I_{q(2)} \neq 0$?

4. Observing the transients for the switch Q_2, why is there no plateau for $V_{gs(2)}$?

5. Which of the two cases has higher switching losses? Is there a consequence with the case that has the lower switching loss?

Note: The report should include the preparation task, the answers to the questions above including the two figures, and the Table 2.2.

Hand-in 3

Simulation and Measurements of PWM Full-Bridge Inverter

. This chapter presents the study of the basic operation of a full-bridge inverter using pulse width modulation (PWM).

3.1 Preperations: Full-bridge inverter PWM

Consider a DC-voltage input (U_d) of 15 V to the full-bridge inverter and calculate the fundamental (i.e., 50 Hz) RMS output voltage before the filer inductor for the following cases:

1. $m_a = 0.9,\ U_{ab} =$ ____ V.
2. $m_a = 0.5,\ U_{ab} =$ ____ V.

Use the following relation to determine U_{ab},

$$U_{ab} = m_a U_d \,[\mathrm{V}] \tag{3.1}$$

Study the full-bridge inverter manual in [8], to be able to physically identify the corresponding location on the inverter board of the following components and sub-circuits:

1. DC input terminals
2. MOSFETs T_1-T_4
3. AC-output terminals
4. Load resistor
5. Gate control input connector
6. 5 V supply terminal
7. Gate driver supply terminal
8. Gate driver T_1-T_4
9. Voltage measurement configuration
10. Measurement output connector

3.2 Full-bridge inverter PWM simulation

This section presents the simulation of the full-bridge inverter in SIMULINK.

All the necessary files required for the hand-in are present on the course webpage under the Laboratory section.
Place the downloaded files into the local C: drive on the Lab computer,

for example in `C:\users\<<LIUID>>\TSTE25\Lab3`

Note:Please do not change the folder structure!

The contents of the handin3.zip (downloaded from the course webpage) are as follows:

FB_ctrl_Adue_meas.vi LabVIEW measurement interface file used for visualizing the measurements.

Simulink/Libraries A folder containing the source code for programming the Arduino using Simulink.

Simulink/FB_ctrl_Adue/FB_ctrl_Adue.slx The main Simulink file used in handin 3.

Simulink/FB_ctrl_Adue/FB_ctrl_Adue_sim.slx The main Simulink file for simulation of FB-inverter used in handin 3. This file can be used if the Matlab has no hardware support packages installed.

Simulink/FB_ctrl_Adue/FB_ctrl_Adue_init.m The initialization matlab-script.

Simulink/FB_ctrl_Adue/plots_handin3.m A Matlab script that can be used to plot the recorded measurements.

Simulink/FB_ctrl_Adue/mesh A directory used for storing the recorded measurement data.

Simulink/FB_ctrl_Adue/plots A directory with the plots used for the report.

Simulink Control Setup

The Simulink model FB_ctrl_Adue.slx can be found on the course webpage and once opened, it should look like as shown in Figure 3.1, which contains three main parts, they are:

Command Interface The left part of the model with slider switches and displays,

FB inverter control block The center subsystem block that contains the instructions for the control of FB-inverter, i.e., PWM duty cycle generation, etc. In this block, there is a switch that enables the transition between simulation and hardware monitoring and tuning (programming and monitoring signals using an Arduino due).

Signal measurement interface The right part of the model has several scope windows to visualize simulation data.

The Simulink model is when using the Arduino operated in External mode, which implies that a communication link is set up between the Arduino due target and the Simulink program to acquire data for presentation in Simulink. This practically implies that the command blocks and measurement presentation are executed on the host computer while the actual controller is executed on the Arduino due target.

In this section, a simulation is performed, and the Simulink control setup can also be used in a fully simulated environment without the use of the Arduino due board or other hardware. A switch, shown in Figure 3.2, is used to change the signal interface to the inverter control functions

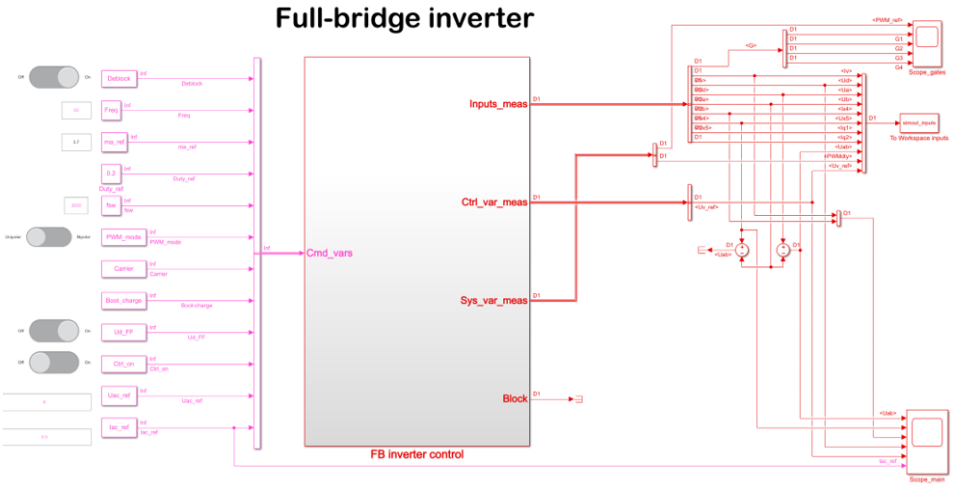

Figure 3.1: Simulink control interface for the FB-Inverter.

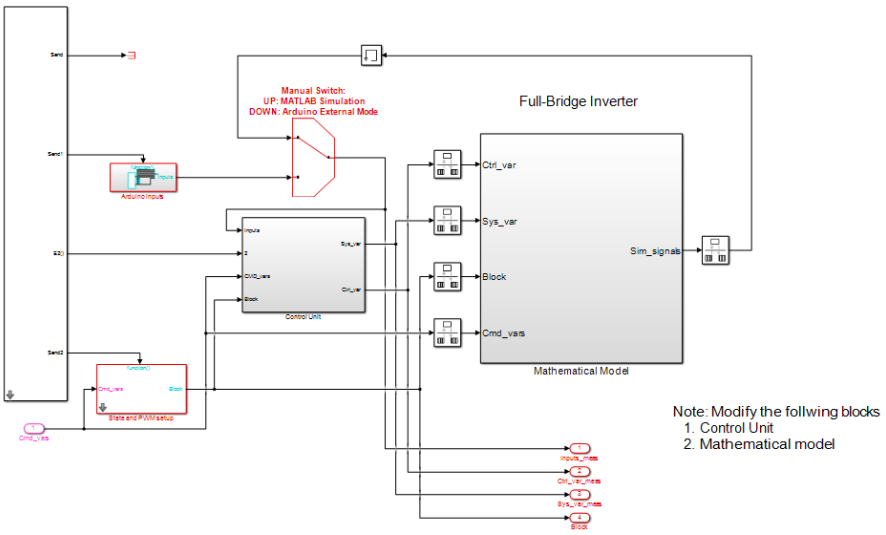

Figure 3.2: FB inverter control subsystem.

to be connected to either a mathematical model of the full-bridge inverter (simulation) or the Arduino due ADC (hardware). In this task, ensure that the switching is in the 'up' position.

A SIMULINK mathematical model of the full-bridge inverter located in the block Mathematical Model, subsystem shown in Figure 3.2, is used. Simulation Mode is activated through the Run (play icon) button on the Simulation tab.

Control Interface

The control parameters for the inverter can be changed through the SIMULINK command interface. Slider switches and edit boxes are used to change the status and parameters of the controller. The following commands are defined:

Deblock	Enable and disable of gate pulses	Hand-in 3 and 4
Freq	Fundamental PWM reference frequency for the AC-output voltage	Hand-in 3 and 4
. ma_ref	PWM modulation index (when Ud_FF is disabled)	Hand-in 3 and 4
Duty ref	Test mode setting of PWM duty cycle	Not used
fsw	PWM switching (carrier) frequency	Hand-in 3 and 4
PWM_mode	Changing between Unipolar PWM (0), Bipolar PWM (1)	Hand-in 4
Carrier	(=0) Left aligned (saw tooth wave), (=1) Center aligned (triangular wave)	Not used
Boot_charge	Enable initial turn-on of MOSFETs T2 and T4 at deblock, to charge the gate driver (boot-strap supply) for MOSFETs T1 and T3	Not used
Ud_FF	Enable feed-forward of measured U_d for calculation of PWM reference signal	Hand-in 4
Ctrl_on	Enable of feedback current control related to Iac_ref	Hand-in 4
Uac_ref	AC voltage magnitude (peak value) when Ud_FF is enabled	Hand-in 4
Iac_ref	AC current magnitude reference when Ctrl_on is enabled	Hand-in 4

FB inverter mathematical model

The full-bridge inverter is modeled using a Full-Bridge Converter block (shown in Figure 3.3), having the DC-inputs on the (+) and (-) terminals to the left and the AC-output terminals (1) and (2) to the right. A constant DC source is connected to the DC input and a resistive load in series with a filter inductor is connected to the AC output of the Full-Bridge Converter block.

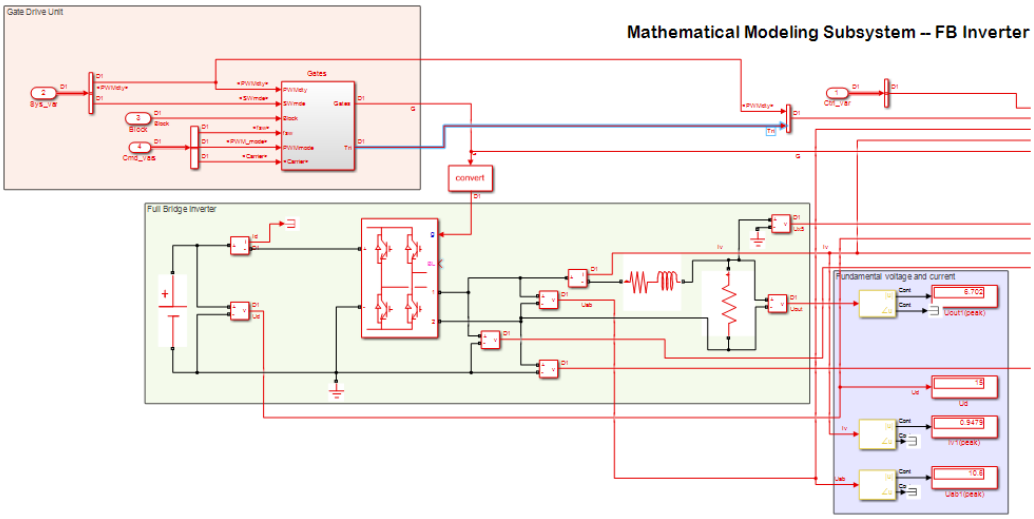

Figure 3.3: FB inverter mathematical model.

3.2.1 Full-bridge inverter simulation

Load the SIMULINK model FB_ctrl_Adue.slx. Ensure that the computer you are working on has the Arduino support packages installed, if not then download FB_ctrl_Adue_sim.slx file. To simulate the FB inverter, perform the following tasks:

1. Ensure that FB_ctrl_Adue/FB inverter control/Manual Switch is in the 'up' position (in MATLAB Simulation position). If you are using FB_ctrl_Adue_sim.slx file then you can ignore this step.

2. Enter the Mathematical Model clock (double-click the block to enter):

   (a) Confirm that a 5 mH inductor is connected between the full bridge and the load resistor.

   (b) Confirm a 15 V DC voltage supply is connected.

3. Start the simulation by clicking the green play button on the toolbar in the Simulation tab for Matlab 2020a or later.

4. Switch to the top level (FB_ctrl_Adue) and perform the following setup of the command interface:

   (a) Set fundamental PWM frequency (Freq) = 50 Hz.

   (b) Set PWM amplitude (ma_ref) = 0.9.

   (c) Set carrier frequency (fsw) = 950 Hz.

   (d) Select Unipolar PWM.

   (e) Set the Ud_FF = off.

   (f) Set the Ctrl_on = off.

   (g) Turn on the Deblock switch in SIMULINK.

5. Check and document the resulting peak fundamental output voltage before and after the inductor.

   U_{ab} is the voltage between terminals A and B before the inductor, and

   U_{out} is the voltage after the inductor across the load resistor.

   The fundamental frequency peak voltages are measured through the SIMULINK blocks Fourier, which are shown in the lower right area of Figure 3.3. The Fourier block gives the peak voltage of defined harmonic components as defined by its parameters.

6. Zoom in on one fundamental frequency period in Scope_main (located on the top hierarchical level of the model) to see the voltages U_{ab} and U_{out}. In addition, the gate pulses can be observed with the Scope inside the Mathematical model block.

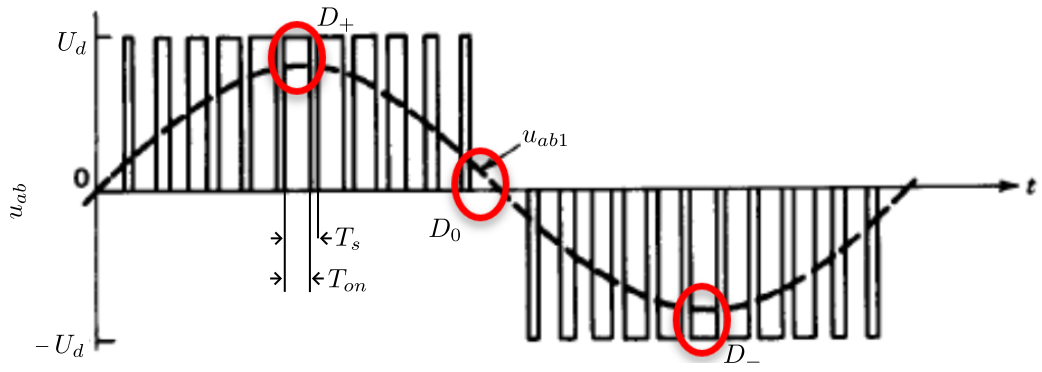

Figure 3.4: Typical unipolar output voltage.

Table 3.1: Unipolar PWM results from simulation.

Cases	m_a -	U_d V (pk.)	$\hat{U}_{ab1}$ V (pk.)	$\hat{U}_{out1}$ V (pk.)	T_s μs	D_+ -	D_0 -	D_- -
Sim-2a	0.9							
Sim-2b	0.5							

3.2.2 Full-bridge inverter simulation excercises

In this section, the simulation results of the full-bridge inverter are presented. The report should contain the answer to the following questions and fill in Table 3.1:

1. Determine the fundamental frequency peak voltages, U_{ab1} and U_{out1} related to the 50 Hz component and fill the fundamental voltages in Table 3.1.

2. Determine the effective switching cycle time T_s from the waveform, U_{ab}. Compare with the selected carrier frequency (fsw).

3. Determine the duty cycles, D, given by

$$D = \frac{T_{on}}{T_s}, \tag{3.2}$$

   where T_{on} is the duration of output voltage U_{ab} when $U_{ab} \neq 0$ over one switching cycle time T_s (i.e., $T_{on} < T_s$).

   Determine D at three different sections over a fundamental as shown in Figure 3.4.

4. Comment on the relation between ma and the duty cycle values.

3.3 Full-bridge inverter hardware

This section presents the hardware setup and the measurement procedure for the full-bridge inverter with unipolar PWM.

3.3.1 Full-bridge inverter hardware setup

This section presents the preparation and measurement setup required to perform measurements on the full-bridge hardware. Perform the following tasks:

1. Confirm the full-bridge inverter board is prepared as per the schematic shown in Figure 3.5.

2. Ensure the DC-voltage source is at +15 V and is connected to the full-bridge inverter but is switched off.

3. Ensure that the 5 mH inductor is connected between the yellow output connections IO1 and IO2.

4. Follow the schematic to set up the connections to measure the following:

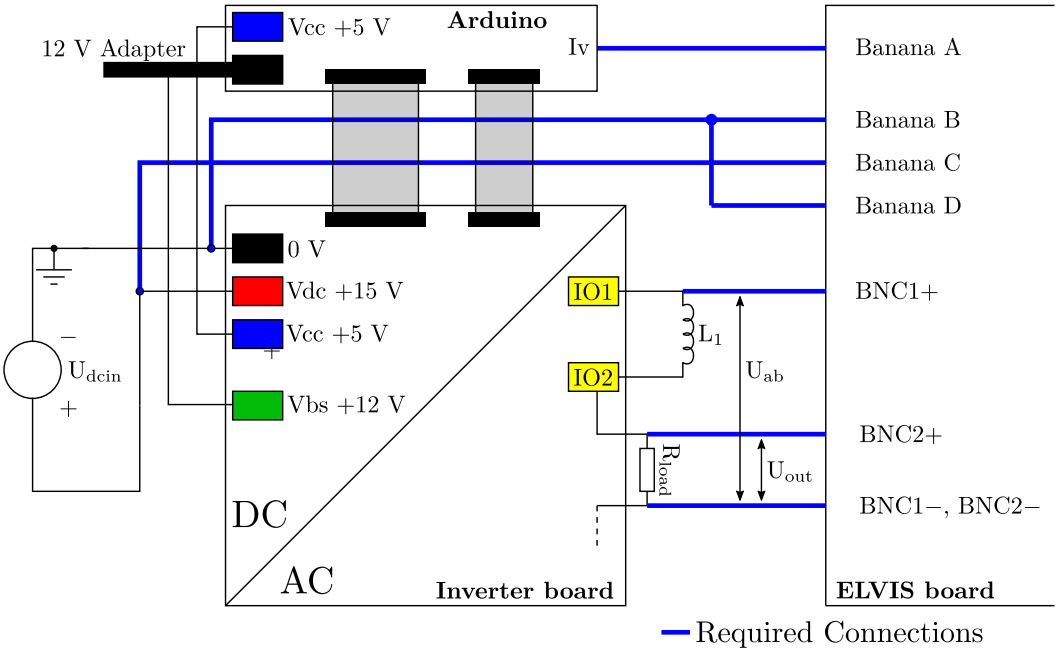

Figure 3.5: Full-bridge inverter hardware measurement schematic.

Load current, I_v: Connect ELVIS Banana A to the Iv terminal of the Arduino interface.
Connect ELVIS Banana B to the 0 V terminal of the full-bridge inverter board.

DC voltage, U_d: Connect ELVIS Banana C to the red, Vdc +15 V, terminal of the full-bridge inverter board.
Connect ELVIS Banana D to the 0 V terminal of the full-bridge inverter board.

Converter output voltage, U_{ab} Connect the ELVIS BNC1 measurement between yellow terminal IO1 (BNC1 positive) and the left terminal (board oriented as in Figure 3.6) of the power resistor on the inverter board (BNC1 negative).

Load voltage, U_{out} Connect the ELVIS BNC2 measurement across the power resistor. BNC2 positive to the right resistor terminal and the left terminal of the power resistor to BNC2 negative (board oriented as in Figure 3.6).

.

5. A special LabVIEW software interface is used for the Lab3 measurement with ELVIS. Copy the file: FB_ctrl_Adue_meas.vi to your local folder if not already there. Load the LabVIEW software by double-clicking the file. When the file is loaded the measurement interface will appear as shown in Figure 3.7.

   Before running the LabVIEW interface, the ELVIS device number must be set with the specific setup on your Lab computer. This is done by turning on the main power to the ELVIS board using the switch on the top-right corner of the board, and selecting the ELVIS device from the drop-down menu "DAQmx Device Name" on the LabVIEW front panel as shown in Figure 3.7. The program is started by clicking the circular arrow symbol (Run Continuously) in the Program execution control in Figure 3.7.

6. The Arduino due microcontroller is deployed based on a Matlab/Simulink controller setup.

   The Simulink files used in the lab can be downloaded from the course webpage. Put the downloaded files into the local C: drive on the Lab computer,

   for example in `C:\users\<<LIUID>>\TSTE25\Lab3`

   Remember to copy files to your LiU server student account after the lab. The files are organized in two folders: Libraries and FB_ctrl_Adue.
   Both these folders MUST be in the same directory!

   Start MATLAB 2021a, browse the MATLAB command window to set the current folder to your project folder FB_ctrl_Adue, and open the FB_ctrl_Adue.slx file.

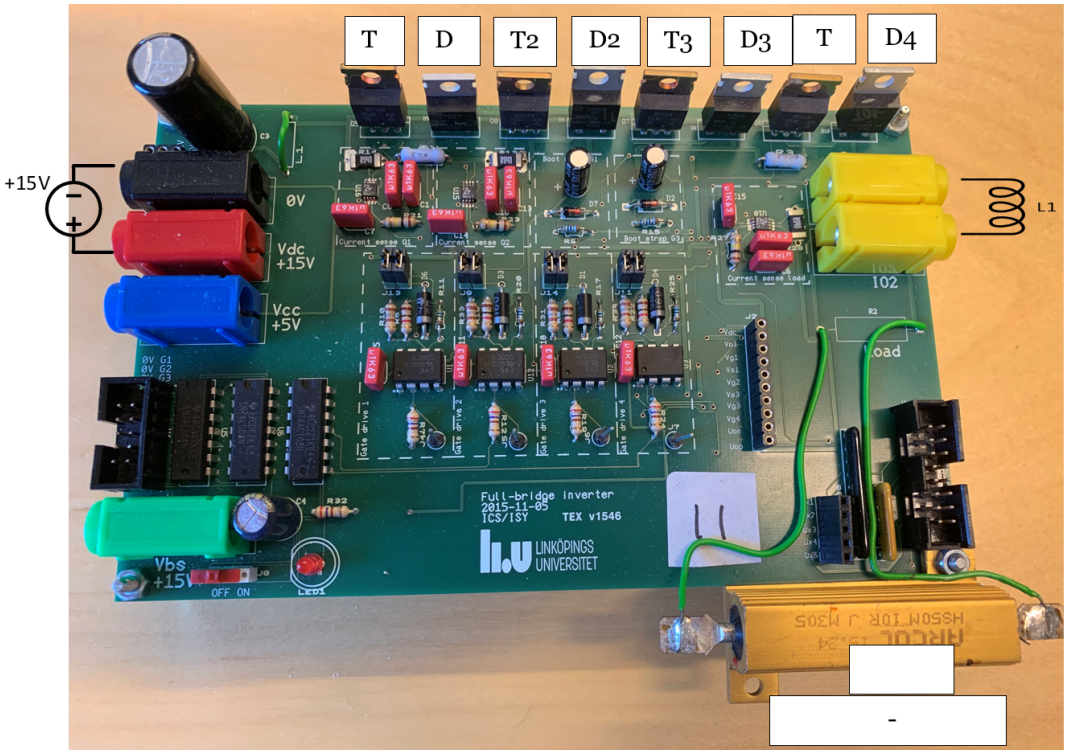

Figure 3.6: Full-bridge inverter hardware.

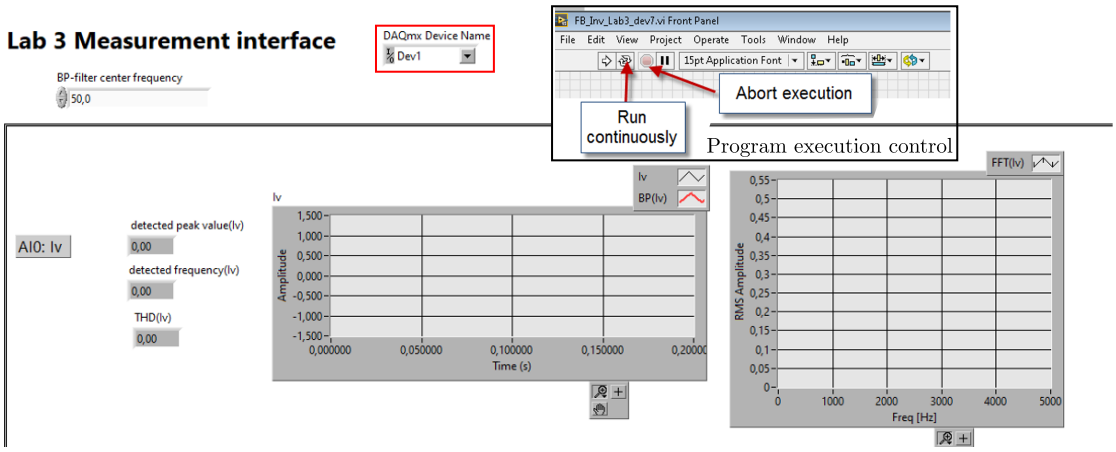

Figure 3.7: LabVIEW measurement interface for ELVIS.

7. Connect the USB cable to host-PC, thus enabling communication between Arduino due and MATLAB/SIMULINK.

3.3.2 Full-bridge inverter hardware measurements

In this section, the control of the output AC voltage magnitude using PWM is investigated.

1. Set Deblock switch on the full-bridge inverter board to the **'off'** position.
2. Ensure that FB_ctrl_v21_lab_3/FB inverter control/Manual Switch is in the 'down' position (i.e., Arduino External Mode).
3. Start the SIMULINK program FB_ctrl_v21_lab3.slx to run in external mode by clicking the green 'Monitor & Tune' button on the toolbar in the Hardware tab for Matlab 2020a or later.
4. Ensure that the Deblock switch in Simulink is **'off'**.

5. Perform the following steps to configure the command interface:
   (a) Set fundamental PWM frequency (Freq) = 50 Hz.
   (b) Set carrier frequency (fsw) = 950 Hz.
   (c) Select Unipolar PWM.
   (d) Set the Ud_FF to **'off'**.
   (e) Set the Ctrl_on to **'off'**.
6. Start the LabVIEW measurement interface for ELVIS.
7. Turn-on the 15 V DC voltage supply. Check that the current limit of the supply does not reduce the voltage. If the voltage reduces then increase the current limit.
8. Set Deblock switch on the board **'on'**.
9. Turn on the Deblock switch in Simulink.
10. BE AWARE THAT THE POWER RESISTOR WILL BE HOT!

Excercises

Measure the quantities, fill in Table 3.2, and perform the following activities:

1. Zoom in time graphs to a 20 ms view. Use a final 20 ms interval since the bandpass filtered signal has a settling interval. Save and present the time plot for the following variables:
   (a) Converter output voltage (U_{ab}),
   (b) Load voltage (U_{out}), and
   (c) Load current (I_v).

   How to save and use the measurement data for the report?

   (a) pause the Lab-VIEW software.
   (b) Right-click on a time-plot (for example, I_v) that is to be saved. Select export data to Excel and save the file in the Simulink/FB_ctrl_Adue/mesh directory with the name as the variable name followed by the case number with an underscore. For example,
   To save data for I_v, right-click on the I_v time-plot and go to export, export data to excel. If the measurements are performed for $m_a = 0.9$, then the file should be saved under the name Iv_Mesh-2a.xlsx in the directory Simulink/FB_ctrl_Adue/mesh.
   (c) Upon completion of recording the measurements for all the cases, run the Matlab script file plots_handin3.m, upon running a bmp file will appear in the directory Simulink/FB_ctrl_Adue/plots which can be added to the report.
2. Compare and comment U_{out}, U_{ab}, and I_v with the simulated results in Section 3.2.2.

Table 3.2: Unipolar PWM results from simulation.

Task	m_a -	$\hat{U}_d$ V (pk.)	$\hat{U}_{ab1}$ V (pk.)	$\hat{U}_{out1}$ V (pk.)	$\hat{I}_{v1}$ A (pk.)
Mesh-2a	0.9				
Mesh-2b	0.5				

Hand-in 4

Harmonic Analysis and Control of a Full-Bridge Inverter

. This chapter presents the harmonic analysis and control of a full-bridge inverter.

All the necessary files required for the hand-in are present on the course webpage under the Laboratory section.
Place the downloaded files into the local C: drive on the Lab computer,

for example in `C:\users\<<LIUID>>\TSTE25\Lab3`

Note:Please do not change the folder structure!

4.1 Unipolar PWM with variable fundamental frequency

In this section, the impact of the output voltage with changes in the fundamental frequency is studied.
Follow the hardware connections as shown in Sectiom 3.3.1. After completing the instructions in Sectiom 3.3.1, proceed with the following measurement procedure:

1. Make sure the deblock switch in SIMULINK is off.
2. Ensure that a 5 mH inductor is connected between the terminals (IO1 and IO2).
3. Ensure that FB_ctrl_Adue/FB inverter control/Manual Switch is in the 'down' position (i.e., Arduino External Mode).
4. Start the SIMULINK program FB_ctrl_Adue.slx to run in external mode by clicking the green 'Monitor & Tune' button on the toolbar in the Hardware tab for Matlab 2020a or later. (Do not stop the 'Monitor & Tune')
5. Set the command interface as follows:
   (a) Set PWM amplitude (ma_ref) to 0.9.
   (b) Set carrier frequency (fsw) to 950 Hz.
   (c) Select Unipolar PWM.
   (d) Vary the fundamental PWM frequency, Freq from 10 Hz to 200 Hz. Do not change the carrier frequency, fsw.
   (e) Set the Ud_FF to the off position.
   (f) Set the Ctrl_on to the off position.
6. Connect and turn-on the 15 V DC voltage suppply.
7. Turn-on the Deblock switch on the inverter board.
8. Turn-on the Deblock switch in SIMULINK.
9. Note the magnitude of the DC voltage and the output voltage at the fundamental frequency with respect to the given amplitude modulation index, m_a, in Table 4.1.

(a) Modify the Fundamental Frequency parameter in the LabVIEW interface to tune the bandpass filter to the detected frequency (i.e., change the BP-filter center frequency to match Freq).

Questions

Answer the questions presented, in this section, in the report.

1. How does the fundamental frequency amplitude of the voltage before and after the inductor, i.e., U_{ab} and U_{out}, change with the fundamental PWM frequency and why?
2. Observe the Uab spectrum (FFT window) in LabVIEW and explain how the change in fundamental frequency affects the sidebands clustered around 1800 Hz (2×950 Hz)?

Fill Table 4.1.

Table 4.1: Variable fundamental PWM frequency at switching frequency of 950 Hz.

Freq Hz	m_f -	U_{ab1} V	U_{out1} V
10			
50			
100			
200			

After recording the values, turn off the Deblock switch in Simulink and set the Deblock switch on the board to the off position. **Do not STOP the Monitor & Tune** in Simulink.

4.2 Unipolar PWM with variable switching frequency

In this section, the impact of the output voltage with changes in the switching frequency is investigated. The Measurement procedure is presented as follows:

1. If not done already then start the Simulink program FB_ctrl_Adue.slx to run in external mode by clicking the green 'Monitor & Tune' button on the toolbar in the Hardware tab for Matlab 2020a or later. (Do not stop the 'Monitor & Tune')
2. Set fundamental PWM frequency, Freq = 50 Hz.
3. Ensure that the 5 mH inductor to the yellow output connection (IO1 and IO2).
4. Set PWM amplitude, ma_ref = 0.9.
5. Perform experiments by variation of the PWM carrier frequency, fsw and check the range from 400 Hz to 100 kHz. Keep the fundamental PWM frequency (Freq) at 50 Hz and fill in Table 4.2.
6. After recording the values, turn off the Deblock switch in Simulink and set the Deblock switch on the board to the off position. **Do not STOP the Monitor & Tune** in Simulink.

Table 4.2: Variable PWM switching frequency with a fundamental frequency of 50 Hz.

f_sw Hz	m_f -	U_{ab1} V	U_{out1} V
500			
1 k			
10 k			
100 k			

Questions

Answer the questions presented, in this section, in the report.

1. How does the fundamental frequency amplitude of the voltage before and after the inductor, i.e., U_{ab} and U_{out}, change with the PWM switching frequency?

2. Observe the frequency spectrum of Uab and comment on how the side-bands are affected when fsw is changed.

4.3 DC-voltage feed-forward

In this section, a DC feed forward is implemented. To implement the DC-voltage feed-forward, a sound understanding of the SIMULINK model is necessary. It is worth mentioning that a SIMULINK model is a visual representation of mathematical equations.

We know that the fundamental output voltage magnitude from a full-bridge converter with PWM is defined by the following:

$$\hat{U}_{ab1} = m_a U_d, \tag{4.1}$$

where m_a is the modulation index, and U_d is the DC-link pole-to-pole voltage.

A new reference signal u^*_{ab1} is introduced, which is the desired output voltage, and unlike $m_a \in [-1, 1]$, $u^*_{ab1} \in [-\hat{U}_{ab1}, \hat{U}_{ab1}]$. From (4.1), it is clear that the output voltage is regulated by varying m_a (since U_d is usually constant), m_a is given by the relation

$$m_a = \frac{\hat{U}^*_{ab1}}{U_d} \tag{4.2}$$

In the SIMULINK model, in the command interface, the slider switch (when turned on) enables the feed-forward variable Ud_FF, i.e, Ud_FF = 1 when the slider switch is in the on position.

Simulink implementation

Stop the 'Monitor & Tune' in SIMULINK.

In the SIMULINK model in FB_ctrl_Adue/FB inverter control/Control Unit/AC-PWM block, among other things, the following code is implemented.

PWM_ref = 1 · Uv_ref,

---

where 1 is the dummy gain block with unity gain.

Before proceeding with the implementation of DC feed-forward, ensure that all the simulink bocks (especially the product block) are uncommented. The blocks that are commented out will be gray and have a '%' symbol in the bollow right/left corner of the block. To uncomment a block, right-click on the block and click on uncomment.

Implement the following pseudo-code in FB_ctrl_Adue/FB inverter control/Control Unit/AC-PWM subsystem block:

---

if Ud_FF > 0 **then**
  PWM_ref = $\frac{\text{Uv\_ref}}{\text{Ud}}$
else
  PWM_ref = Uv_ref
end if

After implementing the DC-voltage feed-forward in FB_ctrl_Adue/FB inverter control/Control Unit/AC-PWM, proceed with the following:

1. Start the SIMULINK program FB_ctrl_Adue.slx to run in external mode by clicking the green 'Monitor & Tune' button on the toolbar in the Hardware tab for Matlab 2020a or later. (Do not stop the 'Monitor & Tune')

2. Setup the command interface with the following:

   (a) Set fundamental PWM frequency, Freq = 50 Hz.

(b) Set carrier frequency, fsw = 950 Hz.

(c) Select Unipolar PWM.

(d) Set the Ud_FF = on, i.e., DC-voltage feed-forward is enabled.

(e) Set the Ctrl_on = off.

3. Set Deblock switch on the board to the on position.

4. Set the Deblock switch in SIMULINK to the on position.

5. Perform experiments by changing Uac_ref and DC-voltage supply (Ud) and fill up the Table 4.3.

6. After recording the values, turn off the Deblock switch in SIMULINK and set the Deblock switch on the board to the off position.

Table 4.3: DC voltage feed-forward.

Uac_ref V	Ud V	U_{ab1} V	U_{out1} V	I_{v1} A	m_a -
8	10				
8	15				
8	20				
12	15				
15	15				
20	15				

Questions

Answer the questions presented, in this section, in the report.

1. What happens to the ac-voltage output (U_{ab1} and U_{out1}) for a constant Uac_ref when Ud changes? Explain.

2. What happens to the ac-voltage output (U_{ab1} and U_{out1}) for a constant Ud when Uac_ref changes? Explain.

3. What happens to the ac-voltage output waveform (U_{ab1} and U_{out1}) when Uac_ref > Ud? Explain.

4.4 Full-bridge inverter current control

In this section, an output current controller is implemented. The current controller controls the output current of the inverter to a desired value. The controller to be implemented is a P controller with a voltage feed-forward. Contrary to Section 4.3, the current controller has a feedback loop.

Simulink implementation

Stop the 'Monitor & Tune' in SIMULINK.

The current controller is implemented in the SIMULINK block located in FB_ctrl_Adue/FB inverter control/Control Unit/AC-CTRL/Current control/P Controller with Feed-forward. In the block, implement the following pseudo-code:

---

error = Iv_ref − Iv_mes
Ctrl_op = $k_p \cdot$ error + U_load,

---

and the following psudo-code shall be implemented in FB_ctrl_Adue/FB inverter control/Control Unit/AC-CTRL/Current control

---

U_load = Ux5 − Ub,

---

where error is the error signal, Iv_ref and Iv_mes are the reference and the measured current, respectively. U_load voltage across the load resistor, Ctrl_op is the controller output, and k_p is the proportional gain.

$$k_p = \alpha_c \cdot L, \text{where } 2000 \leq \alpha_c \leq 10000.$$

In the model, the P-controller gain, k_p is defined in the FB_ctrl_Adue_init.m and can be changed using the monitor and tune phase using the MATLAB command window.

After implementing the current controller in FB_ctrl_Adue/FB inverter control/Control Unit/AC-CTRL/Current control/P Controller with Feed-forward, proceed with the following:

1. Connect the Ux5 pin in the Arduino to the BNC2 + (BNC2 positive pin).
2. Start the SIMULINK program FB_ctrl_Adue.slx to run in external mode by clicking the green 'Monitor & Tune' button on the toolbar in the Hardware tab for Matlab 2020a or later. (Do not stop the 'Monitor & Tune')
3. Setup the command interface with the following:
   (a) Set fundamental PWM frequency, Freq = 50 Hz.
   (b) Set carrier frequency, fsw = 500 Hz.
   (c) Select Unipolar PWM.
   (d) Set the Ud_FF = on, i.e., DC-voltage feed-forward is enabled.
   (e) Set the Ctrl_on = on i.e., current control is enabled.
   (f) The reference (or, desired) output peak current is given by the variable Iac_ref, change this variable according to Table 4.4.
4. Set Deblock switch on the board to the on position.
5. Set the Deblock switch in SIMULINK to the on position.
6. Perform experiments by changing Iac_ref fill up the Table 4.4.
7. After recording the values, turn off the Deblock switch in SIMULINK and set the Deblock switch on the board to the off position.

Table 4.4: Full-bridge inverter current control.

Ud	Iac_ref	U_{ab1}	U_{out1}	I_{v1}	m_a
V	A	V	V	A	-
15	0.2				
15	1.0				
20	1.0				

Questions

Answer the questions presented, in this section, in the report.

1. With a P-controller with a feed-forward, there always exists a steady-state error. To have a zero steady-state error, P-I controllers are often used. Can such a P-I controller be used to control the output current of the full-bridge inverter?

4.5 Converter Voltage Harmonics

In this section, the converter harmonics are analyzed, and the total harmonic distortion (THD) is calculated for both bipolar and unipolar modulation schemes in both simulation and hardware. The behavior of the unipolar and bipolar modulation schemes on the THD at different modulation indices (m_a) is investigated in this section.

4.5.1 Simulation

Complete the following steps and fill Table 4.5.

1. Ensure that FB_ctrl_Adue/FB inverter control/Manual Switch is in SIMULINK model is in the 'up' or 'Simulation' position. If you are using FB_ctrl_Adue_sim file then you can ignore this step.

2. Open the scope Scope_main, then go to Configuration Properties (represented as a cogwheel icon on the top-left corner) and go to the Logging tab. In the tab check the Log Data to workspace check box, enter the Variable name of your choice, and ensure that the Save format is Structure With Time.

3. Start the simulation by clicking the green play button on the toolbar in the Simulation tab for Matlab 2020a or later.

4. In the top level of the FB_ctrl_Adue or FB_ctrl_Adue_sim file, setup the command interface parameters as follows:

   (a) Set the fundamental PWM frequency (Freq) to 50 Hz.

   (b) Set PWM amplitude (ma_ref) to 0.9.

   (c) Set carrier frequency (fsw) to 950 Hz.

   (d) Select Unipolar/Bipolar PWM (depending on the task).

   Note: In the model, to switch between bipolar and unipolar modulation schemes, the converter must change from blocked state to de-blocked, i.e., turn-off and then turn-on the Deblock switch in SIMULINK.

   (e) Set the Ud_FF to off, i.e, DC-voltage feed forward disabled.

   (f) Set the Ctrl_on to off, i.e, no current control disabled.

5. Turn on the Deblock switch in SIMULINK.

6. Run the SIMULINK model for a while, check for PWM signals in the scopes, and after several fundamental cycles have passed, stop it.

7. Go to Mathematical Model subsystem and double click on the powergui block. Go to the Tools tab and click on the FFT Analysis button, now the FFT toolbox should be open and it has two tabs, they are:

   (a) Avilable Signals tab has the following fields:

   Name: Select the name of the variable in Scope_main from the drop-down menu. Click on Refresh if no variables are seen in the Name drop-down menu.

   Input: Select the signals, whose spectrum is to be viewed, in Scope_main.

   Dimention: Set this one if the variable chosen is a 1-dimensional vector. If the selected variable has multiple dimensions (outputs of Multiplexer blocks) select which dimension to be viewed.

   (b) FFT Settings tab has the following fields:

   Start time: Select the start time for the signal interval to perform the FFT window.

   Number of cycles: The width of the FFT window in cycles (typically 1 cycle).

   Fundamental frequency: The width of the FFT window cycles in Hz (typically 50 Hz).

   Max frequency: The maximum frequency of the spectrum (typically 5000 Hz).

   Display style: The amplitude (or y-axis) of the spectrum, select Bar (relative to specified base).

   Base value: Set to 1.

   Frequency Axis: Select Hertz.

8. Click on Compute FFT to view the spectrum. If no spectrum is visible try changing the FFT window by selecting a different Start time. The frequency components of the signal are shown here as their peak values.

9. Record the magnitudes of the first five dominating harmonic components.

	Bipolar						Unipolar					
	$m_a = 0.9$			$m_a = 0.5$			$m_a = 0.9$			$m_a = 0.5$		
	f_h [Hz]	U_{abh} [V]	U_{outh} [V]	f_h [Hz]	U_{abh} [V]	U_{outh} [V]	f_h [Hz]	U_{abh} [V]	U_{outh} [V]	f_h [Hz]	U_{abh} [V]	U_{outh} [V]
1												
2												
3												
4												
5												

Questions

Answer the questions presented, in this section, in the report.

Some Tips:

1. Identify the fundamental frequency component of the converter output voltage (U_{ab1}) and load voltage (U_{out1}) and fill in Table 4.5.

2. The frequency ratio, m_f is
$$m_f = f_{sw}/f_1. \tag{4.3}$$

3. Identify the dominating switching harmonics and determine the corresponding frequency ratio.
$$m_{fh} = f_h/f_1, \tag{4.4}$$
where f_h denotes the frequency of the dominating switching harmonics in Hz.

4. Calculate the total RMS voltages based on the dominating harmonics (Consider the 5 largest harmonics).
$$U_{ab} = \sqrt{U_{ab1}^2 + \sum_{k=1}^{5} U_{abhk}^2} \qquad U_{out} = \sqrt{U_{out1}^2 + \sum_{k=1}^{5} U_{outhk}^2}, \tag{4.5}$$
where U_{ab1} and U_{out1} are the peak voltages at the fundamental frequency of 50 Hz, and U_{abhk} and U_{outhk} are the peak voltages at the frequency of hk Hz. $h1$, $h2$, $h3$, ... are the frequencies of the dominating harmonics.

5. Determine the THD, using the following relation:
$$\text{THD}_{ab} = \frac{\sqrt{\sum_{k=1}^{5} U_{abhk}^2}}{U_{ab1}} \qquad \text{THD}_{out} = \frac{\sqrt{\sum_{k=1}^{5} U_{outhk}^2}}{U_{out1}}. \tag{4.6}$$

Note: Ensure consistency with the numerator and the denominators while using (4.6), i.e., if peak values are used in the numerator, then use peak values for the denominator.

Fill Table 4.5.

Table 4.5: Bipolar and unipolar PWM harmonics in simulation.

PWM	m_a -	U_{ab} V	U_{ab1} V	THD_{ab} %	U_{out} V	U_{out1} V	THD_{out} %
Unipolar	0.9						
Bipolar	0.9						
Unipolar	0.5						
Bipolar	0.5						

Questions

1. Compare the results in Table 4.5 with the Generalized harmonics table of a half-bridge inverter output voltage in Table 4.6.

Table 4.6: Generalized harmonics of a half-bridge inverter output voltage for a large m_f.

$h \downarrow \quad m_a \rightarrow$	0.2	0.4	0.6	0.8	1
1 Fundamental	0.2	0.4	0.6	0.8	1
m_f	1.242	1.15	1.006	0.818	0.6023
$m_f \pm 2$	0.061	0.061	0.131	0.22	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.19	0.326	0.37	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.133
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.088	0.105	0.068
$4m_f \pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.05

Note: output voltage ($\hat{V}_o$) is $\hat{V}_o = m_a V_d/2$.

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