Full-bridge Inverter Manual

Contents

Introduction

This document describes the MOSFET based full-bridge PWM inverter. The inverter, which is implemented on a dedicated PCB (Printed Circuit Board), is controlled through a program in LabVIEW using signal interface through the ELVIS prototyping board.

Initial setup

The LabVIEW files and other files used in the lab can be copied from **/site/edu/eks/TSTE25/current/material/Lab3_files** in Linux or from **U:\eks\TSTE25\current\ material\Lab3_files** in Windows. Put the copied files into your home directory, for example in /edu/<userid>/TSTE25/ on Linux or H:\TSTE25 on Windows.
Please note that the software only works on Windows. You can thus only run the software in the Transistorn lab.

Full-bridge inverter board

We will here get familiarized with the design of the Full-bridge (FB) Inverter. The block diagram is presented in Figure 1, where the functional units are placed in a

similar way as on the physical FB-Inverter board in Figure 2. The FB-inverter is sub-divided into the following blocks:

- Gate pulse logic (Gate pulse interlocking)
- Gate drives for Q1-Q4
- FB-Inverter core (The main FB circuit containing MOSFETs and diodes)

The functional description of the different sub-blocks is found in the corresponding sub-sections further on in this manual.

The detailed view of the FB-Inverter sub-blocks can be found through the corresponding pdf-files found in the Lab3 system folder.

The main circuit for the load current is indicated by the bold red line, starting from the positive outputs from the full-bridge (V_op), passing through the load current sense resistor R28, the external load connections (IO1 and IO2) then back through the on-board power resistor R2 to the negative output of the full-bridge (V_on). The external load connections, IO1 and IO2, are here shorted but can be used to include an external load in series with the 10 ohm power resistor.

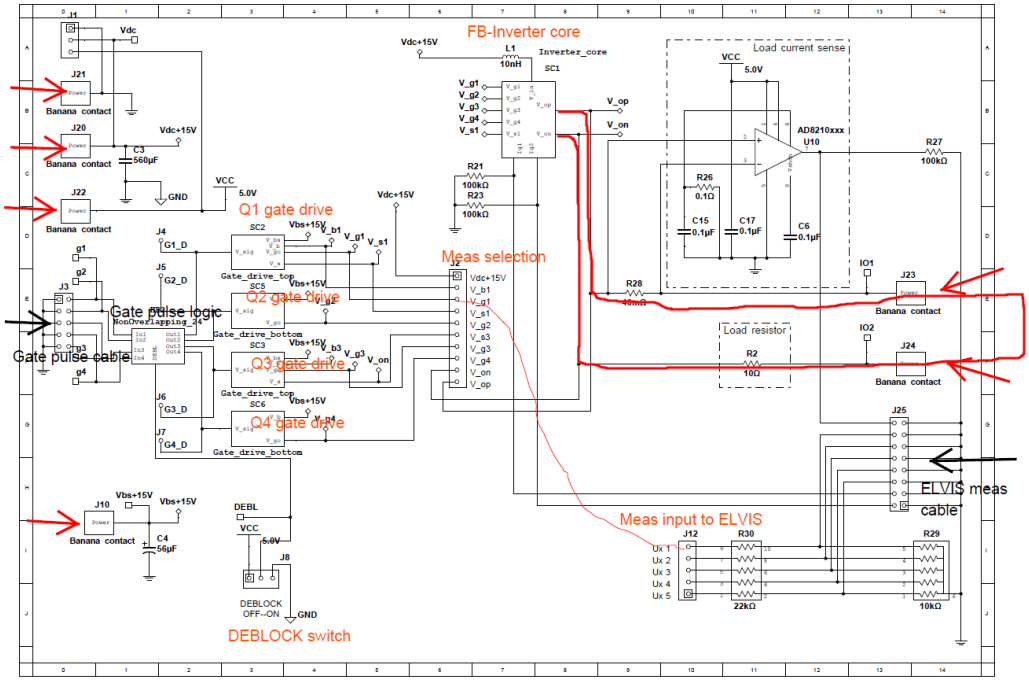

Figure 1 FB-Inverter circuit overview

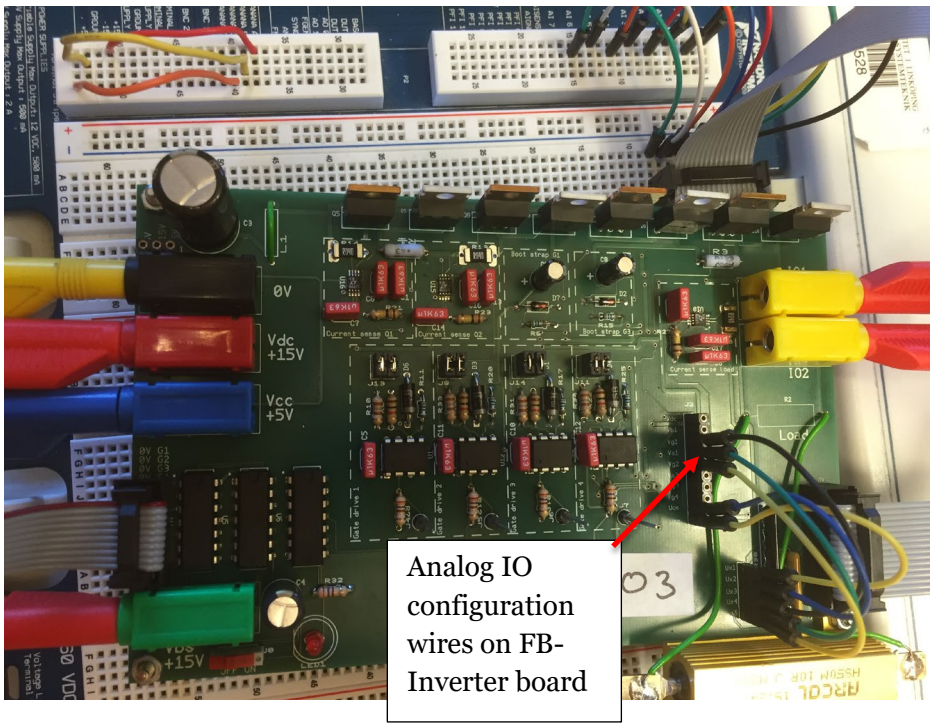

Figure 2 FB-Inverter board

Cable connections

The physical cables required for power supply and signal interface are indicated in Figure 1 by arrows. On the left hand side the 4 banana sockets for power supply connections are found. From the top:

1. 0 V (Black)
2. Vdc +15V (Red). The main dc-voltage supply to the FB-inverter.
3. Vcc +5V (Blue). Supply to digital logic circuits.
4. Vbs +15V (Green). Supply to gate drive circuits including bootstrap of Q1 and Q3

Two yellow banana sockets are located on the opposite side for connection of external load. By connecting these two, the on-board power resistor will be the sole load.

Two flat cables are required to connect gate signals to the full-bridge and to allow measurement signals to be sent back. The flat cable connectors are indicated by black arrows in Figure 1.

1. Gate signals. Left hand side connection in Figure 1 and the lower connection on the physical board (**Fel! Hittar inte referenskälla.**).
2. Measurement signals. Right hand side connection in Figure 1 and the upper connection on the physical board (**Fel! Hittar inte referenskälla.**).

Furthermore, there are a total of 8 measurement signals which can be used from the FB-inverter. 3 of these are dedicated to current sensing while 5 are flexible to setup by selecting among the 10 measurement points, as listed in sub-section "Measurement signals". Selection of the 5 flexible measurement signals are done by installing wires between the corresponding point on the "Meas selection connector" and the "Meas input to ELVIS" as indicated in Figure 1.

Functional description of the FB-Inverter

Gate pulse interlocking

The next block after PWM control is "NonOverlapping" and contains logic to obtain interlocking between G1/G2 and G3/G4 to prevent simultaneous on-state. When G1 is on, G2 must equal zero in order to permit turn-on through G1. The same applies to the other combinations of G1 – G4. The logic also contains a deblock signal which when equal to zero sets all gate pulses to off-state. Enabling of normal switching is done with deblock=1.

Gate drive circuits

The PWM gate pulses are converted into the final gate-source voltage through the circuit showed below:

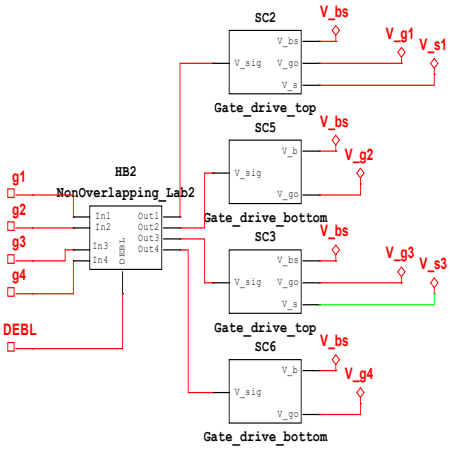

Figure 3 gate drive overview

The gate drive blocks provide isolation in addition to the actual driving of the required gate current for the proper turn-on and turn-off.

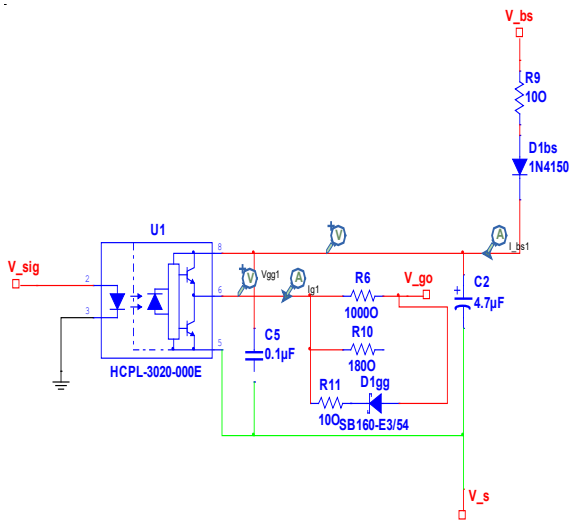

Figure 4 Gate drive of upper switches (Q1 & Q3)

Isolation is provided through the opto-coupler U1 of the type HCPL-3020 by AVAGO Technologies. The data sheet is found in the Lab2 system folder.
The supply to the gate drive is provided by the bootstrap circuit constituted by R9, D1bs and C2 in Figure 4. Bootstrapping is required since the upper switches will see a potential of the source (and gate) that changes through the switching operation. The bootstrap is fed by the dc-voltage source Vdc_bs in Figure 1. Charging of the bootstrap capacitor C2 will commence at the initial turn-on of the main switch Q2 (see Figure 6). The initial charging current will be limited by R2, which also sets a time constant together with the capacitor which defines the speed of charging.

The gate drive provides separate gate resistance for turn-on and turn-off. Turn-on is determined by R6 (can be paralleled by R10) and turn-off by R11 in series with the schottky diode D1gg.

The gate drive for the lower switches Q2 and Q4 does not need the bootstrap circuit due to grounding of the source terminals, allowing the drive circuit to be connected to a normal voltage supply.

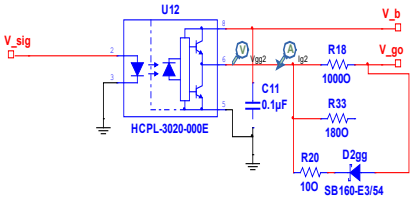

Figure 5 Gate drive for lower switches (Q2 & Q4)

Inverter main circuit

The full-bridge inverter circuit is defined by the “Inverter_core” block in Figure 1, where the following external terminals are found:

V_in: The dc-side voltage
V_op: The positive ac-output terminal
V_on: The negative ac-output terminal

Inside “Inverter-core” the detailed full-bridge inverter circuit is defined as shown by Figure 6. Please note the labeling of the main MOSFETs and diodes not being as per the general notation. The labeling shown in Figure 6 corresponds to labeling found on the FB-Inverter board. However, for general notation the following translation shall be made:

Q1/D1 = Q5/D5
Q2/D2 = Q8/D8
Q3/D3 = Q7/D9
Q4/D4 = Q6/D10

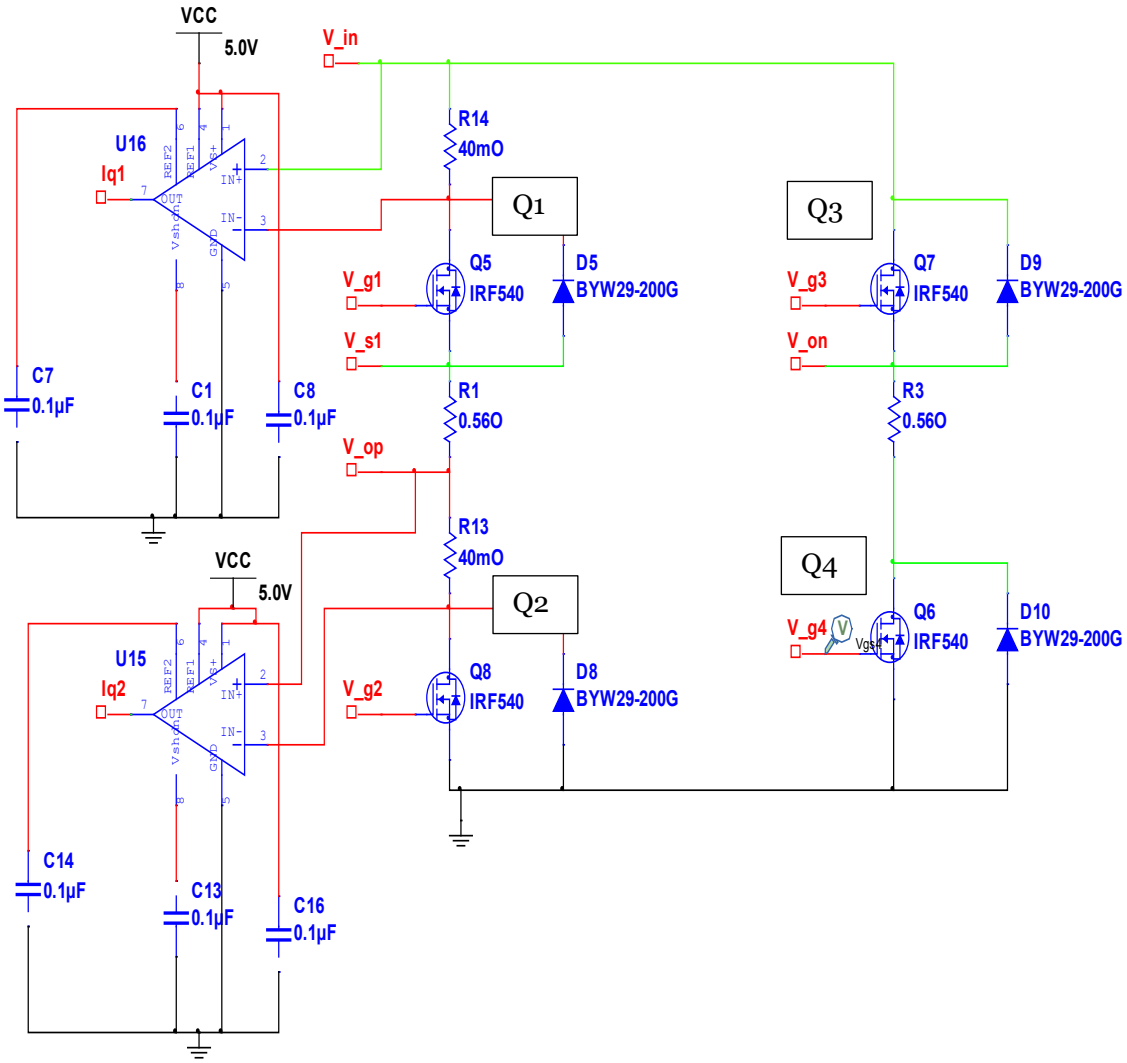

Figure 6 Full-bridge inverter circuit

The full-bridge is designed with MOSFET switches Q1-Q4 of type IRF540 by VISHAY. An antiparallel diode is included with each MOSFET as D1-D4 of the type BYW29E-200. The data sheets for the MOSFET and the diode is found in the Lab2 system folder.

Current sense circuit are included to monitor the current through Q1/D1 (Q5/D5) and Q2/D2 (Q8/D8). The scale factor of the current is 0.4 V/A related to 0.04 ohm current sense resistor and a gain of 10 for the current sense amplifier.

Measurement signals

The FB-Inverter board are setup for output of 8 analog measurement signals. 3 current measurements and 5 voltage measurements. The current signals are derived from current sense amplifiers LT1999IMS-10. As described in previous sub-section, two current sense circuits are monitoring the Q1/D1 and Q2/D2 currents while a third current sense is measuring the load current as shown in Figure 1.

The output of the current sense amplifiers has an offset of 2.5 V with the superimposed voltage related to the measured current with a scaling of 0.4 V/A. Consequently, since the current sense amplifier has a supply voltage of 5V, the peak current that can be measured is 5 A, corresponding to a voltage signal between 0.5 V and 4.5 V.

The five available voltage signals, Ux1-Ux5, are scaled with a factor 0.31 V/V and through flexible wiring selected from the following 10 measurement points.

1. Vdc +15V, the internal dc-side voltage, Vdc, of the full-bridge.
2. V_b1, the bootstrap supply of Q1. [Note: to get the actual gate drive supply voltage V_bs1 of Q1 with reference to the Q1 source, V_b1-V_s1 has to be externally calculated.]
3. V_g1, the gate voltage of Q1. [Note: to get Vgs of Q1, V_g1-V_s1 has to be externally calculated.]
4. V_s1, the source voltage of Q1
5. V_g2, the gate voltage of Q2
6. V_s3, the source voltage of Q3
7. V_g3, the gate voltage of Q3. [Note: to get Vgs of Q3, V_g3-V_s3 has to be externally calculated.]
8. V_g4, the gate voltage of Q4
9. V_on, The negative output voltage with respect to ground (Voltage between Q3 and Q4). [Note: to get the total load voltage V_op-V_on must be externally calculated.]
10. V_op. The positive output voltage with respect to ground (Voltage between Q1 and Q2).

The 8 analog measurements provided are:

1. Load current. (0.4 V/A with 2.5 V offset)
2. Ux1. (0.31 V/V)
3. Ux2. (0.31 V/V)
4. Ux3. (0.31 V/V)
5. Ux4. (0.31 V/V)
6. Ux5. (0.31 V/V)
7. Q1/D1 current. (0.4 V/A with 2.5 V offset)
8. Q2/D2 current. (0.4 V/A with 2.5 V offset)

Converter ratings

The MOSFET based full-bridge converter described here has the following ratings:

- V_{dc} (red terminal) = 40 V
- V_{bs} (green terminal) = 10 V – 20 V (V_{GS} max = 20V)
- V_{out} (m_a = 0.9, V_{dc} = 15 V) = 9.5 Vrms
- I_{out} (R_{load} = 10 ohm, m_a = 0.9, V_{dc} = 15 V) = 0.95 Arms
- P_{out} = 9.1 W
- Power resistor $P_{out,max}$ (without heatsink) = 14 W @ Ta=25C
- MOSFET (IRF540) main data:
    - $V_{DS,max}$ = 100 V
    - $I_{D,max}$ = 20 A (T_{case} = 100C)
    - I_{DM} = 110 A (pulsed drain current)
    - $V_{GS,\ max}$ = 20V
    - R_{DSon} = 0.077 ohm

Datasheets

The following data sheets and application notes are available in the Lab2 system folder for reference it needed:

[1] AN-6076, Design and application guide of bootstrap circuit for high-voltage gate drive IC
[2] BYW29E-200, Ultrafast power diode
[3] HCPL-3020/0302-04-Amp-Output-Current-IGBT-Gate-Drive-Optocoupler
[4] IR MOSFET basics
[5] IRF540, Power MOSFET
[6] Application Note 608, Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance, VISHAY Siliconix
[7] ARCOL HS50, Power resistor
[8] SB160 Schottky barrier rectifier