Examination TSTE25

Date:
Time:
Tentajour:
Permitted aids: A sheet of paper with formulae and a scientific calculator.

Exercise 1. A power transmission company has been tasked with building a 600 kV 5000 MW HVDC link between Stavanger, Norway to Fraserburgh, Scotland. A key component in the HVDC link is the power converter. What is the type and rating of semiconductor switches should they consider for the converter? Motivate. (2 point)

Exercise 2. Consider all components to be ideal in a step-down converter used in a small portable PV phone charger and let the average output voltage (V_o) be held constant at 5 V. If input voltage (V_i) is 10-40 V, output power, $P_o \geq 15$ W, and switching frequency, $f_s = 50$ kHz, calculate the following:

a) The switch duty ratio (D) that is required to maintain the average output voltage of 5 V. (1 point)

b) The minimum inductance (L) required to keep the converter operation in a continuous-conduction mode under all conditions. (4 point)

c) The minimum capacitance (C) required to keep the output peak-to-peak ripple to be 10% of the average output voltage. (2 point)

d) The minimum efficiency of the DC-DC converter. IRF540 MOSFETs are employed (datasheet found at the end of the document) and the voltage and current switching transient times are (4 point)

$$t_{ri} = 19\,\text{ns}, \qquad t_{fv} = 34\,\text{ns}, \qquad t_{rv} = 12\,\text{ns}, \qquad t_{fi} = 16\,\text{ns}.$$

Exercise 3. Consider all components to be ideal in a step-up converter used in a power management system in a vehicle and let the average output voltage (V_o) be held constant at 5 V. If battery voltage on the input side (V_i) is 2.9-4.2 V, $P_o \geq 200$ W, and due to cost limitations, the only available passive components are an inductor, $L = 10\,\mu$H, and several capacitors of $100\,\mu$F. Calculate the following:

a) The switch duty ratio (D) that is required to maintain the average output voltage of 5 V. (1 point)

b) The minimum switching frequency (f_s) required to keep the battery current peak-to-peak ripple below 10% of the average battery current. (4 point)

c) The minimum number of capacitors required to keep the output peak-to-peak voltage ripple below 10% of the average output voltage. (3 point)

Exercise 4. For a half-bridge inverter, assuming all ideal components, the output waveforms are presented in Figure 1, where

$$
\begin{aligned}
\text{peak inverter side voltage} \qquad & \hat{v}_s = 12\,\mathrm{V}, \\
\text{peak inverter side voltage (fundamental)} \qquad & \hat{v}_{s(1)} = 9.61\,\mathrm{V}, \\
\text{peak output current} \qquad & \hat{i}_{out} = 40.1\,\mathrm{A}, \\
\text{peak output voltage} \qquad & \hat{v}_{out} = 11\,\mathrm{V}, \\
\text{peak output voltage (fundamental)} \qquad & \hat{v}_{out(1)} = 8.37\,\mathrm{V}.
\end{aligned}
$$

Determine:

a) The switching frequency used (2 point)

b) The inductance (3 point)

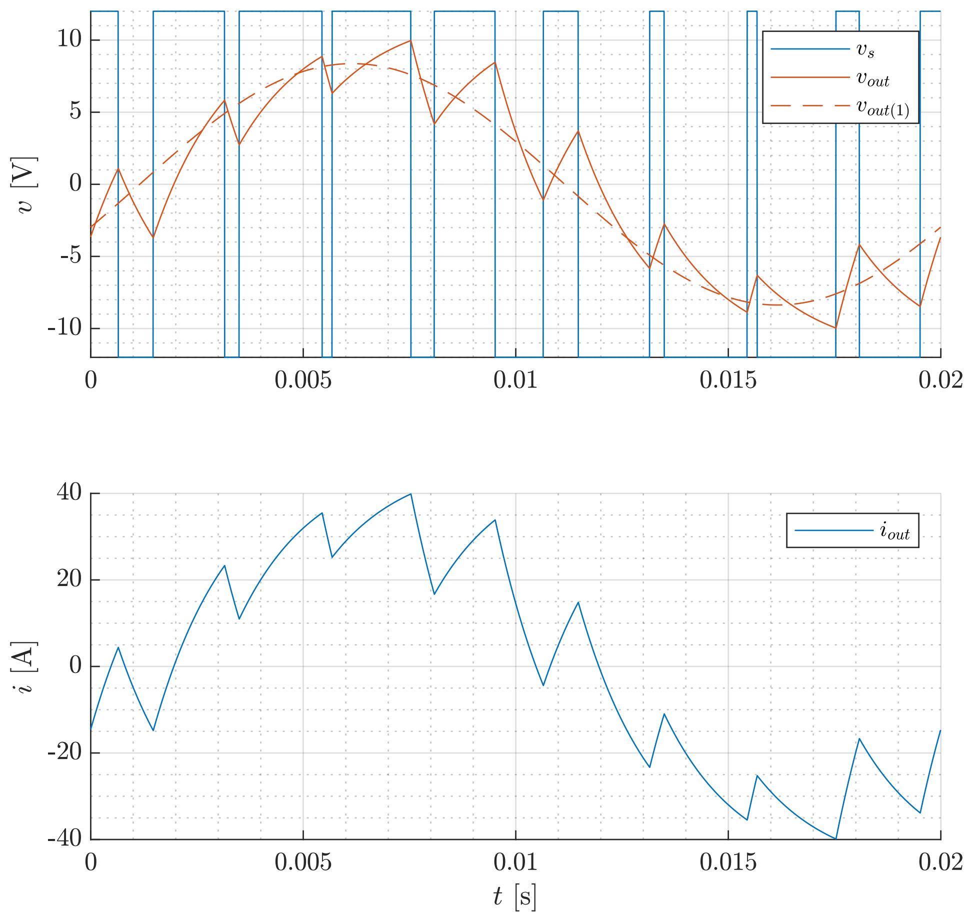
c) The peak fundamental current (2 point)

d) The pole-to-pole DC-link voltage (V_d) and modulation index (m_a) (2 point)

e) The active power on the load at the fundamental frequency. (1 point)

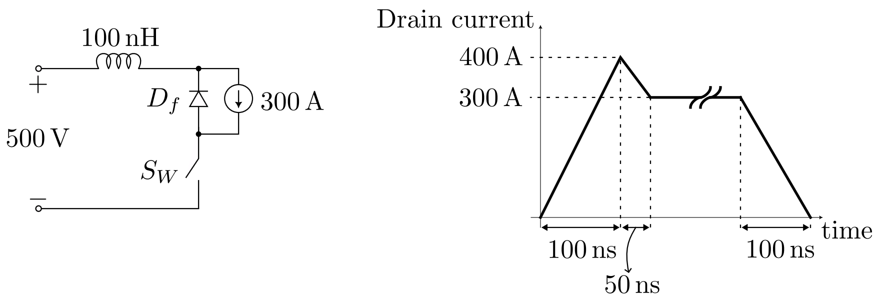
f) The phase angle of the fundamental current with respect to the inverter side voltage. (2 point)

g) The active and reactive power on the converter at the fundamental frequency. (2 point)



Figur 1: half-bridge inverter output waveforms.

Exercise 5. Consider the switched step-down converter shown in Figure 2. The drain current of the MOSFET as a function through one complete turn-on and turn-off sequence is shown in Figure 2. The switch (S_W) and diode (D_f) data are provided in Table 1.



Figur 2: Switched step-down converter and drain current transients.

Tabell 1: switch (S_W) and diode (D_f) data.

S_W data		D_f data	
$V_{ds(\max)}$	700 V	V_{rm}	800 V
$I_{d(\max)}$	400 V	$I_{\max}$	400 A
$T_{j(\max)}$	150°C	$T_{j(\max)}$	150°C
$R_{\theta(\text{ja})}$	0.1°C/W	$R_{\theta(\text{ja})}$	1°C/W
R_{on}	0.01 Ω	R_{on}	0.1 Ω
		V_{on}	0.7 V

a) Sketch and dimension the drain-source voltage of S_W as a function of time. Assume that the voltage across the switch can change instantaneously and is only limited by the external circuit. (4 point)

b) Sketch and dimension the diode voltage as a function of time. (3 point)

c) Are either the diode or the switch overstressed with respect to voltage? If so, specify by how much. (2 point)

d) Determine the junction temperature of the switch and the diode. Do not forget the losses during the switching transients, the diode reverse recovery, a duty cycle of 90%, and assuming a switching frequency of 10 kHz at an ambient temperature of 25°C. (6 point)

Exercise 6. Consider the problem of ripple in the output current of a single-phase full-bridge inverter. Assume $V_{o(1)} = 200\,\text{V}$ and $I_{o(1)} = 10\,\text{A}$ at a frequency of 50 Hz and an induction motor load with inductance of L = 10 mH. Calculate the peak value of the inverter ripple current if the converter is operating in a sinusoidal unipolar PWM mode, with $m_f = 21$ and $m_a = 0.8$. (8 point)

Tabell 2: Generalized harmonics of a half-bridge inverter output voltage for a large m_f.

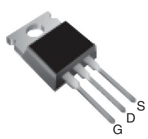
$h \downarrow \quad m_a \rightarrow$	0.2	0.4	0.6	0.8	1
1 Fundamental	0.2	0.4	0.6	0.8	1
m_f	1.242	1.15	1.006	0.818	0.6023
$m_f \pm 2$	0.061	0.061	0.131	0.22	0.318
$m_f \pm 4$					0.018
$2m_f \pm 1$	0.19	0.326	0.37	0.314	0.181
$2m_f \pm 3$		0.024	0.071	0.139	0.212
$2m_f \pm 5$				0.013	0.033
$3m_f$	0.335	0.123	0.083	0.171	0.133
$3m_f \pm 2$	0.044	0.139	0.203	0.176	0.062
$3m_f \pm 4$		0.012	0.047	0.104	0.157
$3m_f \pm 6$				0.016	0.044
$4m_f \pm 1$	0.163	0.157	0.088	0.105	0.068
$4m_f \pm 3$	0.012	0.070	0.132	0.115	0.009
$4m_f \pm 5$			0.034	0.084	0.119
$4m_f \pm 7$				0.017	0.05

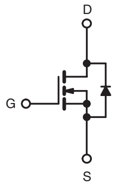
Note: output voltage ($\hat{V}_o$) is $\hat{V}_o = m_a\, V_d/2$.

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.077
Q_g (Max.) (nC)	72	
Q_{gs} (nC)	11	
Q_{gd} (nC)	32	
Configuration	Single	

TO-220





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Pb Available
RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRF540PbF
	SiHF540-E3
SnPb	IRF540
	SiHF540

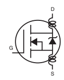
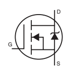
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	28	A
		T_C = 100 °C		20	
Pulsed Drain Current[a]			I_{DM}	110	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	230	mJ
Repetitive Avalanche Current[a]			I_{AR}	28	A
Repetitive Avalanche Energy[a]			E_{AR}	15	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	150	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 440 µH, R_G = 25 Ω, I_{AS} = 28 A (see fig. 12).
c. $I_{SD} \leq$ 28 A, dI/dt $\leq$ 170 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 17 A[b]	-	-	0.077	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 17 A[b]		8.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	1700	-	pF
Output Capacitance	C_{oss}			-	560	-	
Reverse Transfer Capacitance	C_{rss}			-	120	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 17 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	72	nC
Gate-Source Charge	Q_{gs}			-	-	11	
Gate-Drain Charge	Q_{gd}			-	-	32	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 17 A, R_G = 9.1 Ω, R_D = 2.9 Ω, see fig. 10[b]		-	11	-	ns
Rise Time	t_r			-	44	-	
Turn-Off Delay Time	$t_{d(off)}$			-	53	-	
Fall Time	t_f			-	43	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	28	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	110	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 28 A, V_{GS} = 0 V[b]		-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 17 A, dI/dt = 100 A/µs[b]		-	180	360	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.3	2.8	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.