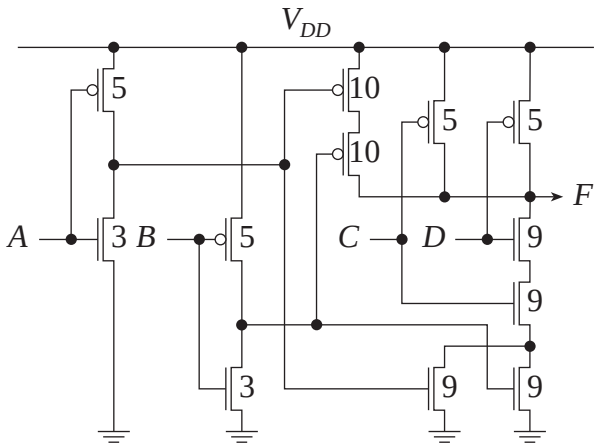
Solutions to exam 2019-10-21 in TSTE86 Digital ICs

1.

a) Switch nets for function *F*:

$$F = AB + \overline{CD} = AB + \overline{C} + \overline{D} \Rightarrow \begin{cases} S_p = F(\overline{A},\overline{B},\overline{C},\overline{D}) = \overline{A}\overline{B} + C + D \\ S_n = \overline{F(A,B,C,D)} = \overline{\overline{A}\overline{B} + C + D} = \left(\overline{A} + \overline{B}\right)CD \end{cases}$$

Two inverters are needed for *A′* and *B′*. Transistor schematic:



b) Aspect ratios are indicated directly by the transistors in the schematic above

2.

From the data it can be seen that $V_{DS} > V_{DSAT}$ for all sets $\Rightarrow$ no operating mode is resistive. To decide between saturated and velocity saturated operating modes we need to compare V_{GT} and V_{DSAT} = 0.58 V. Inspecting the data sets we see the smallest $V_{GT} = 2 - V_T$. Hence we obtain that the MOSFET is velocity saturated for all sets if $2 - V_T < 0.58 \Rightarrow V_T \leq 1.42$ V, which seems likely, so let us guess that and verify it later.

$$I_D = \left(k' \frac{W}{L} V_{DSAT}\right)\left(V_{GS} - V_{T0} - \frac{V_{DSAT}}{2}\right)\left(1 + \lambda V_{DS}\right) = P_1 \cdot P_2 \cdot P_3$$

a) Find V_{T0} e.g. by comparing the relative currents of data set 1 and 2

$$\frac{I_{D1}}{I_{D2}} = \frac{P_1\left(2.5 - V_{T0} - \frac{0.58}{2}\right)P_3}{P_1\left(2.0 - V_{T0} - \frac{0.58}{2}\right)P_3} = \frac{1812}{1297} \Rightarrow V_{T0} \approx 0.45 \text{ V}$$

b) γ is easy to solve if we solve c) first

c) We can find $2|\Phi_F|$ in the V_T-equation for data set 4 and 5, so we start by finding V_T:s

Data set 2 is numerically close to 4 and 5, so we use that in calculations of V_{T4} and V_{T5}

$$\frac{I_{D2}}{I_{D4}} \approx \frac{P_1\left(2-0.45-\frac{0.58}{2}\right)P_3}{P_1\left(2-V_{T4}-\frac{0.58}{2}\right)P_3} = \frac{1297}{1141} \Rightarrow V_{T4} \approx 0.60 \text{ V}$$

$$\frac{I_{D2}}{I_{D5}} \approx \frac{P_1\left(2-0.45-\frac{0.58}{2}\right)P_3}{P_1\left(2-V_{T5}-\frac{0.58}{2}\right)P_3} = \frac{1297}{1039} \Rightarrow V_{T5} \approx 0.70 \text{ V}$$

Now we use the relation $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$ to find $2|\Phi_F|$

$$\text{Let } x = 2\phi_F\,(<0) \Rightarrow \frac{V_{T4}-V_{T0}}{V_{T5}-V_{T0}} = \frac{\sqrt{|1-x|}-\sqrt{|x|}}{\sqrt{|2-x|}-\sqrt{|x|}} = \frac{\sqrt{1-x}-\sqrt{-x}}{\sqrt{2-x}-\sqrt{-x}} \approx \frac{0.60-0.45}{0.70-0.45} \Rightarrow$$

$$x \approx -0.60 \text{ V} \Rightarrow 2\left|\phi_F\right| \approx 0.60 \text{ V}$$

b) *continued*

Insert numerical values into e.g. set 4

$$V_{T4} = V_{T0} + \gamma\left(\sqrt{\left|V_{SB4} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right) \approx 0.45 + \gamma\left(\sqrt{\left|1-(-0.60)\right|} - \sqrt{\left|-0.60\right|}\right) \approx 0.60$$

$$\Rightarrow \gamma \approx 0.30 \text{ V}^{1/2}$$

d) To find *W*/*L*, we e.g. start by finding λ from data set 2 and 3 that are numerically close

$$\frac{I_{D2}}{I_{D3}} = \frac{P_1P_2\left(1+\lambda\cdot 1.8\right)}{P_1P_2\left(1+\lambda\cdot 2.5\right)} = \frac{1297}{1361} \Rightarrow \lambda \approx 0.081 \text{ V}^{-1}$$

W/*L* can now be found from any of data sets, e.g. set 2

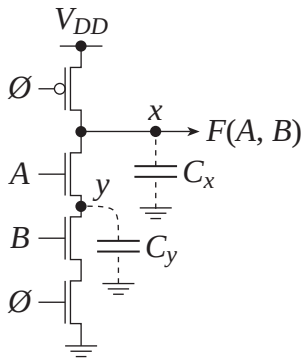
$$I_{D2} \approx 122\cdot 10^{-6}\cdot\frac{W}{L}\cdot 0.58\cdot\left(2-0.45-\frac{0.58}{2}\right)\left(1+0.081\cdot 1.8\right) \approx 1297\cdot 10^{-6} \Rightarrow \frac{W}{L} \approx 13$$

a), b), c), d): check assumption on threshold voltages

$$\left.\begin{array}{l} V_{BS1} = V_{BS2} = V_{BS3} = 0 \Rightarrow V_{T1} = V_{T2} = V_{T3} = V_{T0} \approx 0.45 \text{ V} \le 1.42 \text{ V} \\ V_{T4} \approx 0.60 \text{ V} \le 1.42 \text{ V} \\ V_{T5} \approx 0.70 \text{ V} \le 1.42 \text{ V} \end{array}\right\} \Rightarrow \text{assumption is ok}$$

3.

a) $F(A,B) = \overline{AB} \Rightarrow S_n = AB$. The corresponding transistor schematic is shown in the figure to the right.

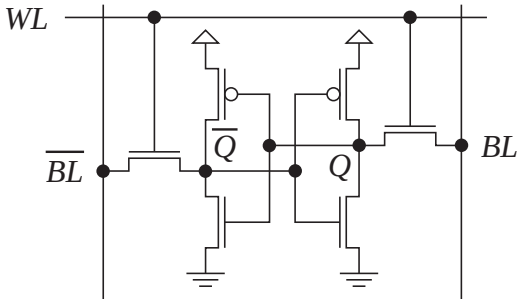


b) Capacitance C_x of node *x* indicated in the figure above is first precharged to V_{DD}, which is done by setting clock Ø low. Then the evaluation starts by setting clock Ø high, where a low *A* or low *B* disconnects the output from the supply, causing *F*(*A*, *B*) to remain at approximately V_{DD} due to the previous precharge. If instead both *A* and *B* are high, the output is discharged and becomes low.

c) For case *F*(*A*, *B*) = *F*(0, 1), capacitance C_y of node *y* indicated in the figure above is discharged. If the next evaluation is *F*(*A*, *B*) = *F*(1, 0), the voltage of node *x* should remain at V_{DD}, but is instead reduced due to sharing of C_x's charge with C_y. Depending on how much the output voltage is reduced, we may need to redesign the circuit to ensure proper operation.

4.

a) Transistor schematic of a six-transistor CMOS SRAM cell



b) For example, to store $\bar{Q}$ = 0, Q = 1, WL is initially set to 0, $\overline{BL}$ is set to 0, and BL is set to 1. Then WL is pulsed high long enough to allow the cross coupled inverter pair to change state hence storing the wanted content.

c) To read the cell content, WL is initially 0 while $\overline{BL}$ and BL are precharged to 1. Then WL is pulsed high long enough for the sense amplifier to detect the voltage drop on the bit-line that is pulled towards 0 by the weak transistors in the cell. Finally the sense amplifier amplifies the voltage difference to a full swing 0 and the result is output.

d) For proper read operation, the ratio between the pull-down NMOSFET and the select NMOSFET needs to be designed high enough to prevent the memory node from changing state from 0 to 1 when the cell is connected to the precharged bit-line. For proper write operation, the ratio between the pull-up PMOSFET and the select NMOSFET must be designed low enough to allow a 0 on the bit-line change the state of the corresponding memory node.

5.

a) Resistor and capacitor values

$$R_{AC} = \frac{l_{AC}}{W_{wire}} R_{sheet} = \frac{3 \cdot 10^{-3}}{4 \cdot 10^{-6}} \cdot 0.25\ \Omega \approx 190\ \Omega$$

$$R_{BC} = \frac{l_{BC}}{W_{wire}} R_{sheet} = \frac{2 \cdot 10^{-3}}{4 \cdot 10^{-6}} \cdot 0.25\ \Omega \approx 120\ \Omega$$

$$R_{CD} = \frac{l_{CD}}{W_{wire}} R_{sheet} = \frac{4 \cdot 10^{-3}}{4 \cdot 10^{-6}} \cdot 0.25\ \Omega \approx 250\ \Omega$$

$$R_{CE} = \frac{l_{CE}}{W_{wire}} R_{sheet} = \frac{6 \cdot 10^{-3}}{4 \cdot 10^{-6}} \cdot 0.25\ \Omega \approx 380\ \Omega$$

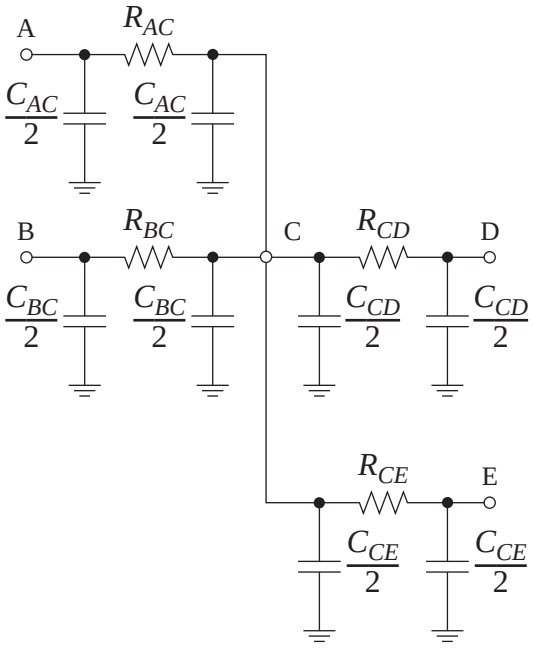
$$C_{AC} = l_{AC} W_{wire} C_{area} = 3 \cdot 10^{-3} \cdot 4 \cdot 10^{-6} \cdot 0.06 \cdot 10^{-3}\ \text{F} = 720\ \text{fF}$$

$$C_{BC} = l_{BC} W_{wire} C_{area} = 2 \cdot 10^{-3} \cdot 4 \cdot 10^{-6} \cdot 0.06 \cdot 10^{-3}\ \text{F} = 480\ \text{fF}$$

$$C_{CD} = l_{CD} W_{wire} C_{area} = 4 \cdot 10^{-3} \cdot 4 \cdot 10^{-6} \cdot 0.06 \cdot 10^{-3}\ \text{F} = 960\ \text{fF}$$

$$C_{CE} = l_{CE} W_{wire} C_{area} = 6 \cdot 10^{-3} \cdot 4 \cdot 10^{-6} \cdot 0.06 \cdot 10^{-3}\ \text{F} = 1440\ \text{fF}$$

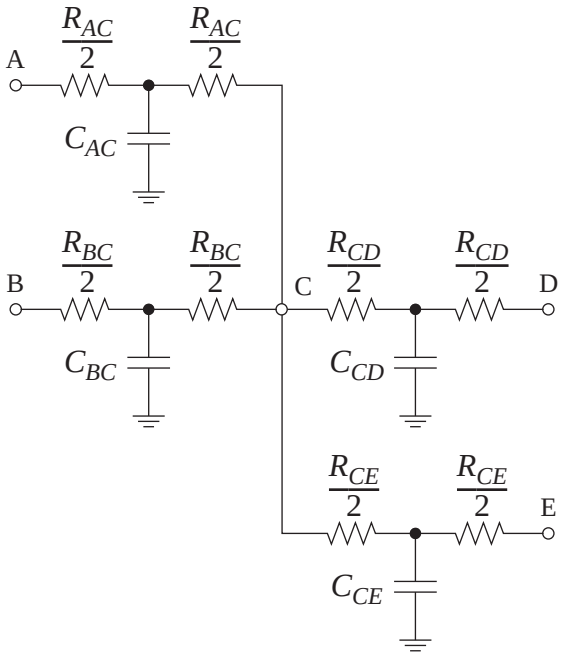
b) Interconnect model based on π models



Total capacitance of node *C* is

$$C_C = \frac{C_{AC}}{2} + \frac{C_{BC}}{2} + \frac{C_{CD}}{2} + \frac{C_{CE}}{2} = 1800\ \text{fF}$$

c) Interconnect model based on T-models



d) Elmore delay time constant based on the π models in b)

$$\tau_\pi = R_{AC}\left(\frac{C_{AC}}{2} + 2\frac{C_{BC}}{2} + 2\frac{C_{CD}}{2} + \frac{C_{CE}}{2}\right) + \left(R_{AC} + R_{CE}\right)\frac{C_{CE}}{2} \approx 0.88 \text{ ns}$$

Elmore delay time constant based on the T models in c)

$$\tau_\pi = \frac{R_{AC}}{2}C_{AC} + 2\frac{R_{AC}}{2}\left(C_{BC} + C_{CD}\right) + \left(2\frac{R_{AC}}{2} + \frac{R_{CE}}{2}\right)C_{CE} \approx 0.88 \text{ ns}$$

Since $\tau_\pi = \tau_T$, there is no difference in propagation delay for these models

The propagation delay is in both cases $t_p = 0.38\tau_\pi = 0.38\tau_T \approx 0.33$ ns

6.

a) *Logic synthesis*: Tools translate an HDL design description into a netlist.

b) *Placement*: Precise positioning of the cells is decided.

c) *Routing*: Interconnections are wired.

d) *Tape out*: All information needed for mask generation is collected into a binary file and sent to the ASIC vendor.