Solutions to exam 2019-08-30 in TSTE86 Digital ICs

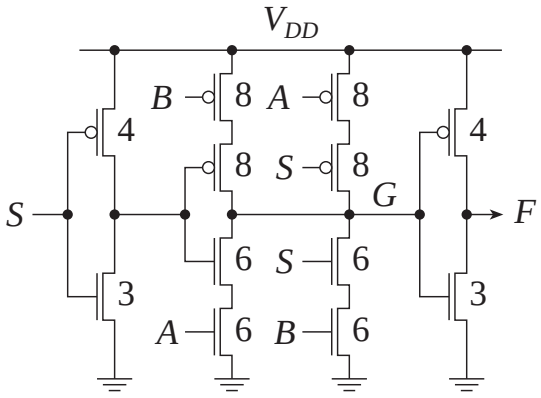
1.

a) Three inverters are needed if we implement *F* directly, while two are sufficient if we first implement the inverted function $G = \bar{F}$ and then invert the output to obtain F.

Design switch net functions for *G*:

$$G = \overline{A\bar{S} + BS} \Rightarrow \begin{cases} S_p = G(\bar{A}, \bar{B}, \bar{S}) = \overline{\bar{A}S + \bar{B}\bar{S}} = (A + \bar{S})(B + S) = AS + B\bar{S} \\ S_n = \overline{G(A, B, S)} = A\bar{S} + BS \end{cases}$$

Two CMOS inverters are added for inverting *S* and *G*. Complete transistor schematic:



b) Aspect ratios are indicated directly by the transistors in the schematic above.

2.

a) Find MOSFET's operating mode at V_M

$$V_{min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(V_M - V_{Tn}, V_M, V_{DSAT}\right) =$$
$$= \min\left(1.25 - 0.43, 1.25, 0.63\right)\ \text{V} = 0.63\ \text{V} \Rightarrow \text{velocity saturated}$$

Equate current through resistor with current through MOSFET to obtain R_L

$$\frac{V_{DD} - V_M}{R_L} = k' \frac{W}{L} V_{min}\left(V_{GT} - \frac{V_{min}}{2}\right)\left(1 + \lambda V_{DS}\right) \Leftrightarrow$$
$$\frac{2.5 - 1.25}{R_L} = 115 \cdot 10^{-6} \cdot \frac{2.5}{0.25} \cdot 0.63 \cdot \left(1.25 - 0.43 - \frac{0.63}{2}\right)\left(1 + 0.06 \cdot 1.25\right) \Rightarrow R_L \approx 3.2\ \text{k}\Omega$$

b) MOSFET is off during charge $\Rightarrow t_{pLH} = 0.69 R_L C_L$

Find t_{pHL} by discharging C_L from V_{DD} to $V_{DD}/2$

MOSFET's operating mode at $V_{out} = V_{DD}$

$$V_{min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(V_{DD} - V_{Tn}, V_{DD}, V_{DSAT}\right) =$$
$$= \min\left(2.5 - 0.43, 2.5, 0.63\right)\ \text{V} = 0.63\ \text{V} \Rightarrow \text{velocity saturated}$$

Derive an expression for the discharge current at V_{DD}

$$I_D\left(V_{DD}\right) = k'\frac{W}{L}V_{min}\left(V_{DD} - V_{Tn} - \frac{V_{min}}{2}\right)\left(1 + \lambda V_{DD}\right) =$$

$$= 115\cdot 10^{-6}\cdot\frac{2.5}{0.25}\cdot 0.63\cdot\left(2.5 - 0.43 - \frac{0.63}{2}\right)\left(1 + 0.06\cdot 2.5\right)\ \text{A} \approx 1.46\cdot 10^{-3}\ \text{A}$$

MOSFET's operating mode at $V_{out} = V_{DD}/2$

$$V_{min} = \min\left(V_{DD} - V_{Tn}, \frac{V_{DD}}{2}, V_{DSAT}\right) =$$

$$= \min\left(2.5 - 0.43, 1.25, 0.63\right)\ \text{V} = 0.63\ \text{V} \Rightarrow \text{velocity saturated}$$

Derive an expression for the discharge current at $V_{DD}/2$

$$I_D\left(\frac{V_{DD}}{2}\right) = k'\frac{W}{L}V_{min}\left(V_{DD} - V_{Tn} - \frac{V_{min}}{2}\right)\left(1 + \lambda\frac{V_{DD}}{2}\right) - \frac{V_{DD}/2}{R_L} =$$

$$= 115\cdot 10^{-6}\cdot\frac{2.5}{0.25}\cdot 0.63\cdot\left(2.5 - 0.43 - \frac{0.63}{2}\right)\left(1 + 0.06\cdot 1.25\right) - \frac{1.25}{R_L}\ \text{A} =$$

$$\approx 1.37\cdot 10^{-3}\,\text{A} - \frac{1.25}{R_L}$$

Approximate t_{pHL} by calculating discharge of C_L with average current

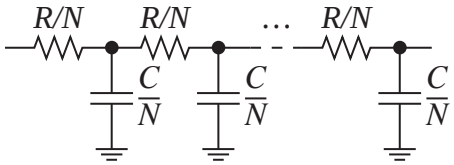
$$t_{pHL} = \frac{C_L V_{DD} - C_L\frac{V_{DD}}{2}}{\frac{1}{2}\left(I\left(V_{DD}\right) + I\left(\frac{V_{DD}}{2}\right)\right)} = \frac{C_L V_{DD}}{I\left(V_{DD}\right) + I\left(\frac{V_{DD}}{2}\right)} \approx \frac{C_L\cdot 2.5}{\left(1.46 + 1.37\right)\cdot 10^{-3} - \frac{1.25}{R_L}}$$

Equate t_{pLH} and t_{pHL} and solve for R_L

$$t_{pHL} = t_{pLH} \Rightarrow \frac{C_L\cdot 2.5}{\left(1.46 + 1.37\right)\cdot 10^{-3} - \frac{1.25}{R_L}} \approx 0.69 R_L C_L \Rightarrow R_L \approx 1.7\ \text{k}\Omega$$

3.

a) *RC*-chain model with *N* identical segments



b) $$\tau = \frac{R}{N}\cdot\frac{C}{N} + \frac{2R}{N}\cdot\frac{C}{N} + \ldots\frac{NR}{N}\cdot\frac{C}{N} = \frac{RC}{N^2}\sum_{i=1}^{N} i = \frac{RC}{N^2}\cdot\frac{N\left(N+1\right)}{2} = \frac{RC}{2}\left(1 + \frac{1}{N}\right)$$

c) $$\lim_{N\to\infty}\left(\tau\right) = \frac{RC}{2}\lim_{N\to\infty}\left(1 + \frac{1}{N}\right) = \frac{RC}{2}\cdot 1 = \frac{RC}{2}$$

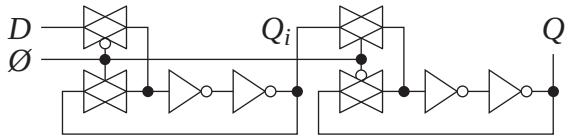
d) $$t_p = \ln\left(2\right)\tau \approx 0.35RC$$

4. Techniques for dealing with capacitive cross talk

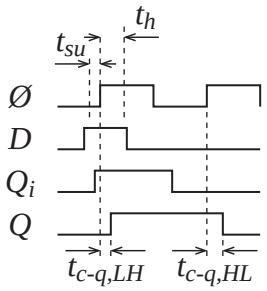
1. Avoid floating nodes by e.g. introducing keeper devices.
2. Separate sensitive nodes from full-swing signals.
3. Make the rise and fall time as large as possible.
4. Use differential signaling to turn cross talk into a common-mode noise.
5. Avoid large capacitance between wires, e.g. parallel wires over long distance
6. Provide a shielding wire connected to the ground or power supply between wires.
7. Reduce interwire capacitance by adding extra routing layers.

5.

a) Positive edge-triggered master-slave D flip-flop



b) Timing diagram



Setup time t_{su}: The time before the rising edge of the clock that the input data D must be valid.

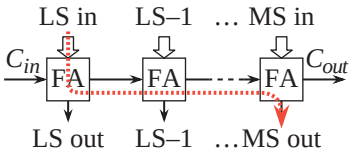
Hold time t_h: The time that the input must be held stable after the rising edge of the clock. Note that the hold time of a circuit can be negative in certain situations.

Clock-to-output delays $T_{c\text{-}q,LH}$ and $T_{c\text{-}q,HL}$: The time after the clock edge before the output Q is stable.

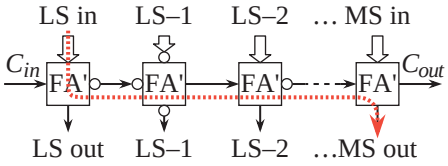
If the setup time or the hold time is violated the circuit might enter a metastable, undecided, state. The output will eventually reach a stable point, either high or low, but the final state will be more or less random.

6. Block schematics with critical path in red-dash (LS = least significant, MS = most significant)

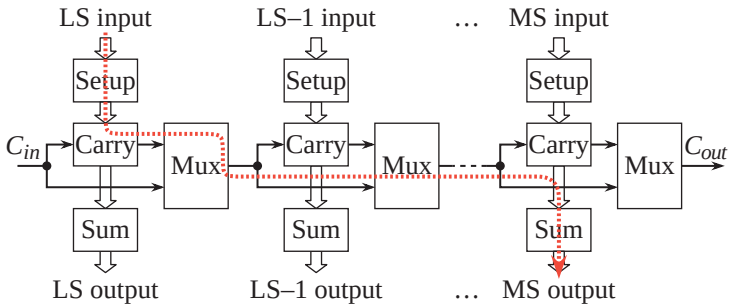
a) Ripple-carry



b) Ripple-carry with inverter elimination (two types of FA:s with carry inversion)



c) Carry-skip



d) Carry-select