Solutions to exam 2018-10-22 in TSTE86 Digital ICs

1.

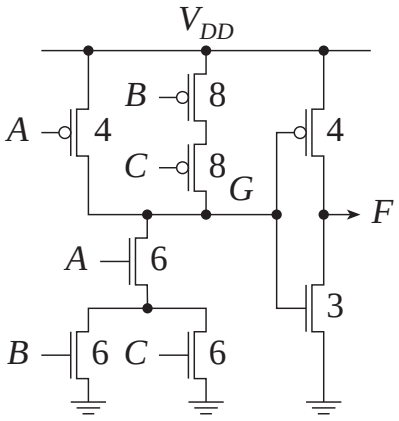
a) Simplify the logic function to contain as few variable entries as possible

$$F = AB + AC = A\left(B + C\right)$$

Since a static CMOS gate is inverting, we can design the function as the inverted output $G = F'$ and add an inverter to the output to obtain F
Switch nets for function G

$$G = \overline{A\left(B+C\right)} \Rightarrow \begin{cases} S_p = G(\overline{A},\overline{B},\overline{C}) = \overline{\overline{A}\left(\overline{B}+\overline{C}\right)} = A + BC \\ S_n = \overline{G(A,B,C)} = A\left(B+C\right) \end{cases}$$

Transistor schematic



b) The worst-case resistance occurs when a single path conducts. A common sizing strategy is to design the widths of every single conduction path to be equal (when possible). Using $R \propto L/W$, the aspect ratios shown by the transistors in the schematic above can be calculated using this strategy

2.

a) $\underline{V_{OH}}$: Assume $V_{in} = V_{OL} < V_T \Rightarrow V_{GSn} < V_T \Rightarrow$ nMOSFET cutoff $\Rightarrow V_{out} = V_{OH} = 2.5$ V
Assumption is checked after V_{OL} calculation below

$\underline{V_{OL}}$: $V_{min,n} = \min\left(V_{DD} - V_{T0n},\ V_{OL},\ V_{DSATn}\right) \rightarrow \left\langle \text{saturated, resistive, velocity sat.} \right\rangle$

Assume well designed circuit with $V_{OL} < 1\text{ V} < V_{DSATn} < V_{DD} - V_{T0n} \Rightarrow$ NMOS resistive

$V_{min,p} = \min\left(\left|0 - V_{DD} - V_{T0p}\right|,\ \left|V_{OL} - V_{DD}\right|,\ \left|V_{DSATp}\right|\right) \rightarrow \left\langle \text{saturated, resistive, velocity sat.} \right\rangle$

Assume well designed circuit with $V_{OL} < 1\text{ V} \Rightarrow$ PMOS velocity saturated

$$I_{Dn} = -I_{Dp} \Rightarrow k'_n \frac{W_n}{L_n} V_{OL}\left(V_{DD} - V_{T0n} - \frac{V_{OL}}{2}\right) = -k'_p \frac{W_p}{L_p}\left|V_{DSATp}\right|\left(\left|0 - V_{DD} - V_{T0p}\right| - \frac{\left|V_{DSATp}\right|}{2}\right)$$

Numerically: $115\cdot10^{-6}\cdot12\cdot V_{OL}\left(2.07-\frac{V_{OL}}{2}\right)=-30\cdot10^{-6}\cdot1\cdot1\cdot\left(2.1-\frac{1}{2}\right)\Rightarrow$

$$V_{OL}^2-2\cdot2.07V_{OL}-\frac{2\cdot30\cdot1.6}{115\cdot12}=0\Rightarrow V_{OL}=2.07\pm\sqrt{2.07^2-\frac{9}{115}}\text{ V}\approx\begin{cases}0.019\text{ V}\\(4.12\text{ V}>1\text{ V})\end{cases}$$

Check assumptions

V_{OL} = 0.019 V < V_T = 0.43 V — first assumption is ok

$V_{min,n}$ = min(2.07, 0.019, 0.63) V → resistive — second assumption is ok

$V_{min,p}$ = min(2.1, 2.481, 1) V → velocity saturated — final assumption is ok

b) $\underline{t_{pLH}}$: $V_{GSn}=V_{OL}<V_T\Rightarrow$ nMOSFET cutoff

$$V_{min,p}=\min\left(V_{DD}+V_{T0p},V_{DD}-V_{out},\left|V_{DSATp}\right|\right)=\left|V_{DSATp}\right|,\ V_{out}\le\left(V_{OH}-V_{OL}\right)/2\approx1.24\text{ V}$$

$$I_{DSATp}=k'_p\frac{W_p}{L_p}V_{DSATp}\left(V_{DD}+V_{T0p}+\frac{V_{DSATp}}{2}\right)=-30\cdot10^{-6}\cdot1\cdot(-1)\left(2.5-0.4-\frac{1}{2}\right)\text{ A}=48\text{ µA}$$

$$t_{pLH}=\frac{\Delta Q}{I_{av}}\approx\frac{CV_{DD}/2}{I_{DSAT,P}}=\frac{100\cdot10^{-15}\cdot2.5/2}{48\cdot10^{-6}}\text{ s}\approx2.6\text{ ns}$$

$\underline{t_{pHL}}$: $V_{min,n}=\min\left(V_{DD}-V_{T0n},V_{out},V_{DSATn}\right)=V_{DSATn},\ V_{out}\ge\left(V_{OH}-V_{OL}\right)/2\approx1.24$ V

$$I_{DSATn}=k'_n\frac{W_n}{L_n}V_{DSATn}\left(V_{DD}-V_{T0n}-\frac{V_{DSATn}}{2}\right)=115\cdot10^{-6}\frac{3}{0.25}0.63\left(2.07-\frac{0.63}{2}\right)\text{ A}\approx1.5\text{ mA}$$

$$V_{out1}=V_{OH}\Rightarrow V_{min,p}=\min\left(V_{DD}+V_{T0p},V_{DD}-V_{out1},\left|V_{DSATp}\right|\right)=V_{DD}-V_{out1}=0\Rightarrow I_{D1}=0$$

$$V_{out2}=\frac{V_{OH}-V_{OL}}{2}\Rightarrow V_{min,p}=\min\left(V_{DD}+V_{T0p},V_{DD}-V_{out2},\left|V_{DSATp}\right|\right)=\left|V_{DSATp}\right|\Rightarrow I_{D2}=I_{DSATp}$$

$$t_{pHL}=\frac{\Delta Q}{I_{av}}\approx\frac{Q/2}{\left[\left(I_{DSATn}-I_{D1}\right)+\left(I_{DSATn}-I_{D2}\right)\right]/2}=\frac{CV_{DD}}{2I_{DSATn}-I_{DSATp}}=$$

$$=\frac{100\cdot10^{-15}\cdot2.5}{2\cdot1.5\cdot10^{-3}-48\cdot10^{-6}}\text{ s}\approx83\text{ ps}$$

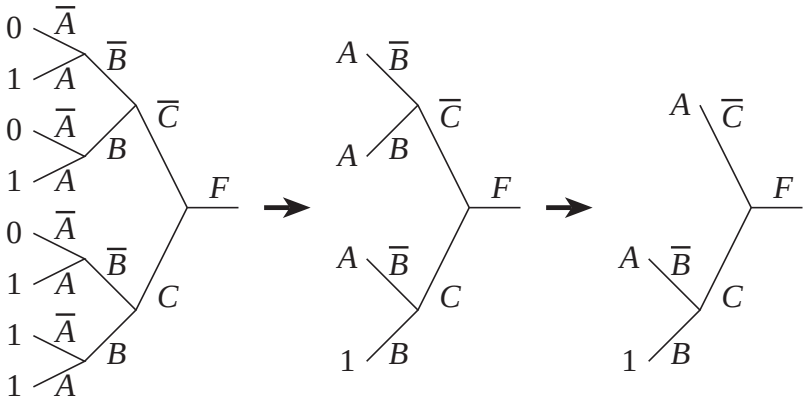
$\underline{t_p}$: $t_p=\left(t_{pHL}+t_{pLH}\right)/2\approx1.3$ ns

3.

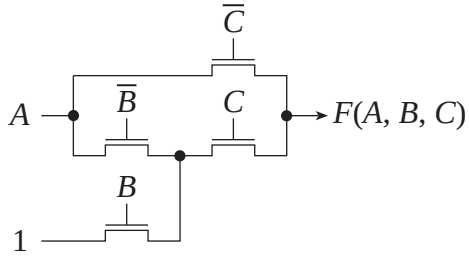
a) Pass transistor logic

b) $A\neq B$, C = 1 yields a short circuit between A and $B\Rightarrow$ output F will be undefined.

c) Below is a binary tree representing the function and its simplification in two steps.

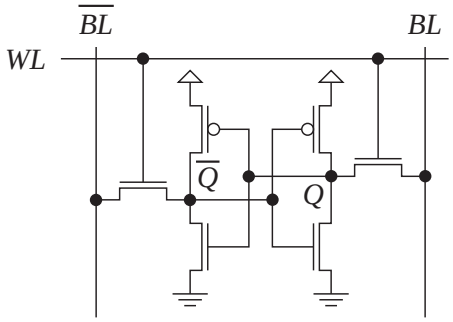


d) The optimized pass transistor circuit is shown below.



4.

a) Transistor schematic of a six-transistor CMOS SRAM cell



b) For example, to store $\bar{Q} = 0$, $Q = 1$, WL is initially set to 0, $\overline{BL}$ is set to 0, and BL is set to 1. Then WL is pulsed high long enough to allow the crosscoupled inverter pair to change state hence storing the wanted content.

c) To read the cell content, WL is initially 0 while $\overline{BL}$ and BL are precharged to 1. Then WL is pulsed high long enough for the sense amplifier to detect the voltage drop on the bit-line that is pulled towards 0 by the weak transistors in the cell. Finally the sense amplifier amplifies the voltage difference to a full swing 0 and the result is output.

d) For proper write operation, the ratio between the pull-up PMOSFET and the select NMOSFET must be designed low enough to allow a 0 on the bit-line change the state of the corresponding memory node. For proper read operation, the ratio between the pull-down NMOSFET and the select NMOSFET needs to be designed high enough to prevent the memory node from changing state from 0 to 1 when the cell is connected to the precharged bit-line.

5.

a) Pipelining is a technique to improve the resource utilization and increase the functional throughput. When splitting logic into smaller and smaller blocks we arrive at the limit, where delays imposed by registers are comparable to delays of the logic blocks. No extra throughput can be achieved at this point, and only the chip area increases.

b) Minimum clock period $T_{\min} = t_{c\text{-}q} + \max(t_{p1},t_{p2},t_{p3}) + t_{su} = 0.7 + \max(3,4,5) + 0.5$ ns = 6.2 ns $\Rightarrow$ max throughput $f_{\max} = 1/T_{\min} \approx 160$ MHz.

c) The time available for a signal to propagate between two successive registers is decreased by the negative skew and we also need to allow for maximum jitter at both the sending and receiving register $\Rightarrow$ minimum clock period $T_{min} = t_{clk\text{-}q} + \max(t_{p1}, t_{p2}, t_{p3}) + t_{su} + \Delta t + 2t_{jitter} = 6.2 + 0.3 + 2 \cdot 0.1$ ns = 6.7 ns.

6.

a) *Logic synthesis*: Tools translate an HDL design description into a netlist

b) *Floor planning*: An overall outlay of the chip is made including power and clock networks

c) *Placement*: Precise positioning of the cells is decided

d) *Routing*: Interconnections are wired

e) *Tape out*: All information needed for mask generation is collected into a binary file and sent to the ASIC vendor