Linköping Institute of Technology
Department of Electrical Engineering, Division of Integrated Circuits and Systems

Exam TEN1 in TSTE86 Digital Integrated Circuits

Time:	Tuesday 7 January 2020, 14:00–18:00
Place:	U1
Responsible teacher:	Mark Vesterbacka, phone 013-281324
Allowed aid:	Calculator
Maximum score:	60 points
Grades:	45 points for 5 35 points for 4 25 points for 3
Solutions:	Posted on the course web
Result:	Posted through LADOK by 23 January 2020

1. A domino logic circuit realizing the function $F(A, B, C)$ is shown in Figure 1. The parasitic capacitances C_x, C_y, C_G, and C_F have been indicated in the schematic.

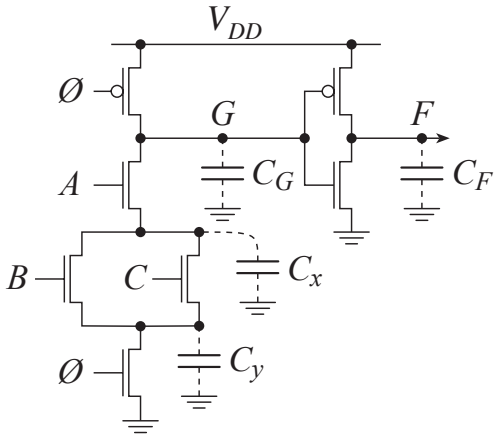

Figure 1. Schematic of a domino logic circuit.

a) What logic function $F(A, B, C)$ has been implemented? (2 p)

b) What is the purpose of the MOSFETs clocked with Ø? (2 p)

c) Can charge sharing occur in the circuit? Motivate your answer. (2 p)

d) Size the devices so that the worst-case output resistance of node G is the same as that of an inverter with an NMOS $W/L = 3$ and PMOS $W/L = 5$. (4 p)

2. An NMOS transistor is plugged into the test configuration shown in Figure 2. Determine the operation region, V_D, and V_S for the two cases below. For simplicity, assume $\lambda = 0$ and $\gamma = 0$.

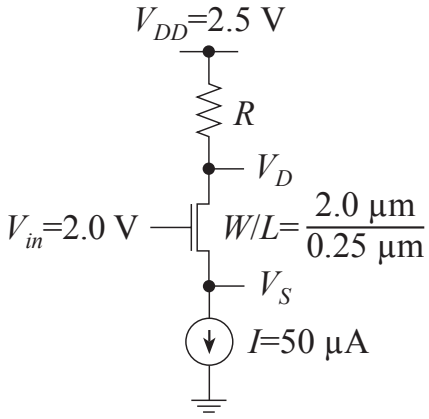

Figure 2. Test configuration for NMOSFET.

a) $R = 10$ kΩ. (5 p)

b) $R = 30$ kΩ. (5 p)

3. A NAND gate shown to the left in Figure 3. To the right in Figure 3, there is a plot showing the output responses of the circuit due to different input transitions.

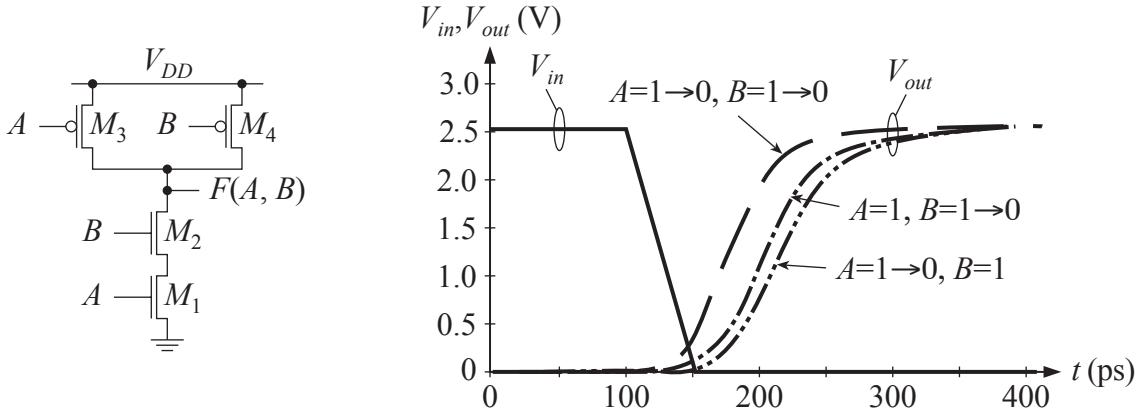

Figure 3. NAND gate and its output response due to different input patterns.

a) Draw an equivalent *RC* switch model for this circuit that includes internal node capacitances. (4 p)

b) Explain why case $A = 1 \rightarrow 0$, $B = 1 \rightarrow 0$ has the smallest delay. (3 p)

c) Explain why case $A = 1 \rightarrow 0$, $B = 1$ is slower than case $A = 1$, $B = 1 \rightarrow 0$. (3 p)

4. A wire is used to connect two inverters as shown in Figure 4. The wire has length $L = 50$ mm, resistance per wire length $r = 0.075$ Ω/μm, and capacitance per wire length $c = 0.11$ fF/μm.

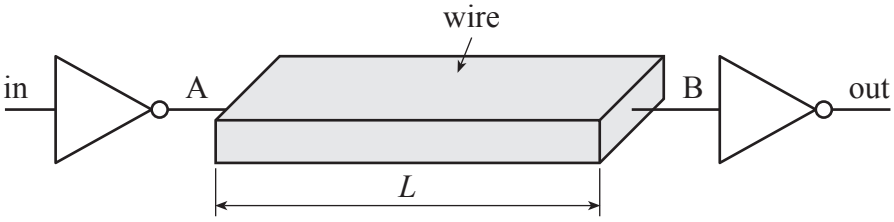

Figure 4. Two inverters connected by a long wire.

a) Estimate the propagation delay between the input 'in' and node 'B' of this circuit. Assume the inverters are identical and have an inherent propagation delay $t_{inv} = 35$ ps and equivalent input/output capacitances $C_{in} = C_{out} = 5.0$ fF. (6 p)

b) What will be the propagation delay when an extra inverter is placed as a repeater in the middle of the wire? Assume the same delay and capacitances for this inverter as for the other two. (4 p)

5. Design a 3-bit Carry-Lookahead Adder (CLA) with inputs $A = \sum_{i=0}^{2} a_i 2^i$, $B = \sum_{i=0}^{2} b_i 2^i$, carry in c_{in}, and outputs $S = \sum_{i=0}^{2} s_i 2^i = A + B$ and carry out c_{out}.

a) State Boolean functions of the output bits s_i using propagate and generate functions. (3 p)

b) State the Boolean function of c_{out} using input bits a_i, b_i, and c_{in}. (3 p)

c) Estimate the critical path of an implementation that uses instances of gates with propagation delay according to Figure 5 below. (4 p)

Gate	Propagation delay
AND = $x \cdot y$	50 ps
ANDOR = $x \cdot y + z$	70 ps
XOR = $x \oplus y$	90 ps

Figure 5. Propagation delay of some basic gates.

6. Consider Design for Testability (DfT) for digital ICs.

a) What is *observability*? (2 p)

b) What is *controllability*? (2 p)

c) What is an *ad-hoc test*? (2 p)

d) What is a *scan-based test*? (2 p)

e) What is a *built-in self-test*? (2 p)

Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***V_{DSAT}* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{\text{V}}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq}C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.