Digital ICs — Lectures

1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
4) **Circuits** [Ch. 5]	*TSEI03/TSTE86*
5) **Combinational logic** [Ch. 6]	*TSEI03/TSTE86*
6) **Sequential circuits** [Ch. 7]	*TSEI03/TSTE86*
7) **Synchronization** [Ch. 10]	*TSTE86*
8) **Adders** [Ch. 11]	*TSEI03/TSTE86*
9) **Multipliers** [Ch. 11]	*TSTE86*
10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
11) **Manufacturing** [Ch. 2]	*TSTE86*
12) **System design** [Ch. 8]	*TSTE86*

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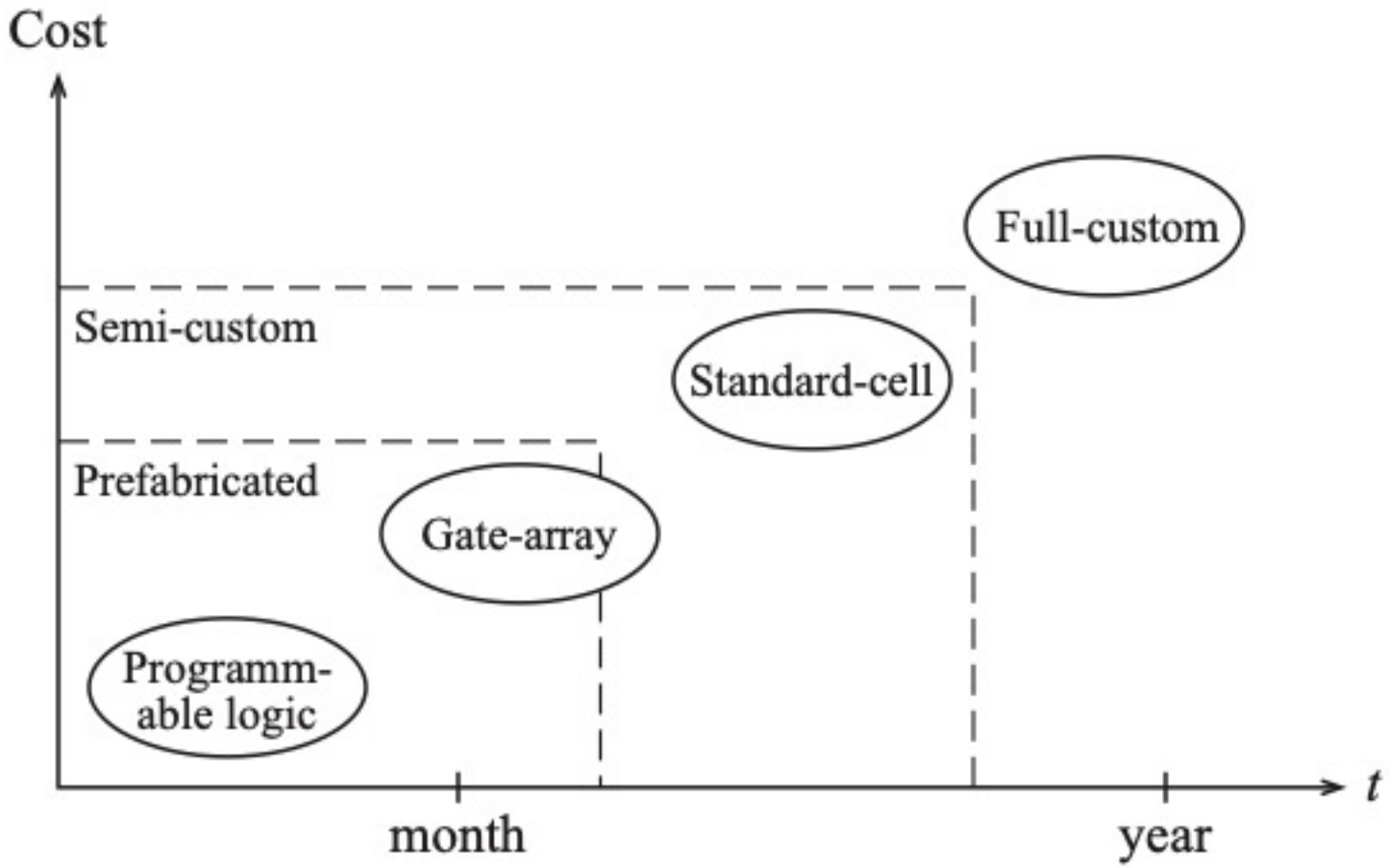
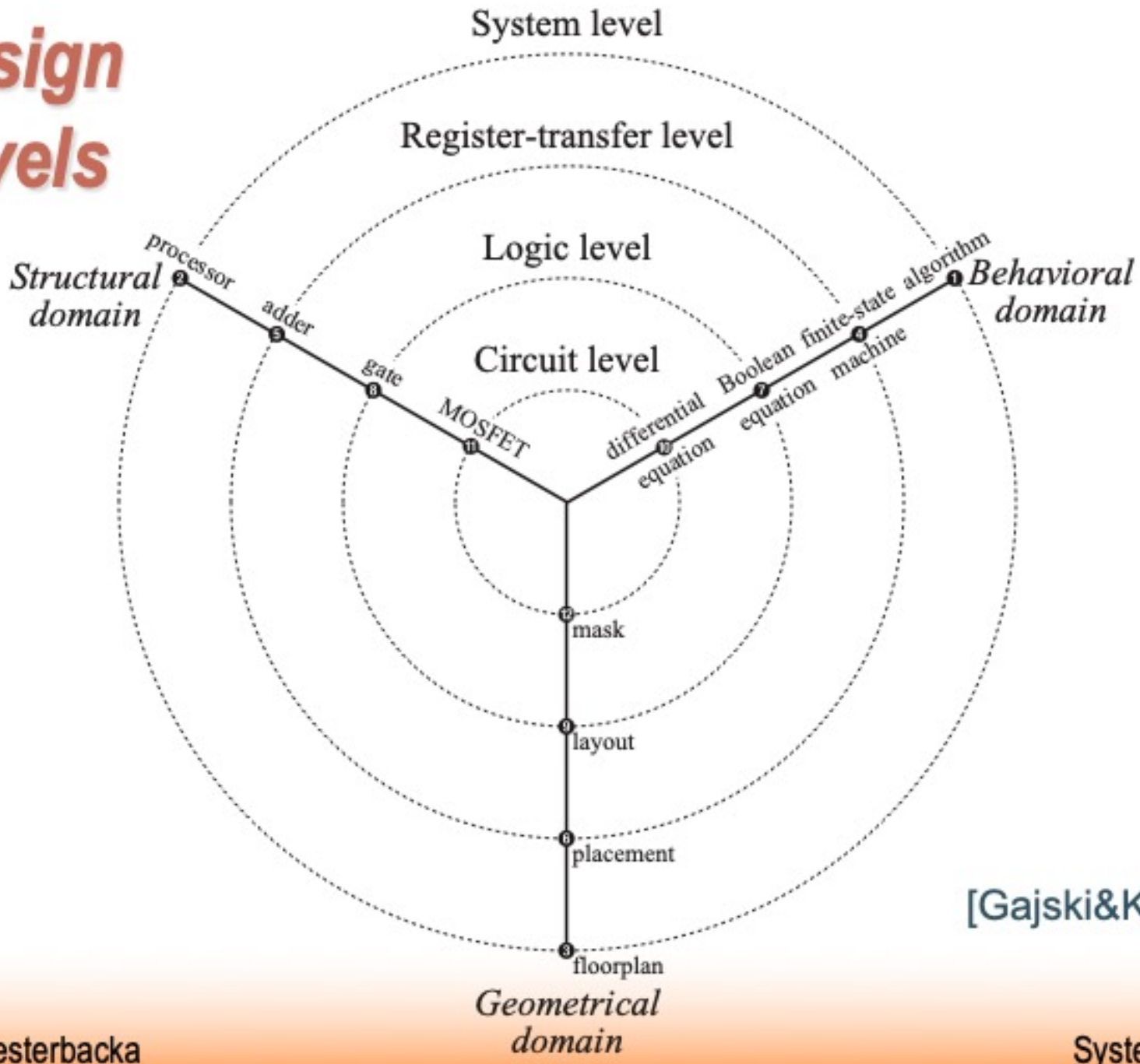
Implementation Approach

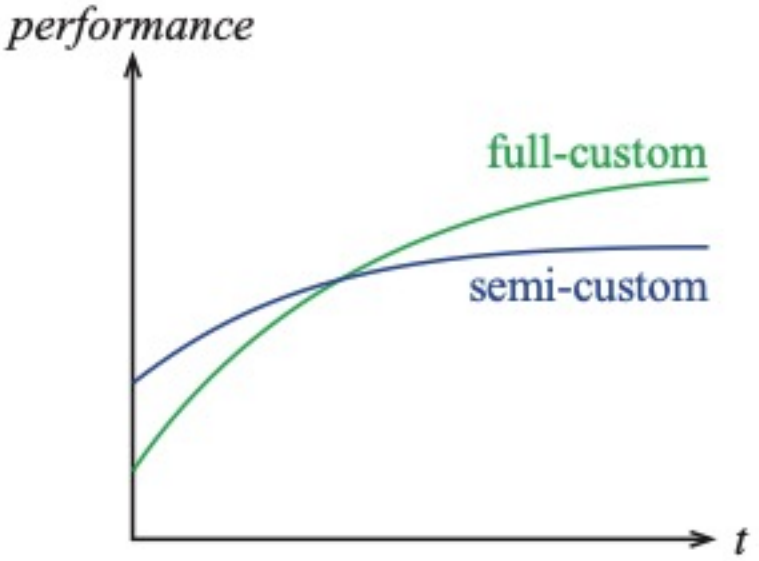


Design Levels

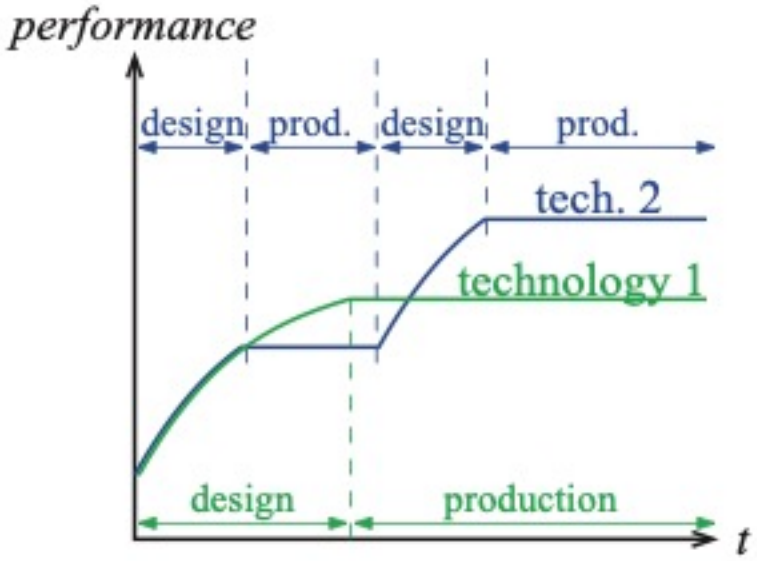


[Gajski&Kuhn'83]

Circuit Development

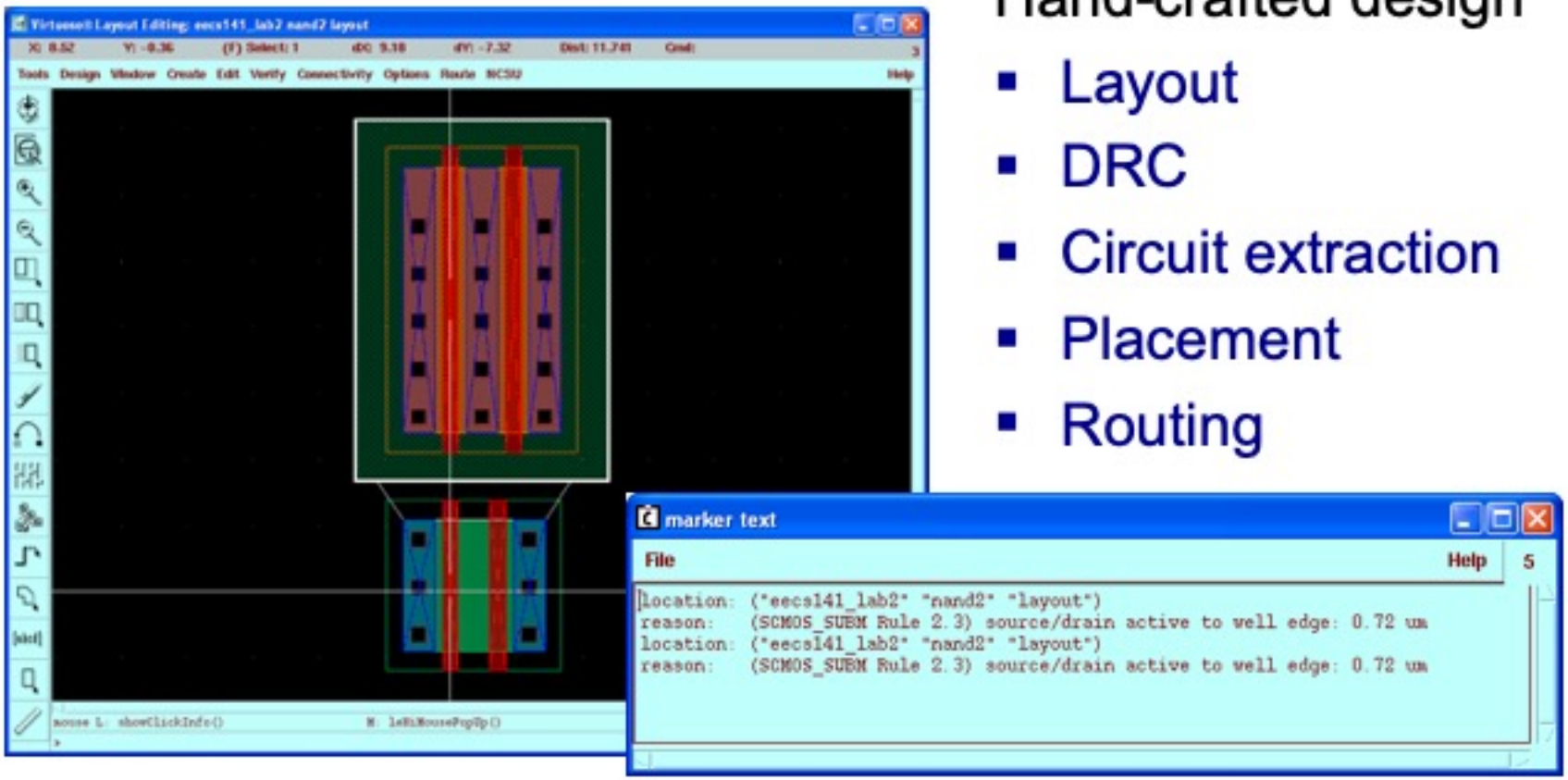


Design approach



Technology use

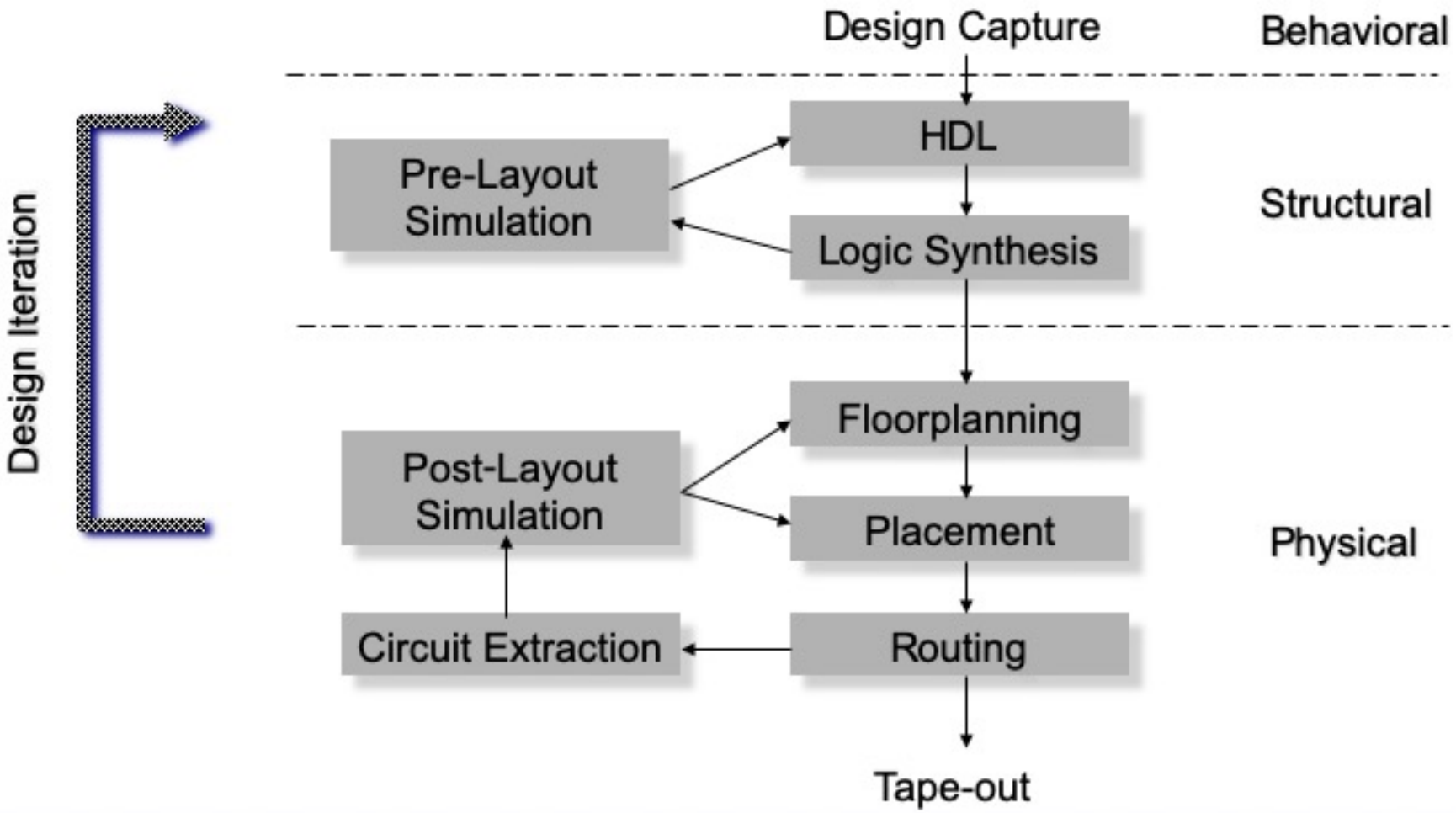
Full-Custom Design



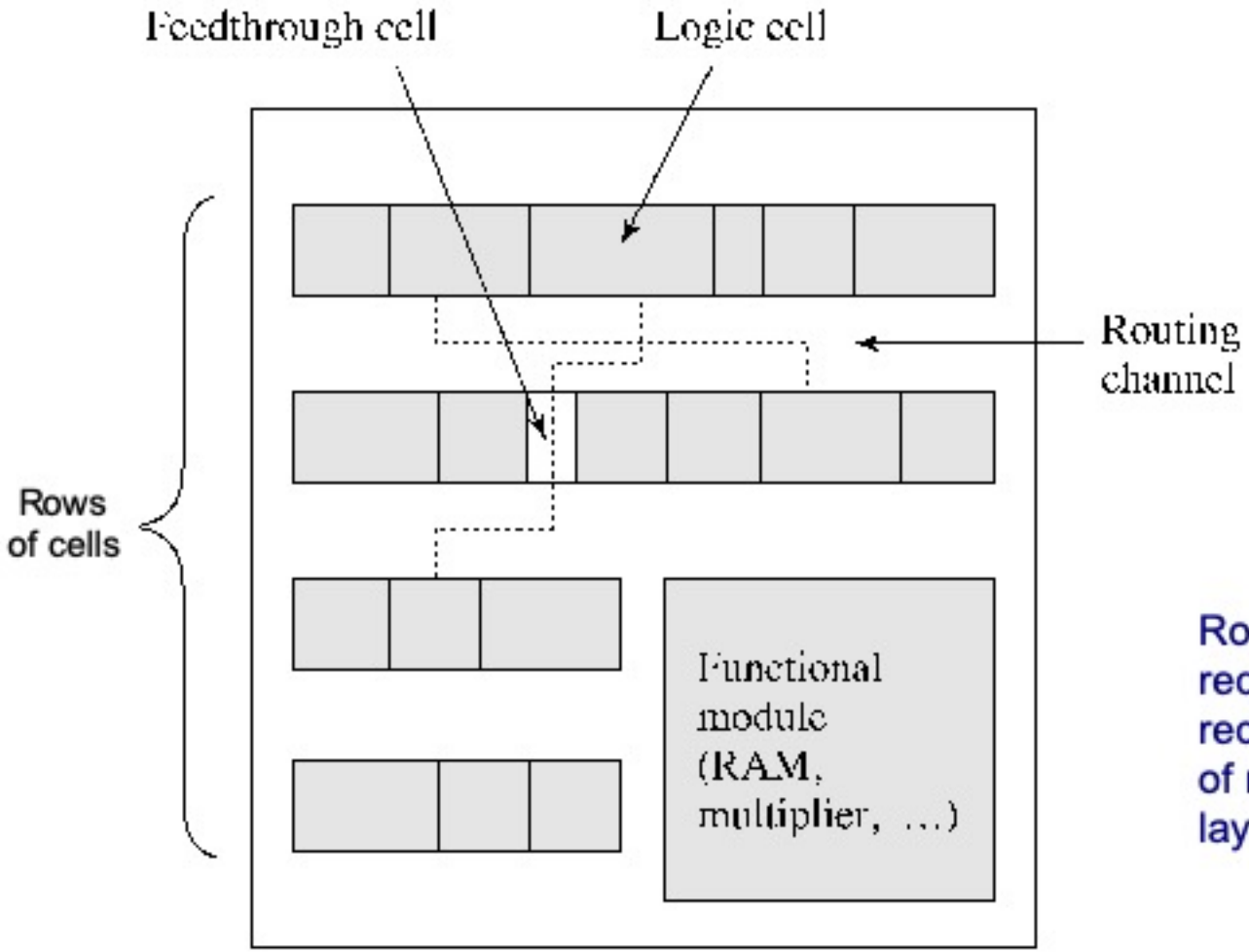
Hand-crafted design

- Layout
- DRC
- Circuit extraction
- Placement
- Routing

Semi-Custom Design Flow

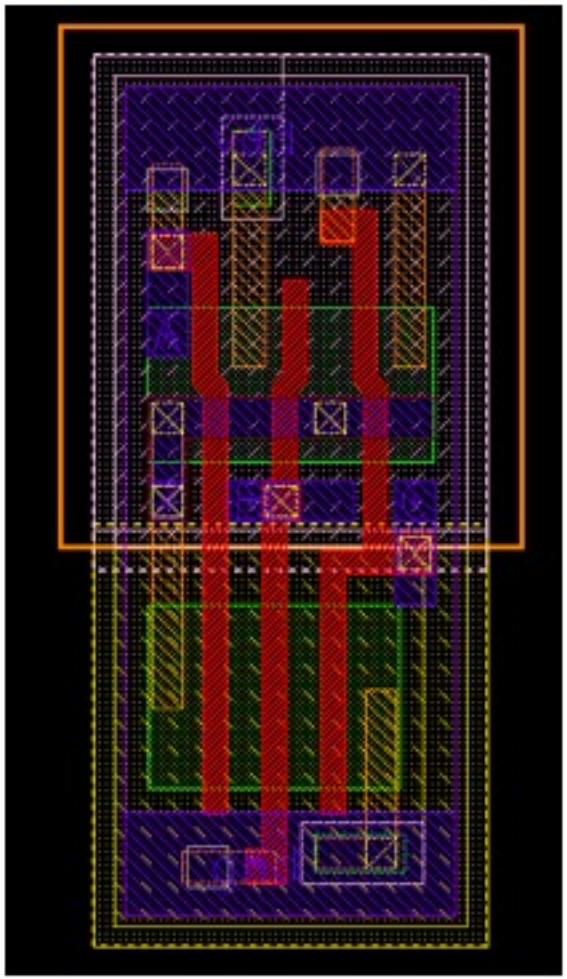


Standard Cells



Routing channel requirements are reduced by presence of more interconnect layers

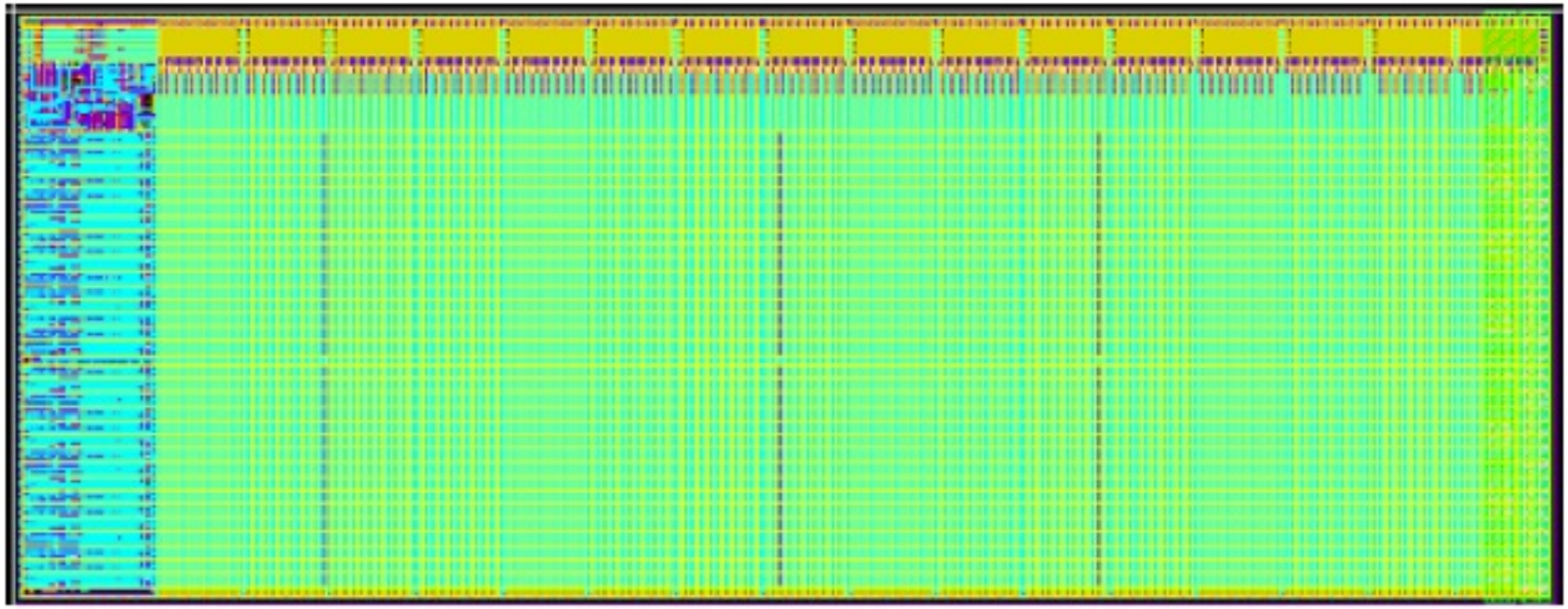
Standard Cell



Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

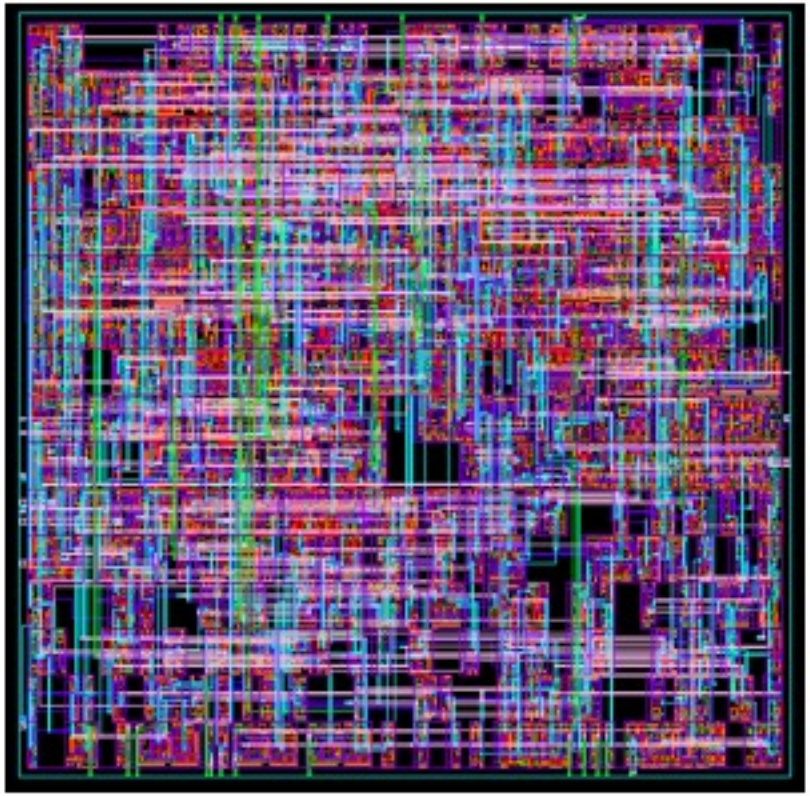
3-input NAND cell
(from ST Microelectronics):
C = Load capacitance
T = input rise/fall time

MacroModules

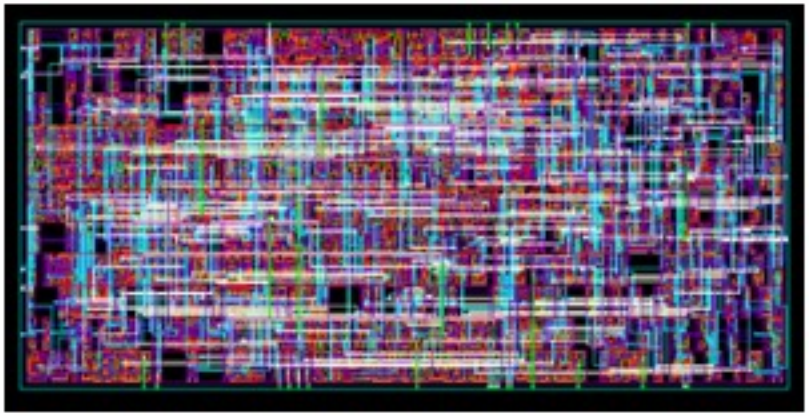


256×32 (or 8192 bit) SRAM
Generated by hard-macro module generator

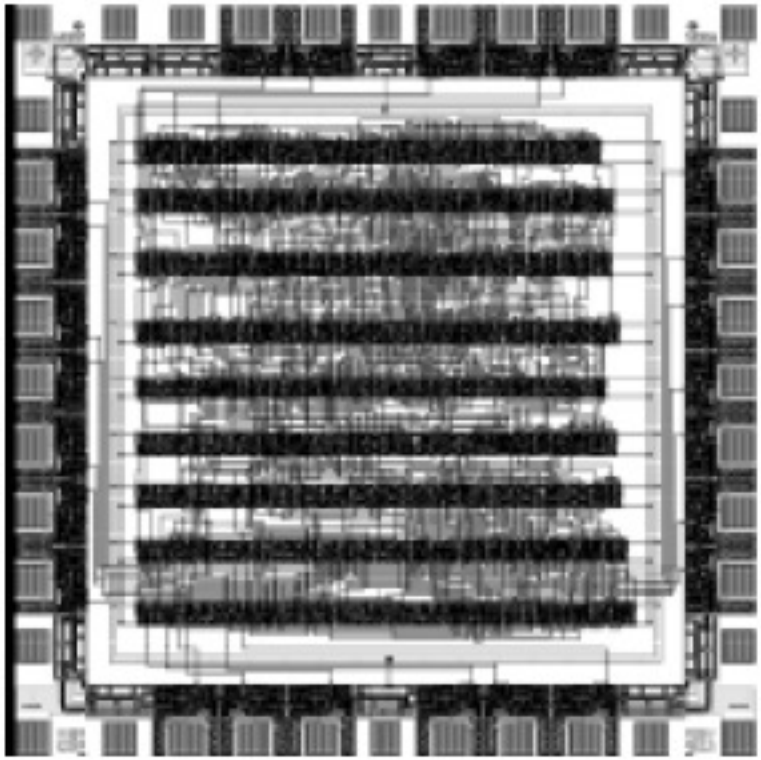
Soft MacroModules



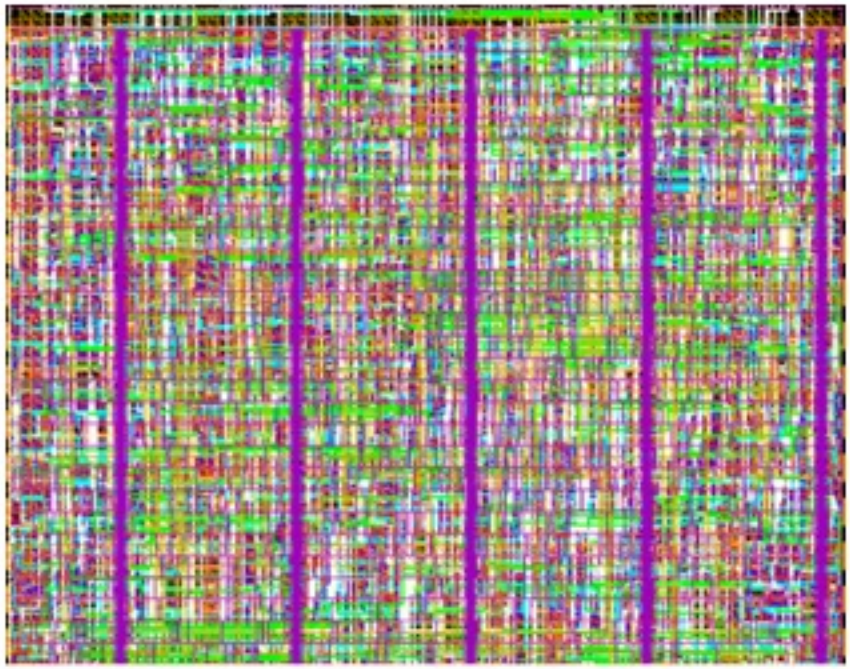
```
string mat = "booth";
directive (multtype = mat);
output signed [16] Z = A * B;
```



Standard Cells Wire Routing

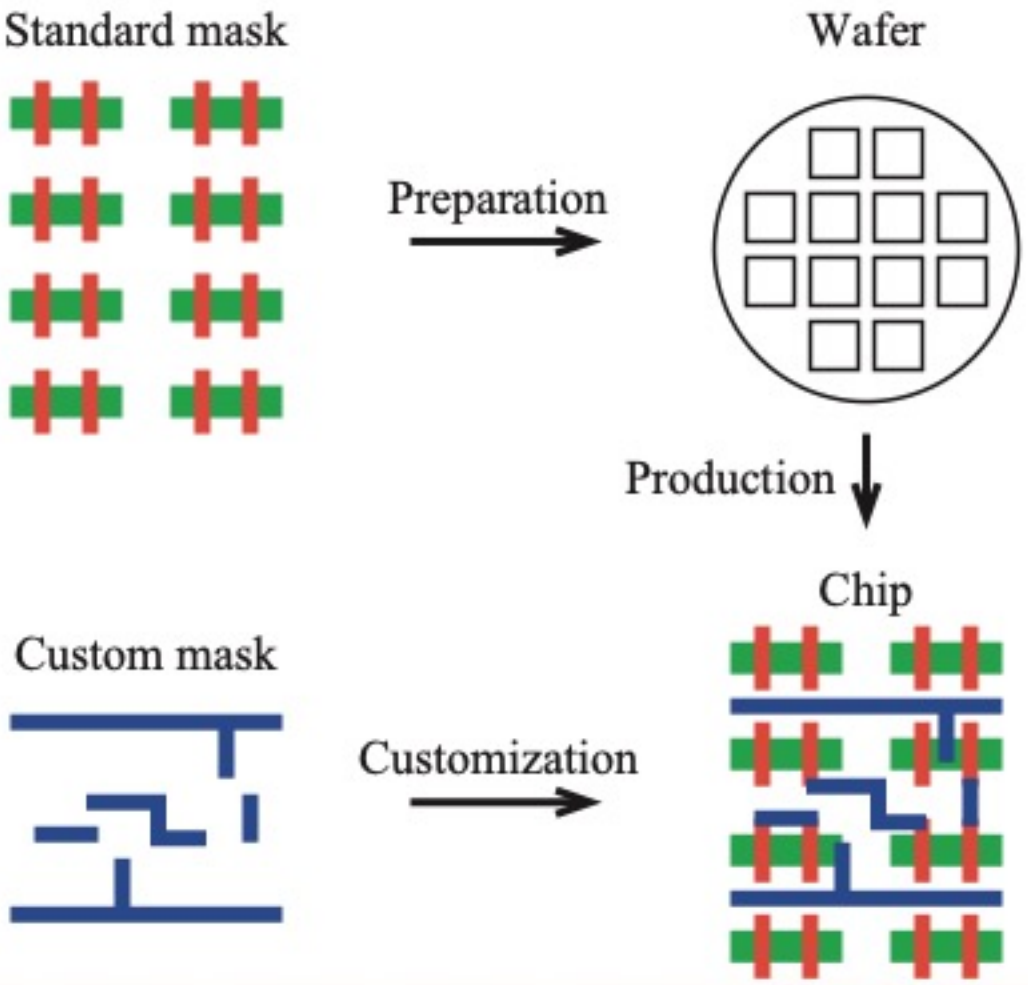


Few metal layers

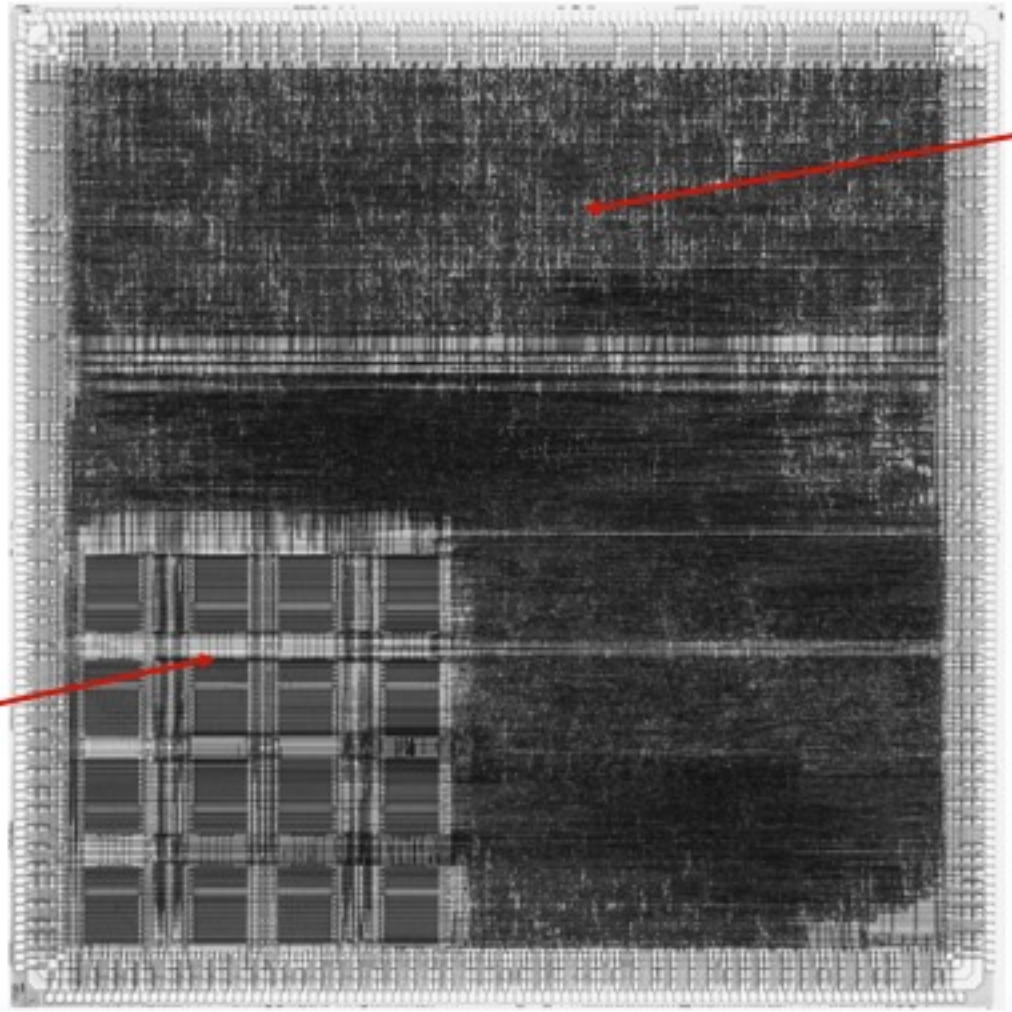


Many metal layers

Sea-of-Gates

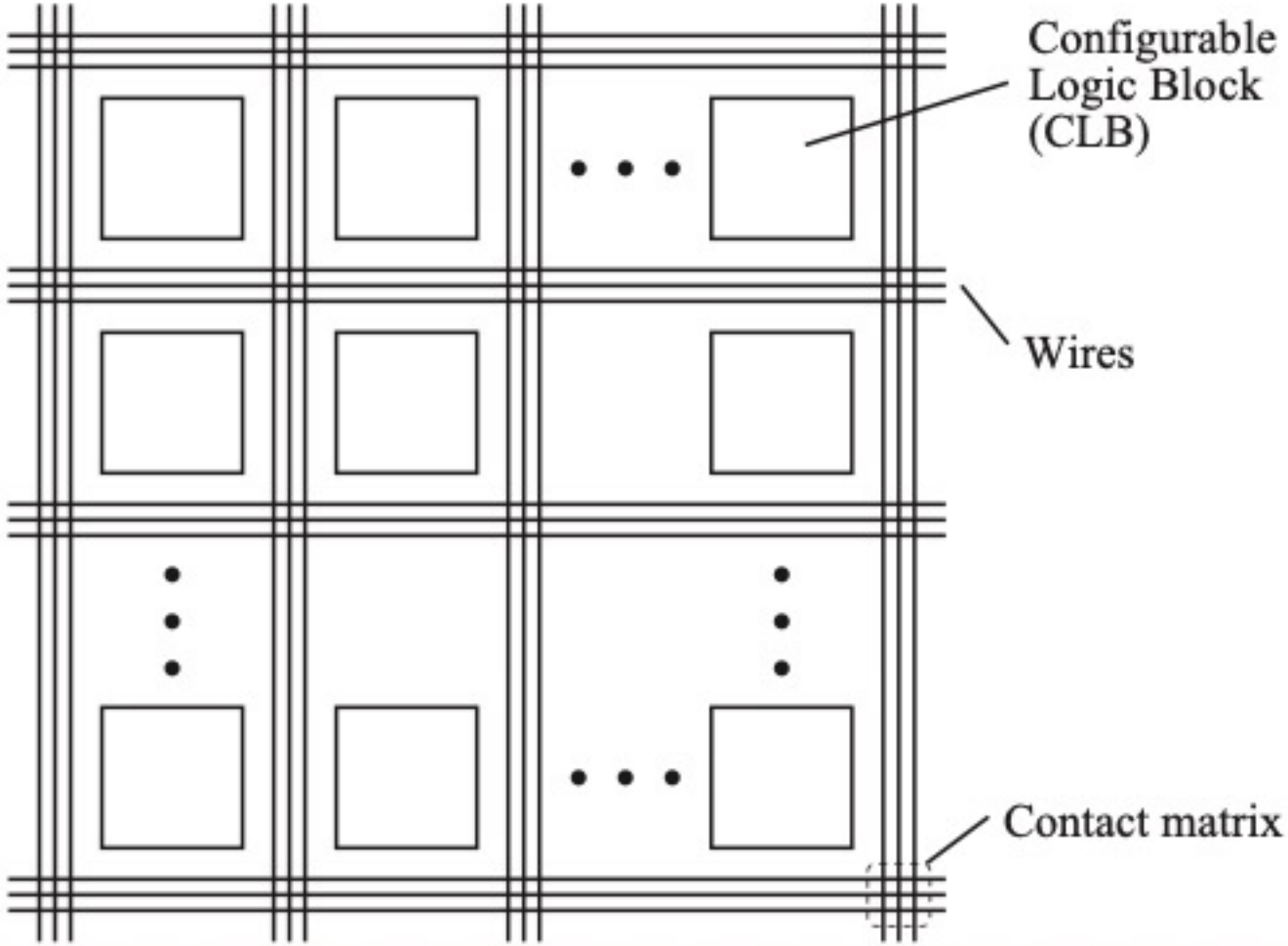

Standard mask
Wafer
Preparation
Production
Chip
Custom mask
Customization

Sea-of-Gates Chip



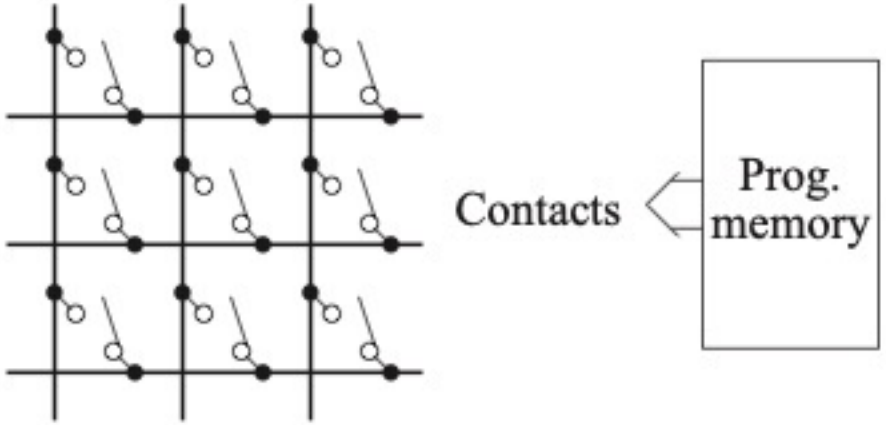
LSI Logic LEA300K
(0.6 μm CMOS)

FPGA Architecture

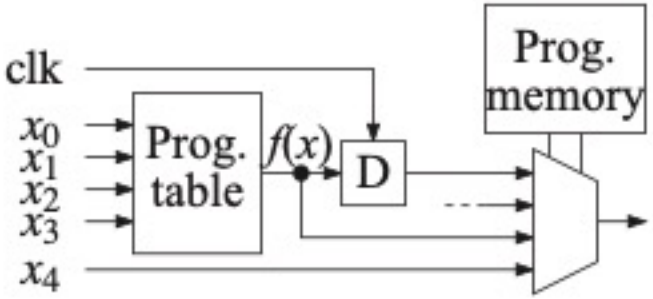


FPGA Programming

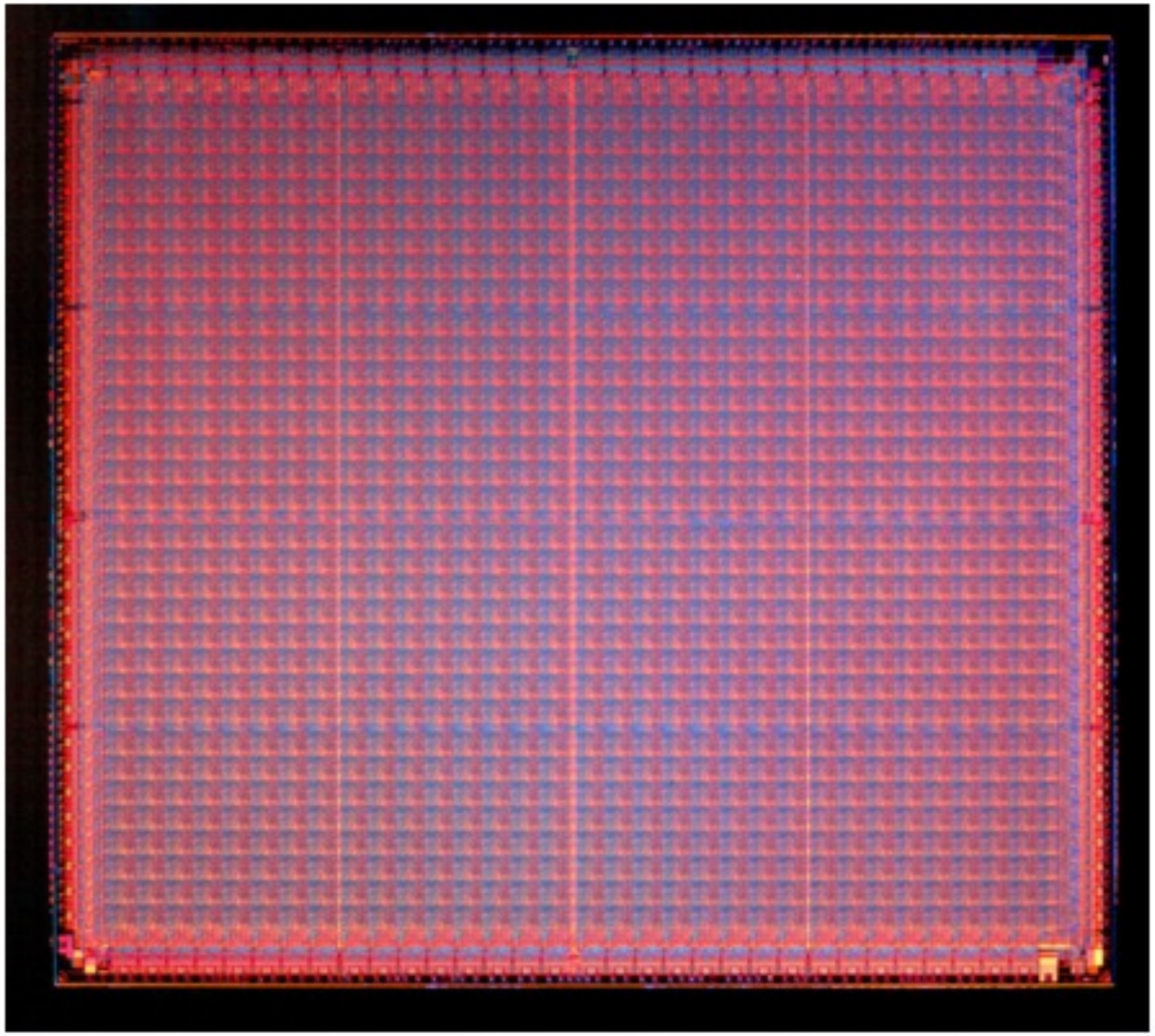
Interconnect



Functions
(CLB)



FPGA Chip



Faults

Physical defects

- Defects in substrate
- Litographic defects
- Mask contamination and scratches
- Process variations
- Oxide defects

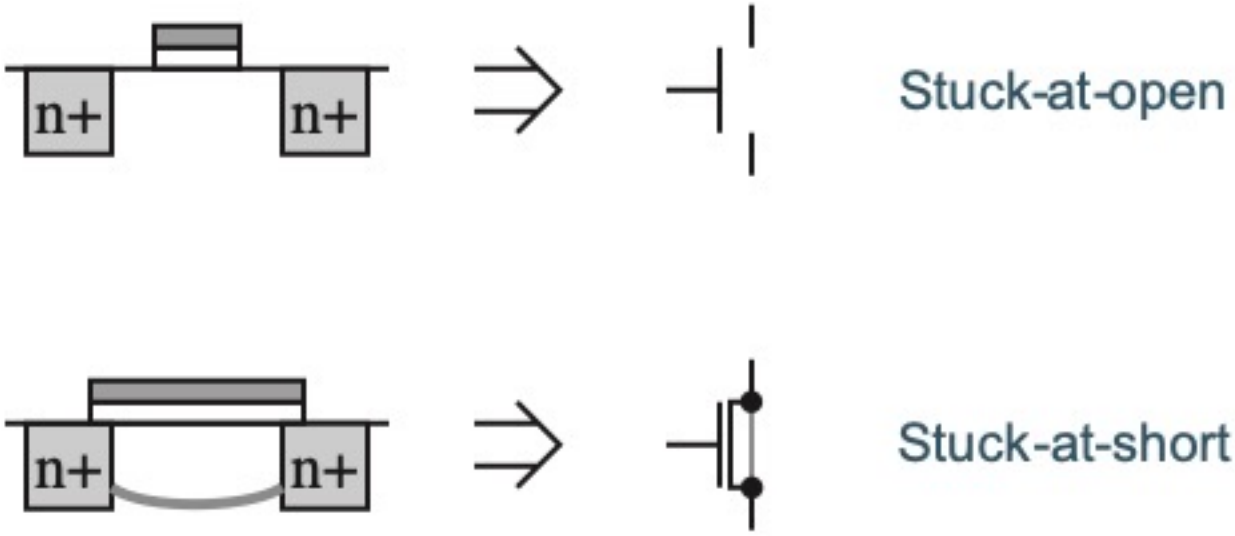
Electrical faults

- Shorts/opens
- Resistive shorts/opens
- Transistor stuck-on/off
- Error in threshold voltage
- Excessive current draw

Logical faults

- Logical stuck-at-0, stuck-at-1
- Delay fault
- AND/OR-bridging

MOSFET Defects



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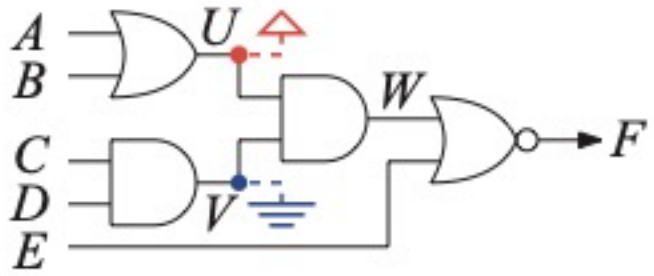
Simple Stuck-At Model

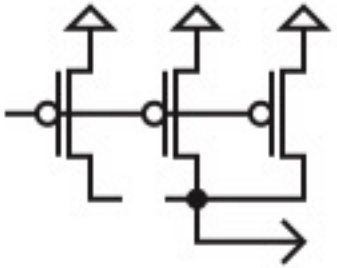
- Example: simple logic network



- *Stuck-at-one* fault: short-circuit from *U* to VDD
  - Test with pattern $A = B = 0$, $C = D = 1$, $E = 0$
- *Stuck-at-zero* fault: short-circuit from *V* to GND
  - Test with pattern $A = 1$ or $B = 1$, $C = D = 1$, $E = 0$

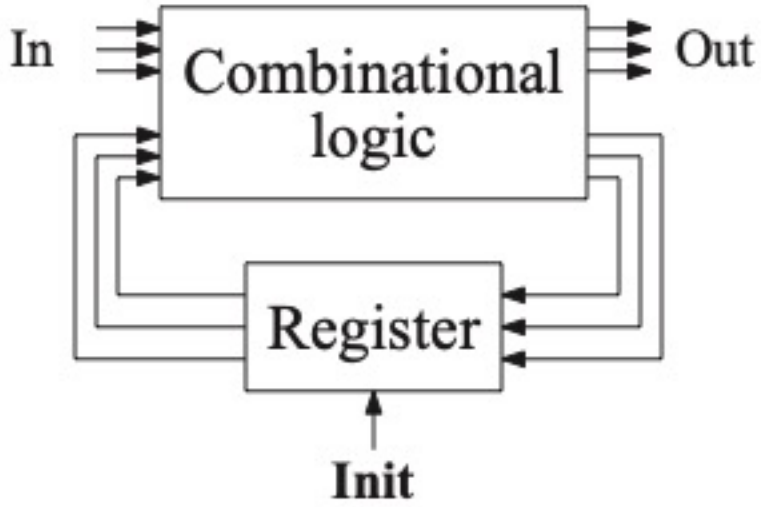
Delay Fault

- Delay faults require full-speed tests



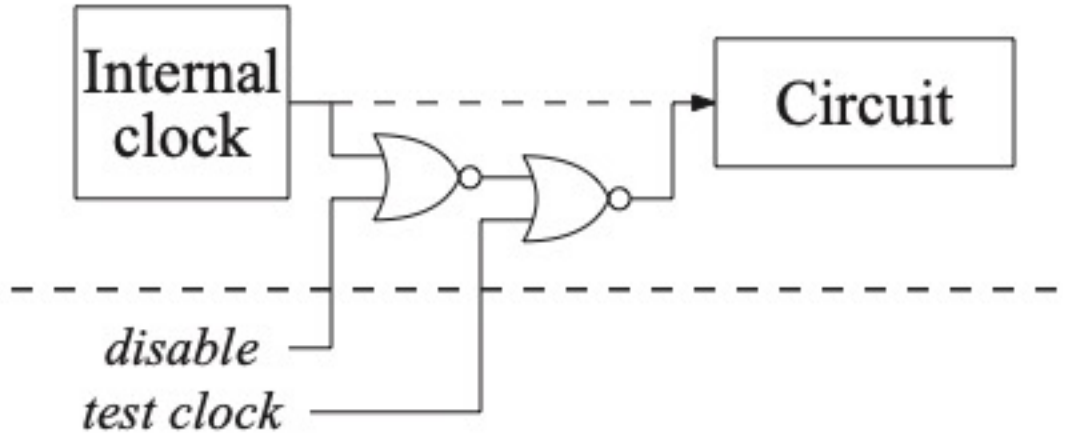
- Example on causes
  - Poor estimation of delay and timing
  - Abnormal process variations (e.g. V_T)
  - Opens in parallel connected transistors
  - Aging effects (e.g. hot-carrier, electromigration)

Setting Test State



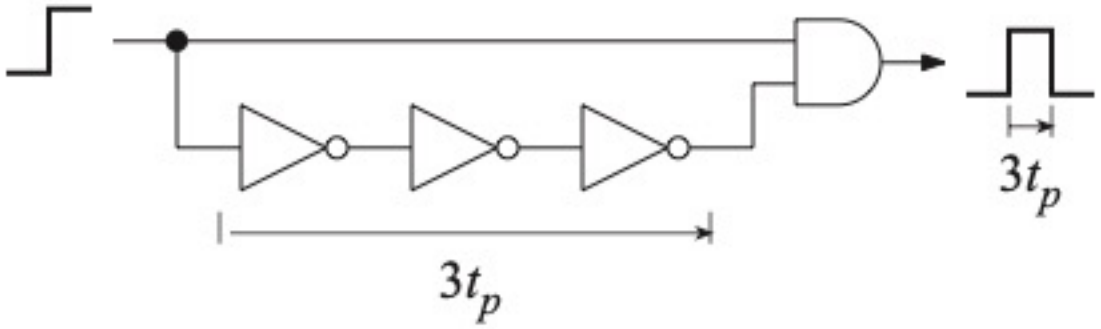
Design the register such that it can be initiated to a known state

Test Clock



Design the clocking so it can be tested with special clocks

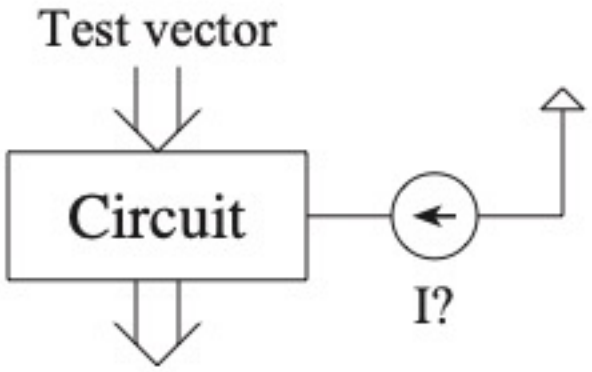
Asynchronous Logic



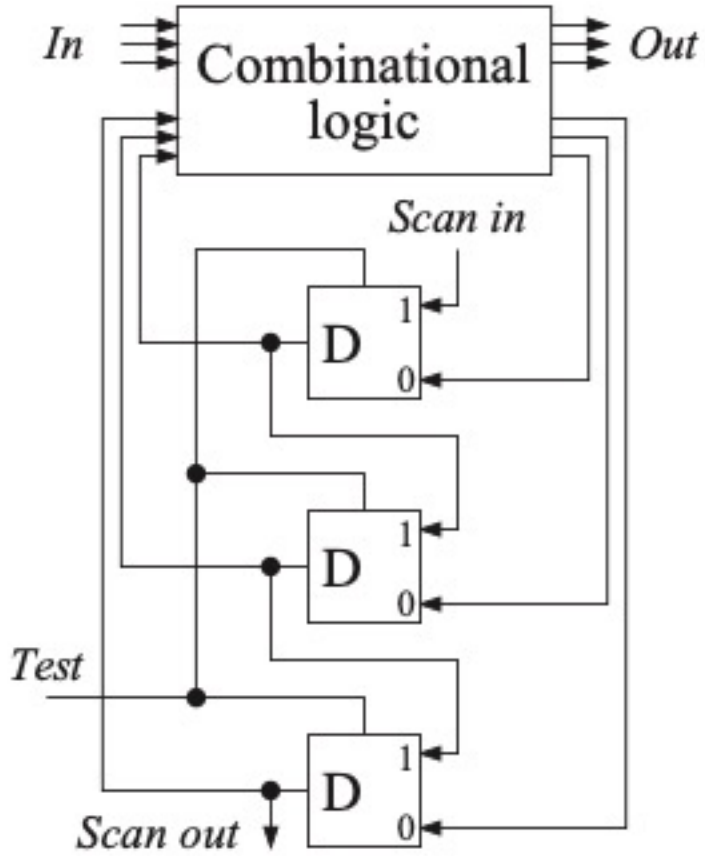
More difficult to test than synchronous solutions

IDDQ Test

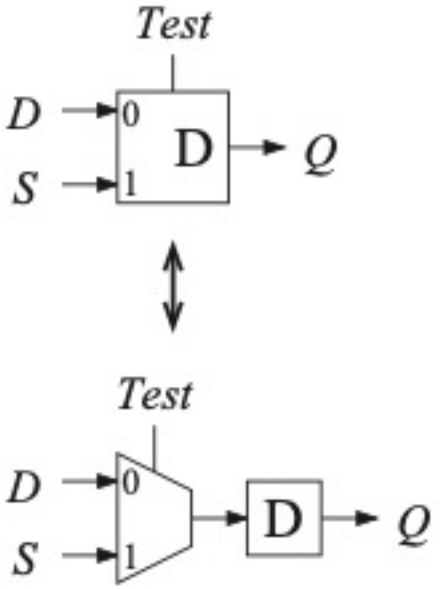
- Discovers fabrication faults and some defects that are difficult to detect
  - Gate oxide short
  - Channel punch-through
  - Diode leakage
  - Transmission gate defects



Scan Techniques

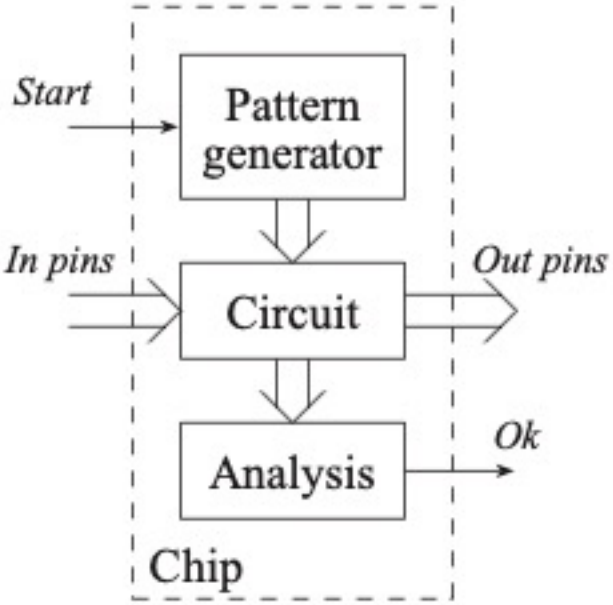


Scan chain

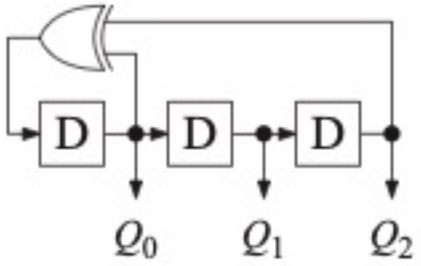


Scan flip-flop

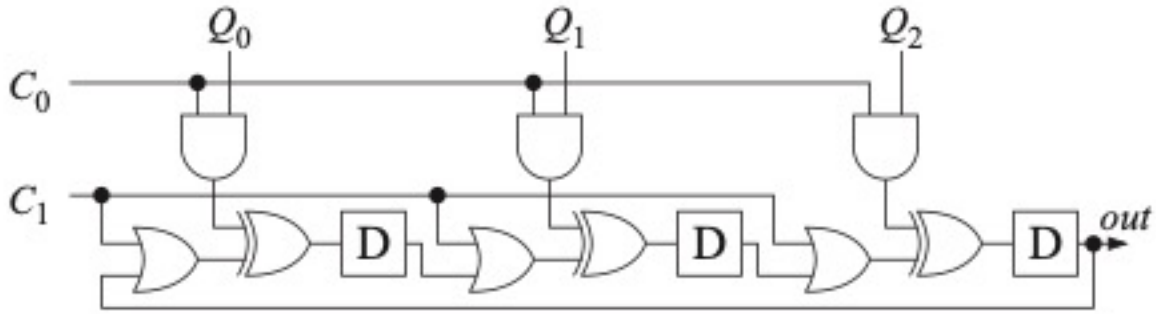
Built-In Self Test (BIST)



BIST



PRBS



Observer circuit