Digital ICs — Lectures

1) **Introduction** [Ch. 1]	*TSEI03/TSTE86*
2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
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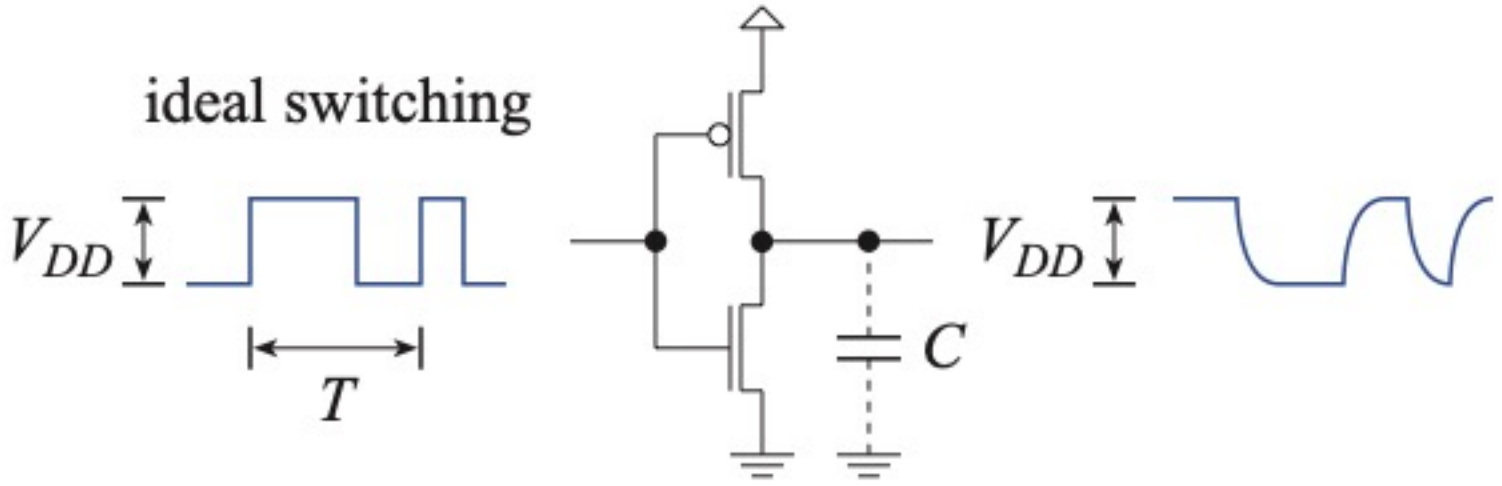
6) **Sequential circuits** [Ch. 7]	*TSEI03/TSTE86*
7) **Synchronization** [Ch. 10]	*TSTE86*
8) **Adders** [Ch. 11]	*TSEI03/TSTE86*
9) **Multipliers** [Ch. 11]	*TSTE86*
10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
11) **Manufacturing** [Ch. 2]	*TSTE86*
12) **System design** [Ch. 8]	*TSTE86*

Switch Activity

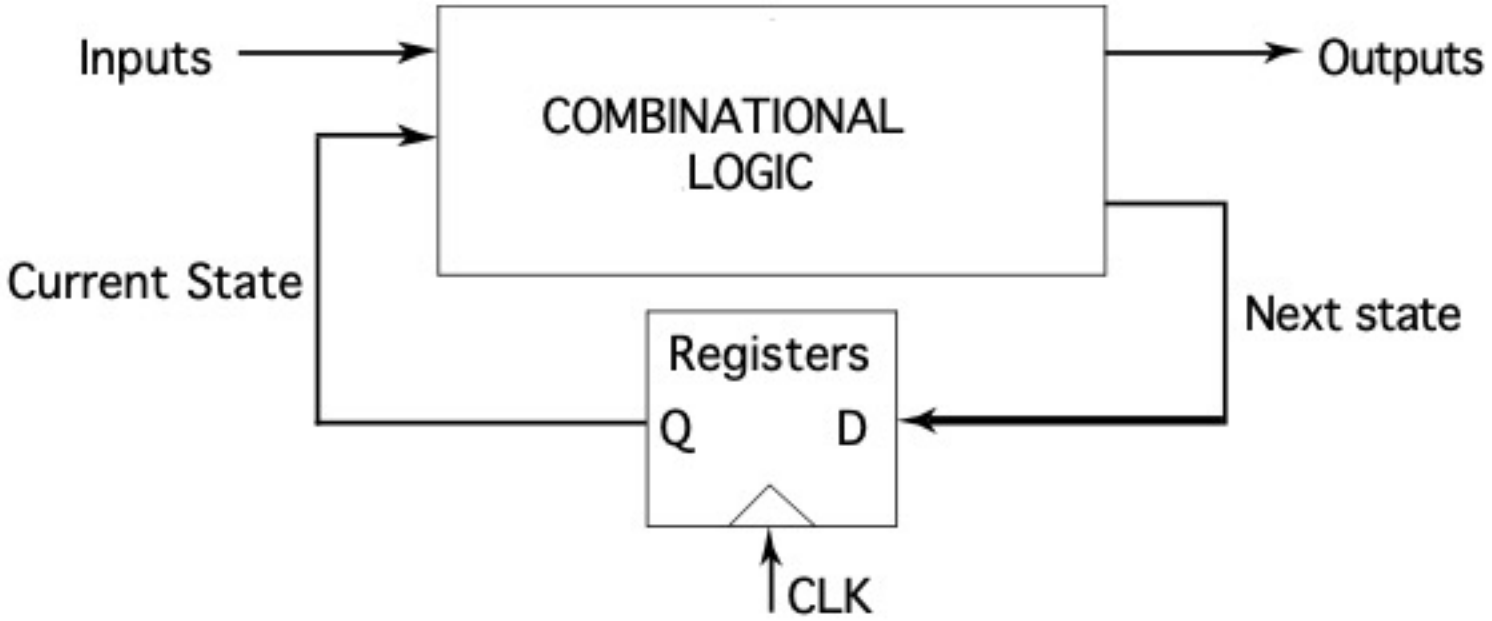


Dynamic power dissipation is

$$P_d = I_{av} V_{DD} = \frac{Q_C}{T} V_{DD} = fCV_{DD} \cdot V_{DD} = af_{clk} CV_{DD}^2$$

where a is the switch activity

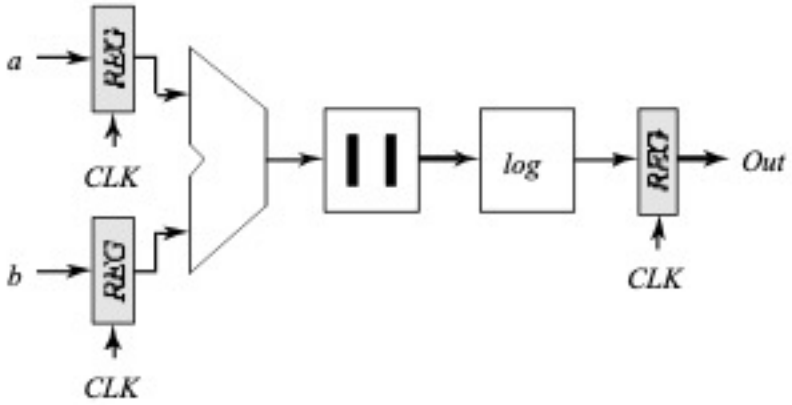
Sequential Logic

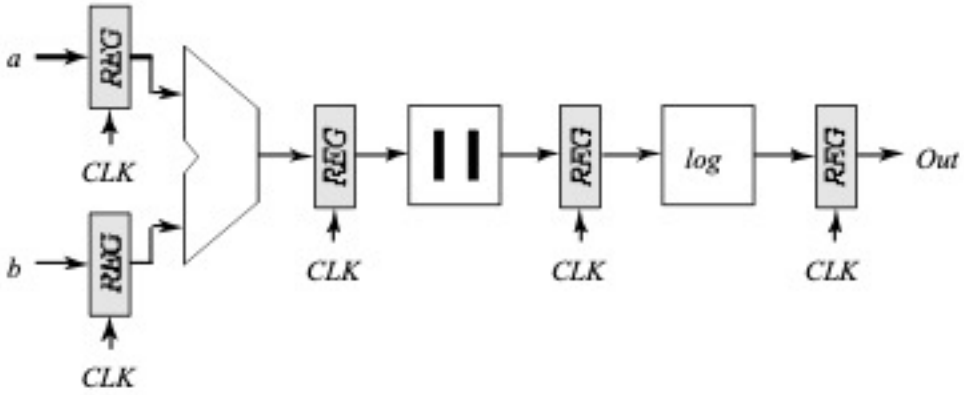


2 storage mechanisms

- positive feedback
- charge-based

Pipelining



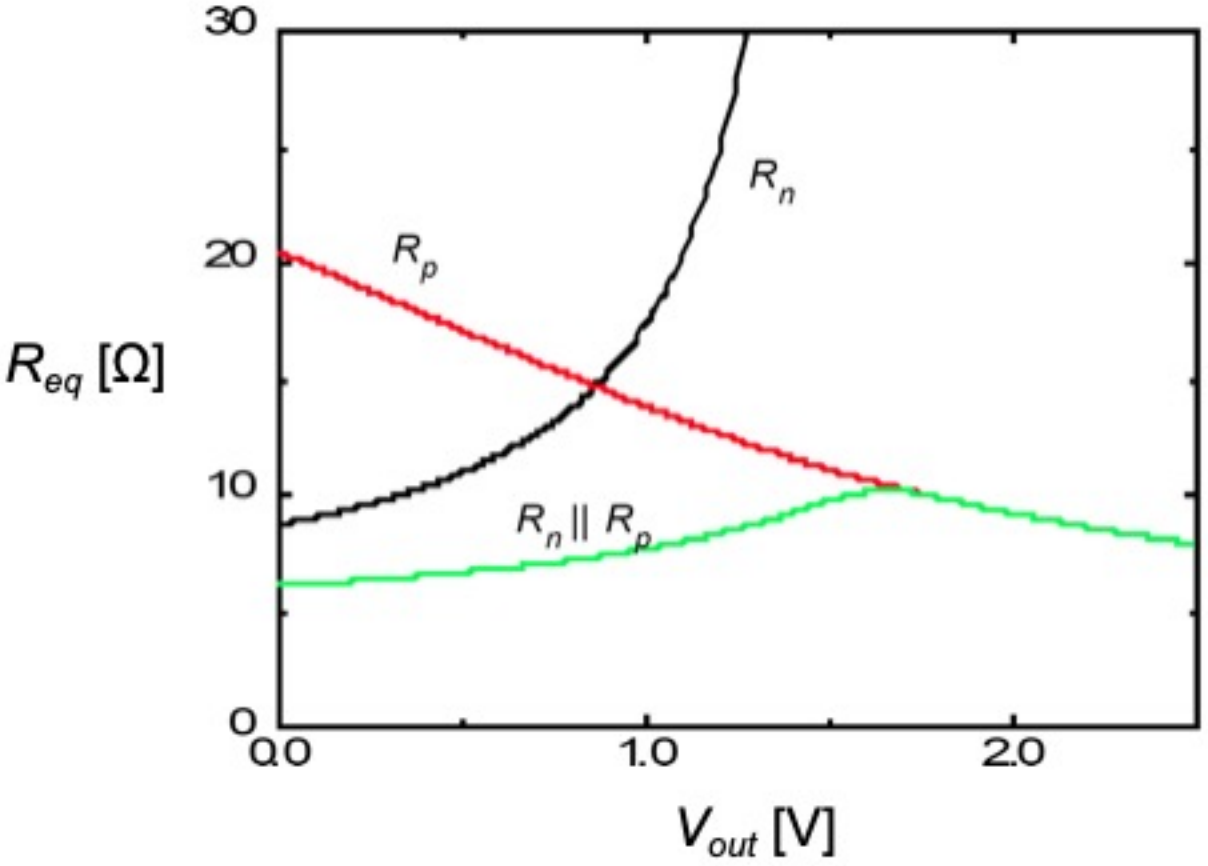


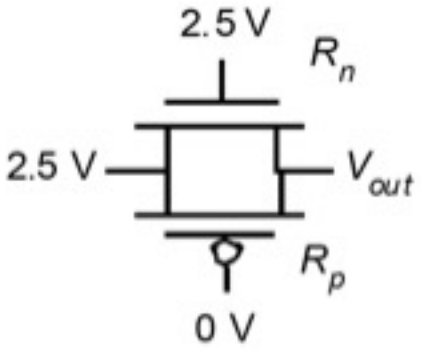
Reference

Pipelined

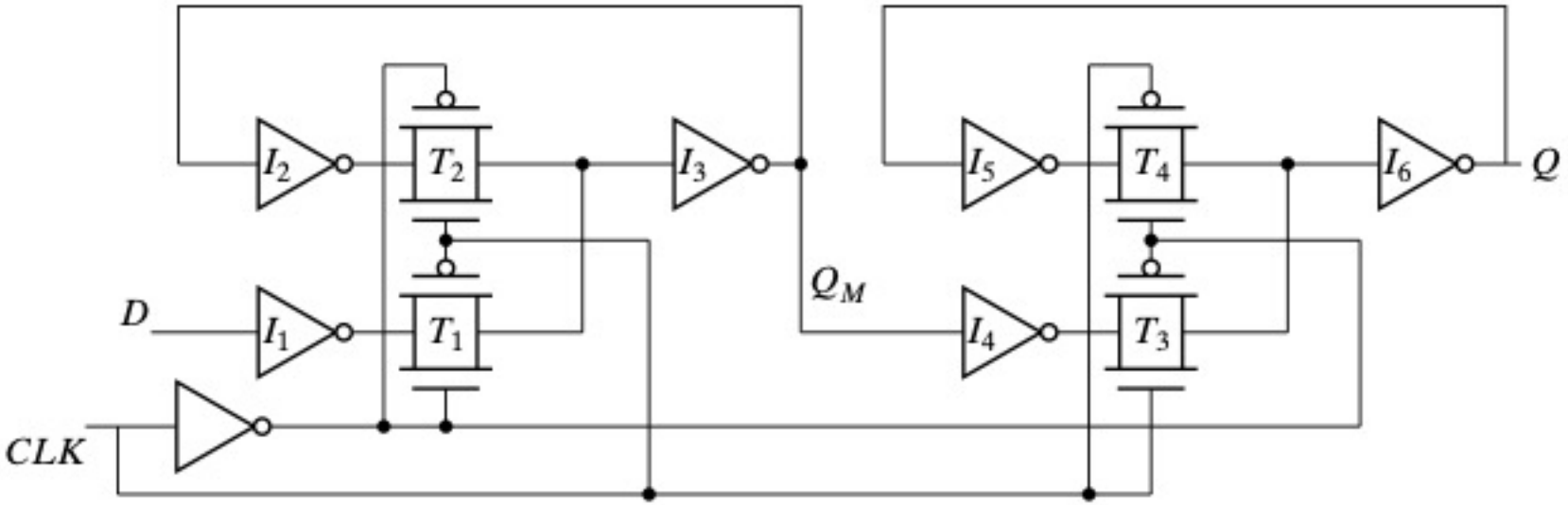
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\|a_1 + b_1\|$	
3	$a_3 + b_3$	$\|a_2 + b_2\|$	$\log(\|a_1 + b_1\|)$
4	$a_4 + b_4$	$\|a_3 + b_3\|$	$\log(\|a_2 + b_2\|)$
5	$a_5 + b_5$	$\|a_4 + b_4\|$	$\log(\|a_3 + b_3\|)$

Transmission Gate



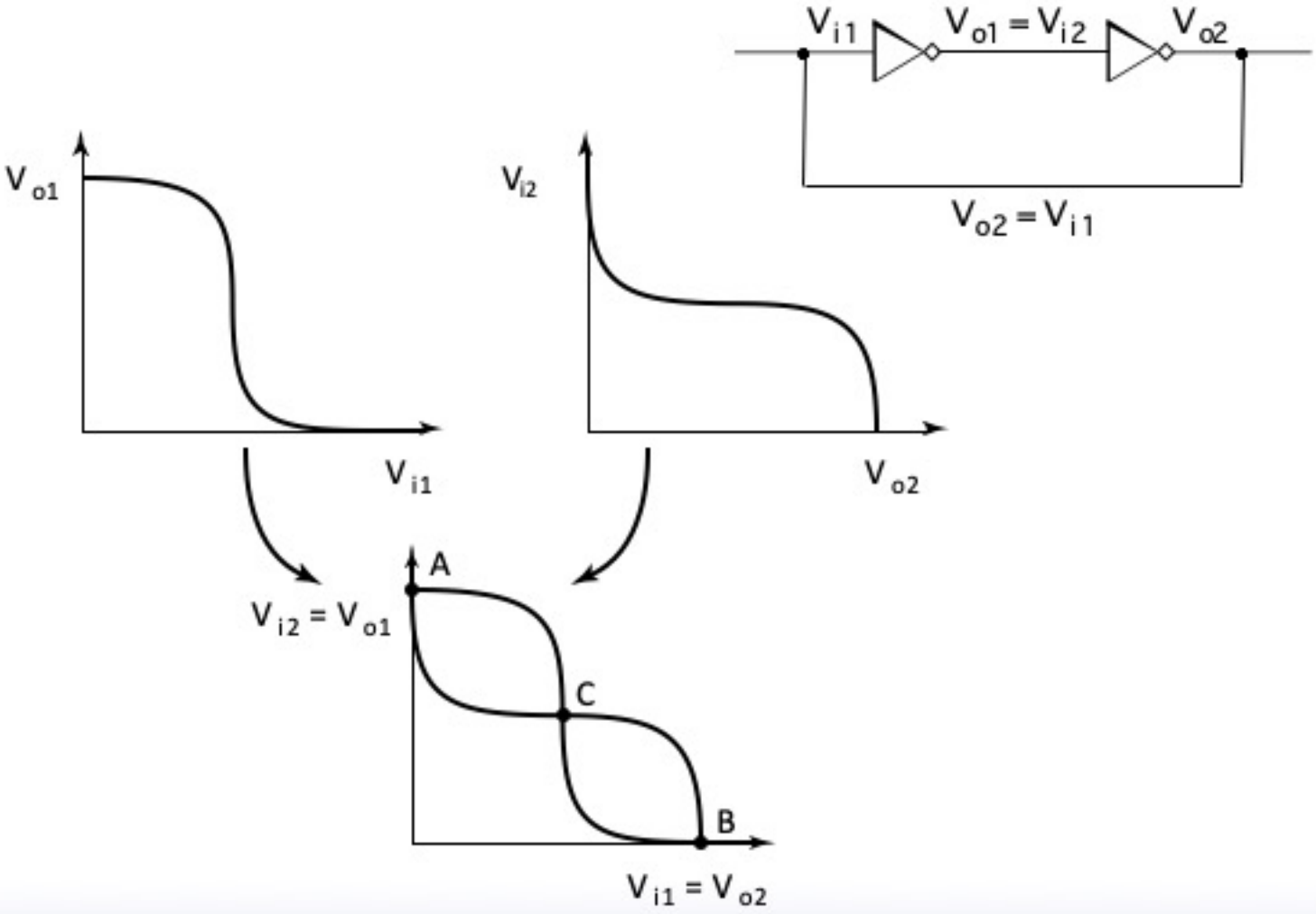


Master-Slave Register

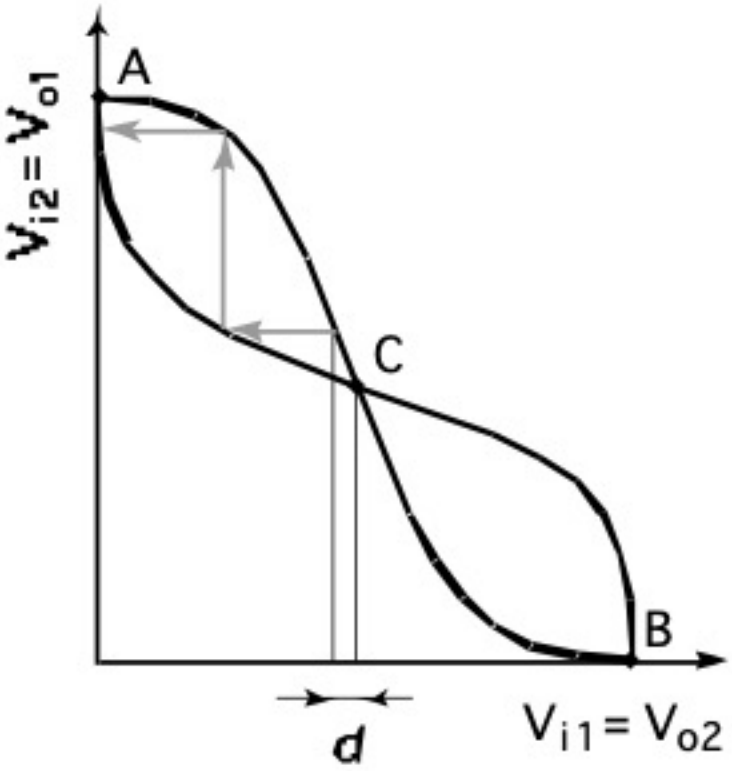


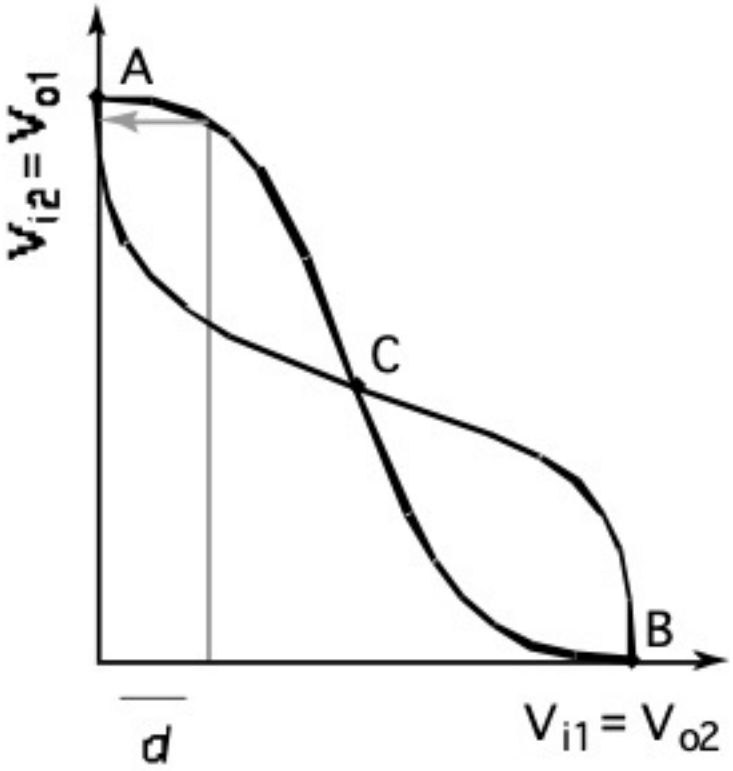
Multiplexer-based latch pair

Positive Feedback



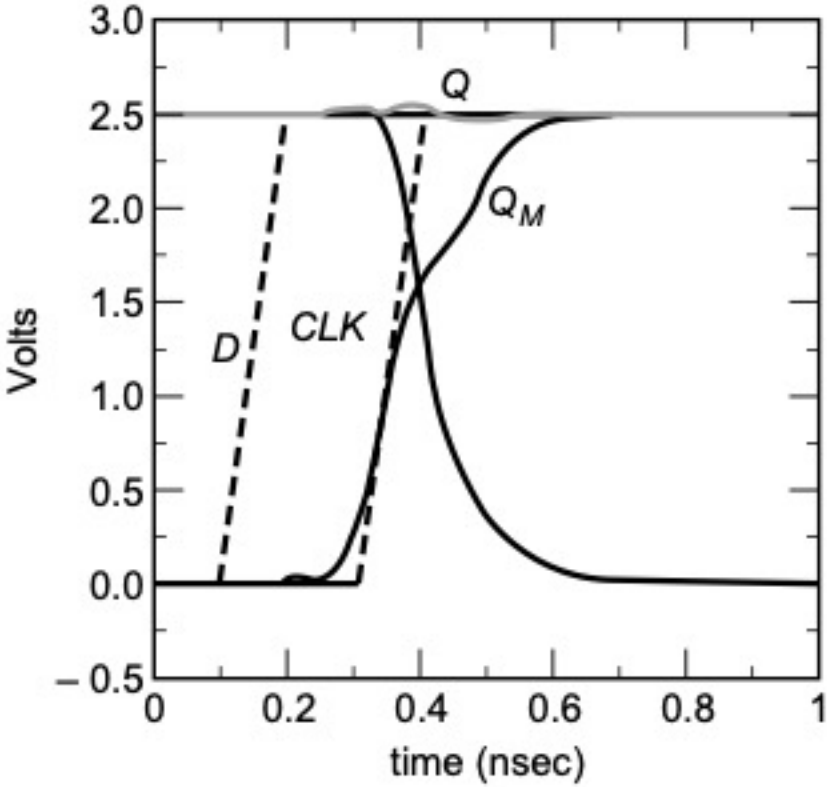
Metastability



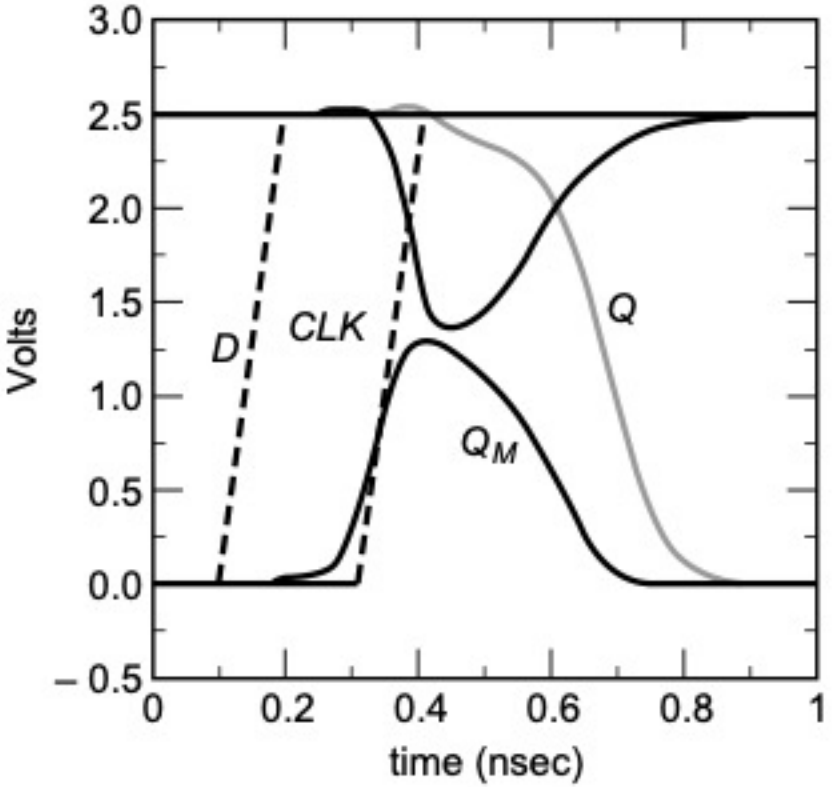


Gain is larger than 1 in the transition region

Setup Time

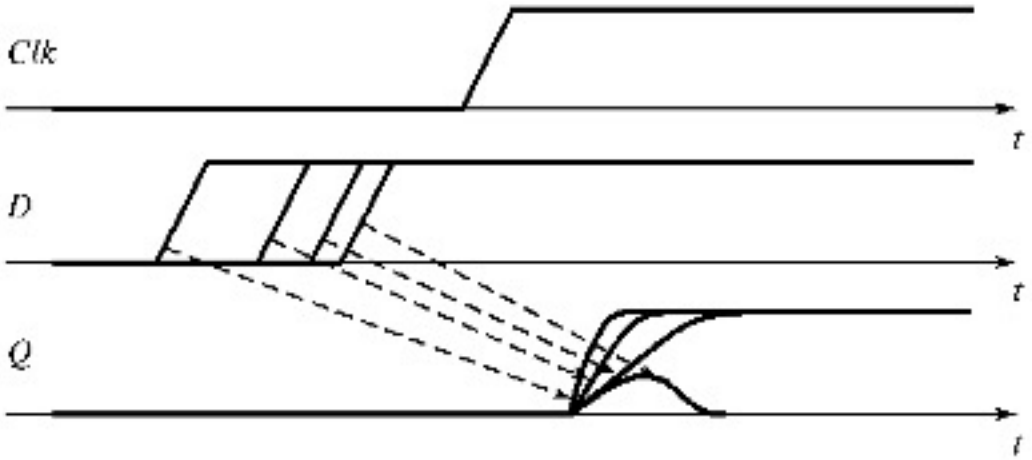


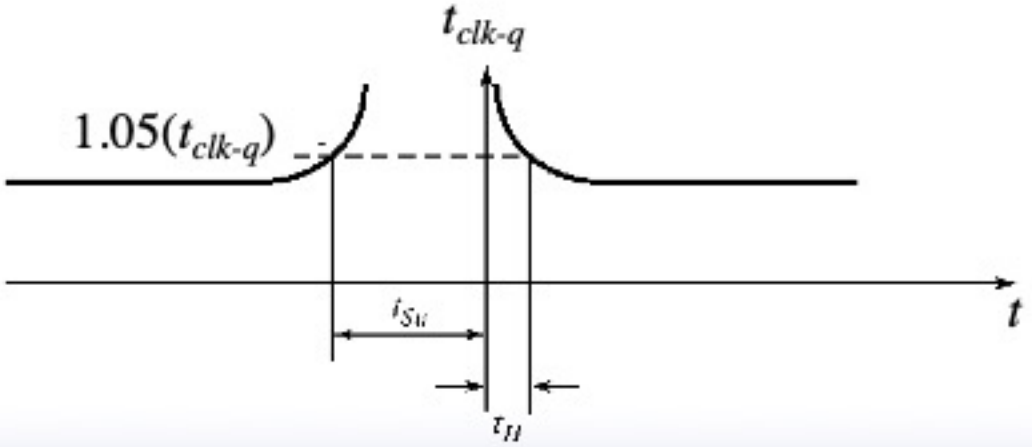
(a) $T_{D->CLK}$ = 0.21 nsec



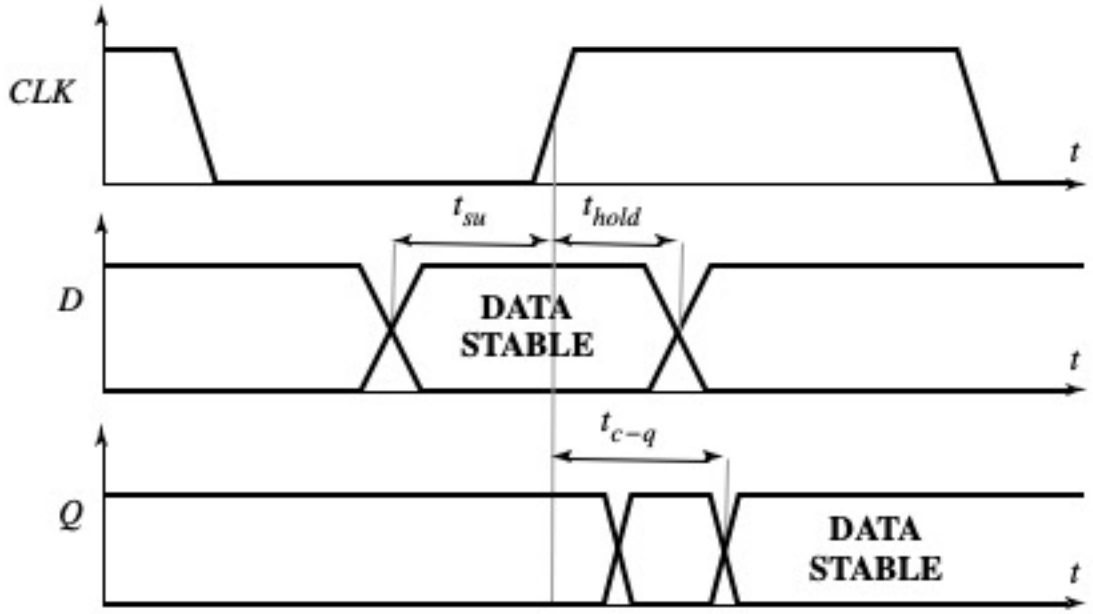
(b) $T_{D->CLK}$ = 0.20 nsec

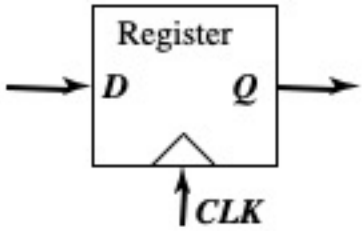
Setup and Hold Times



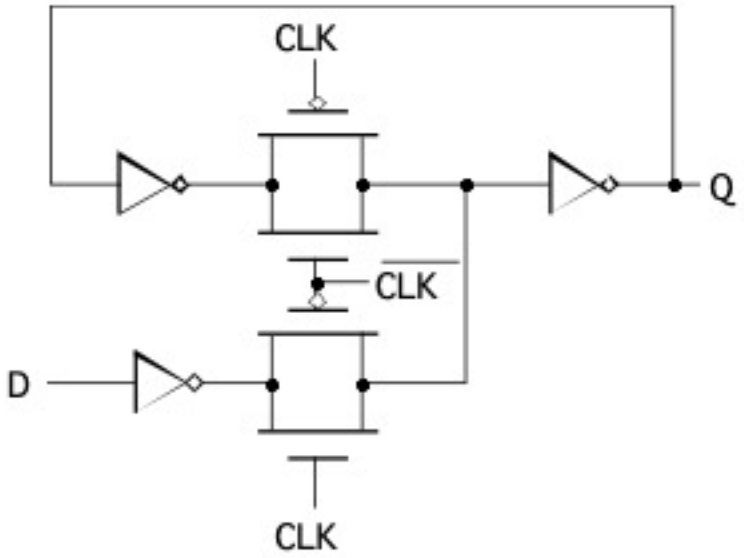


Timing Definitions

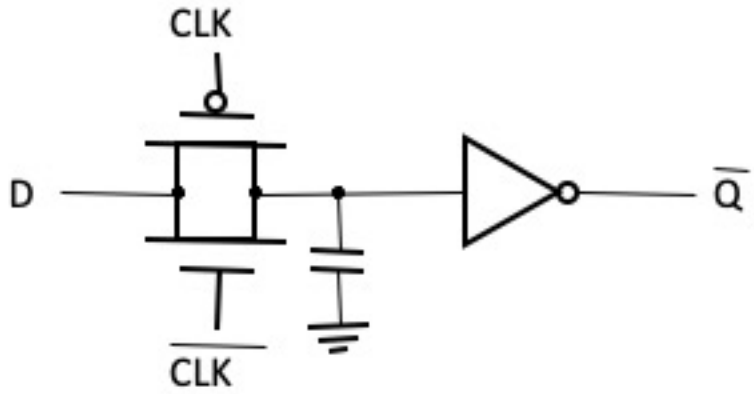




Storage Mechanisms

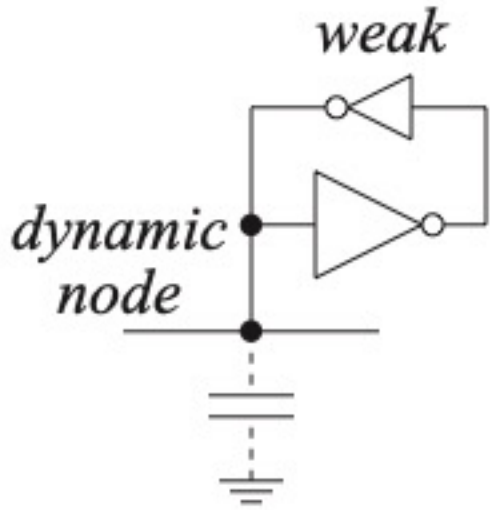


Static latch



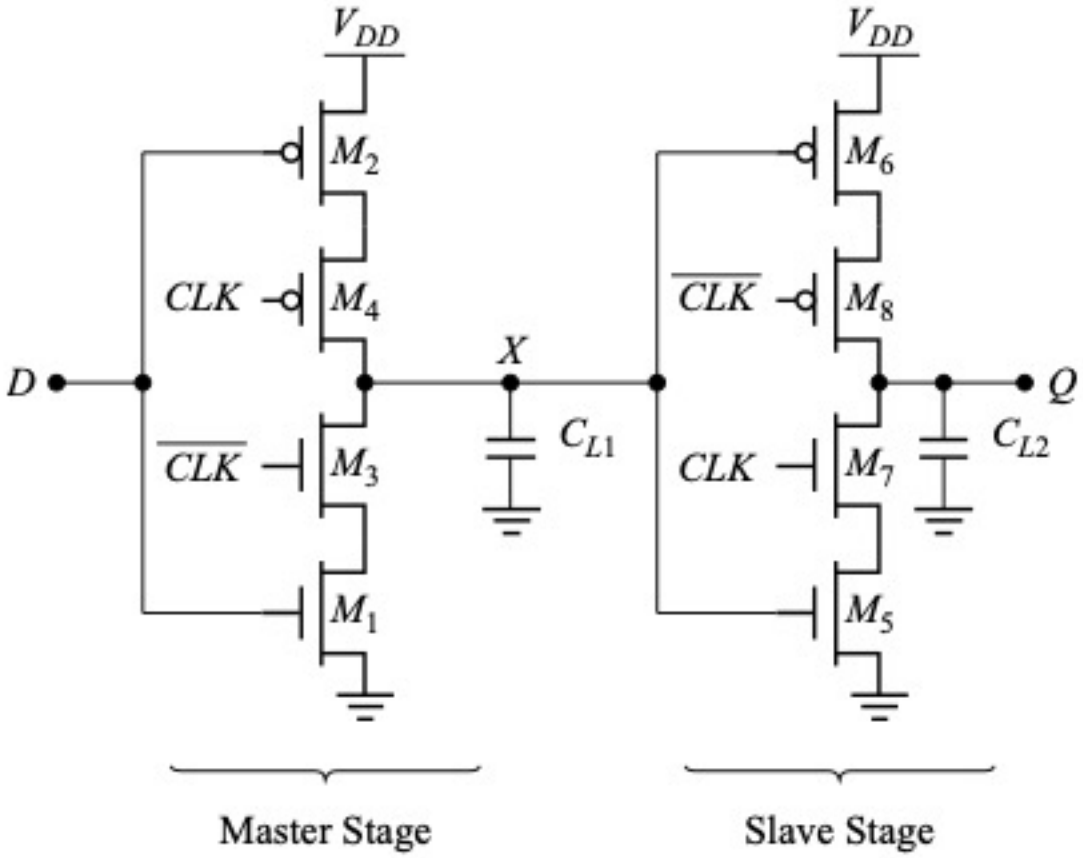
Dynamic latch

Keeper



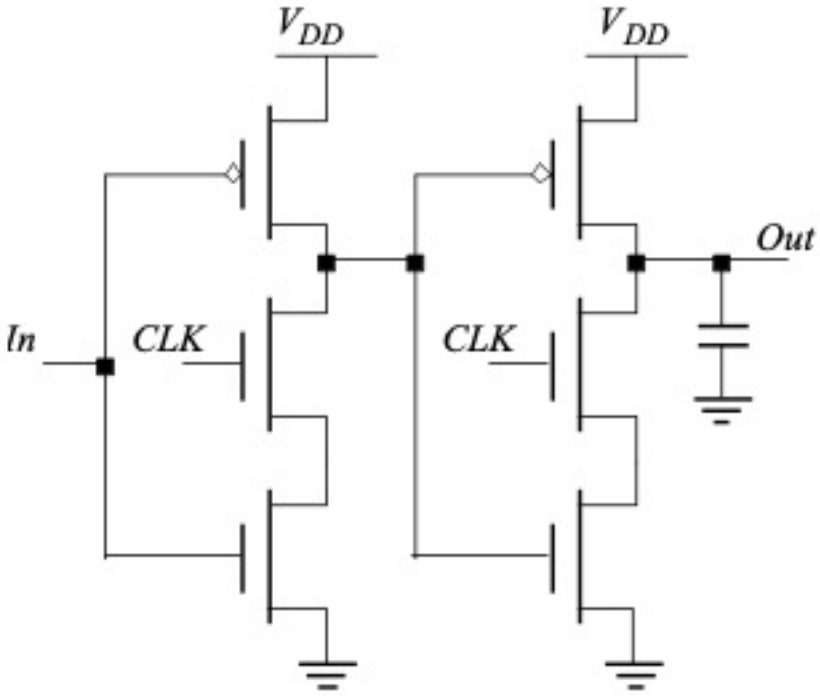
A keeper makes a dynamic circuit static

C²MOS Dynamic Latch

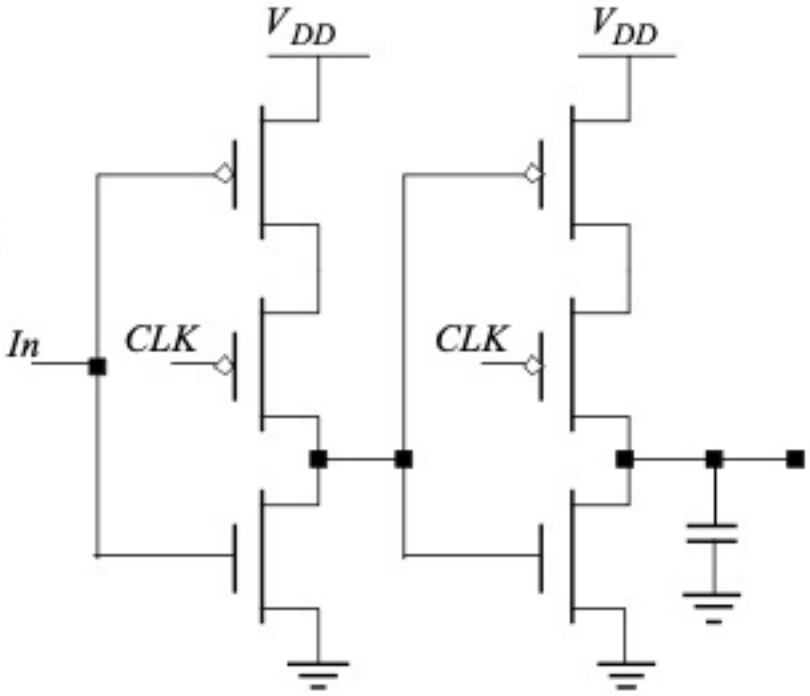


Keepers are often used to make the flip-flop static

TSPC Dynamic Latch

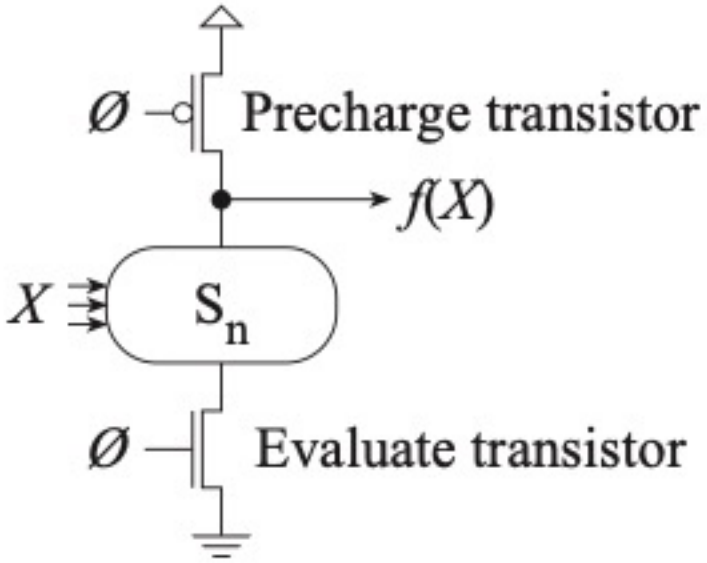


Positive latch
(transparent when CLK = 1)

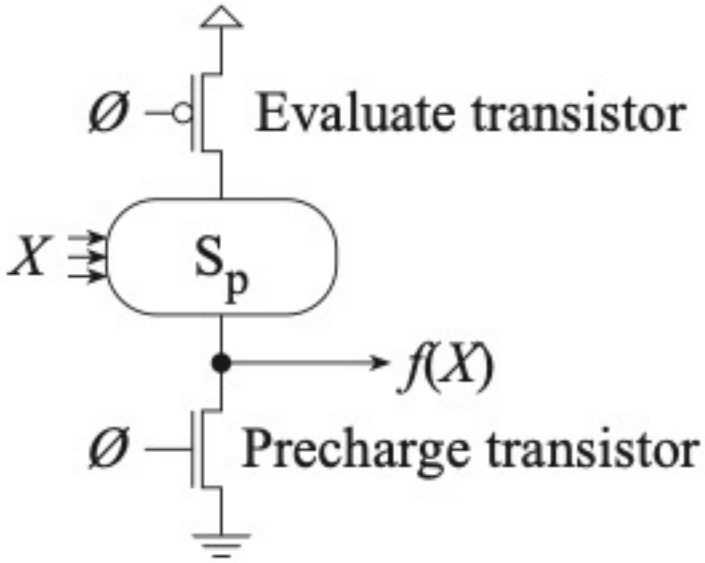


Negative latch
(transparent when CLK = 0)

Precharged Logic

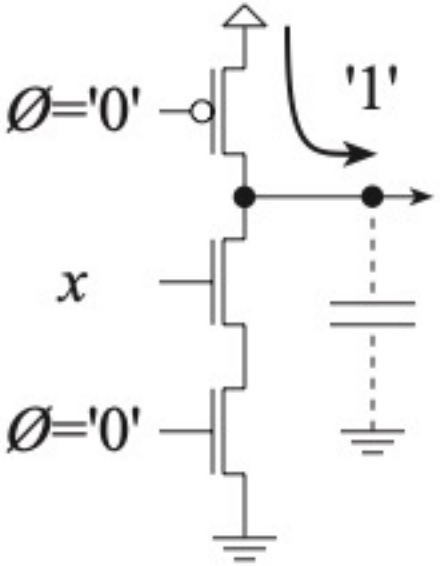


NMOS logic

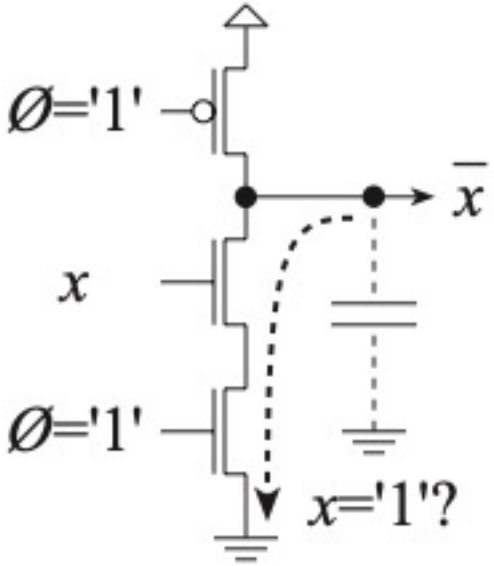


PMOS logic

Operation

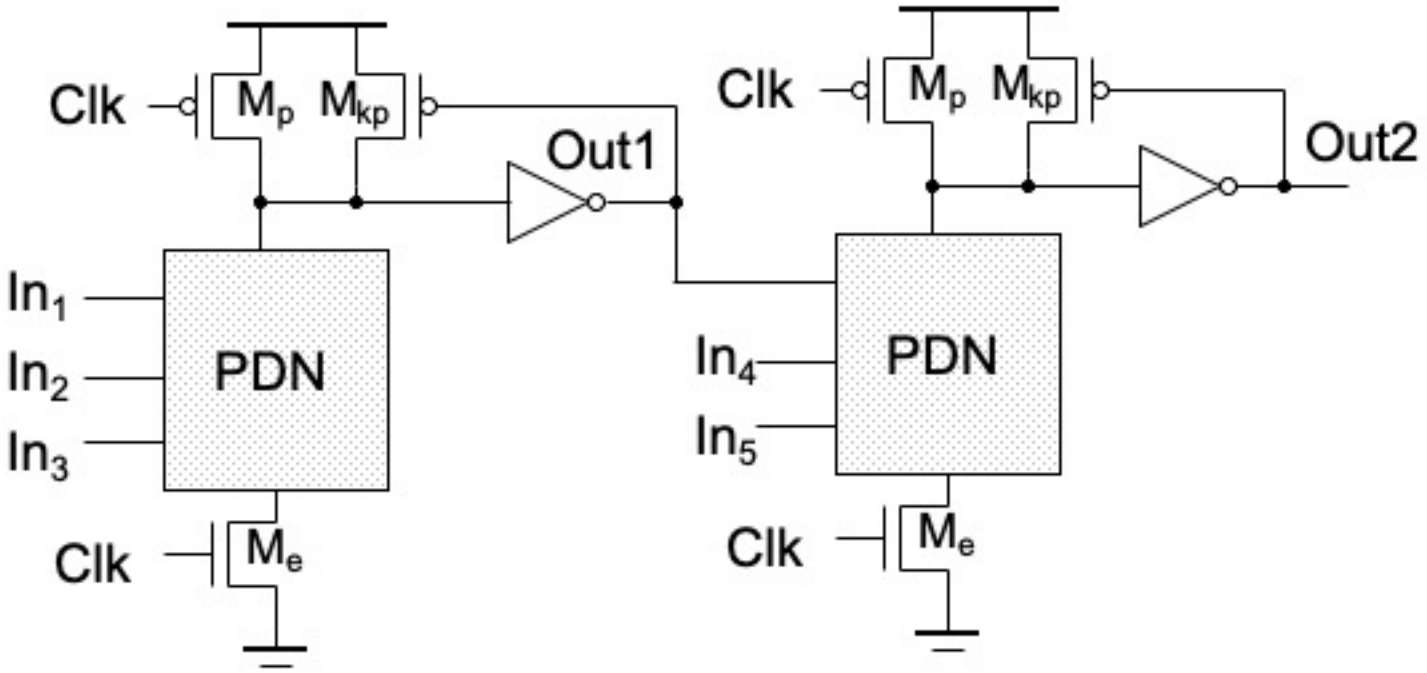


Precharge phase

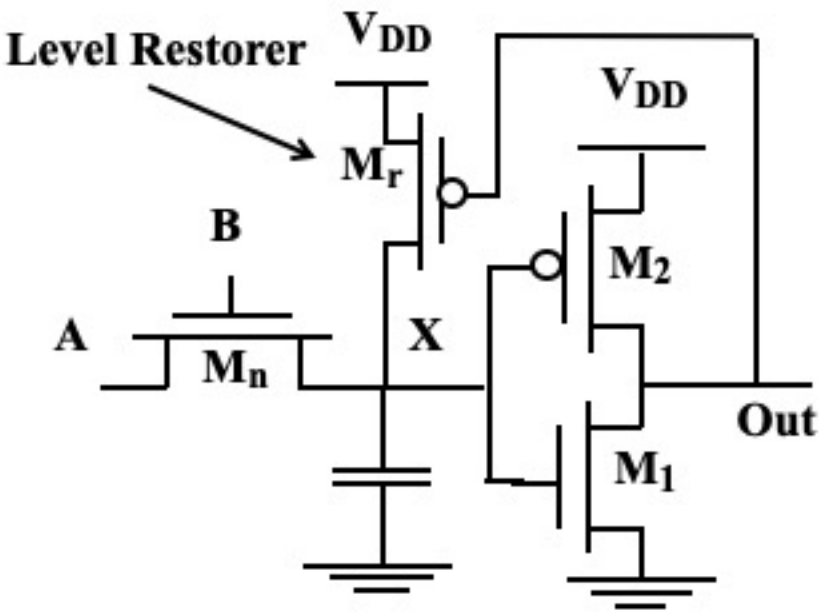


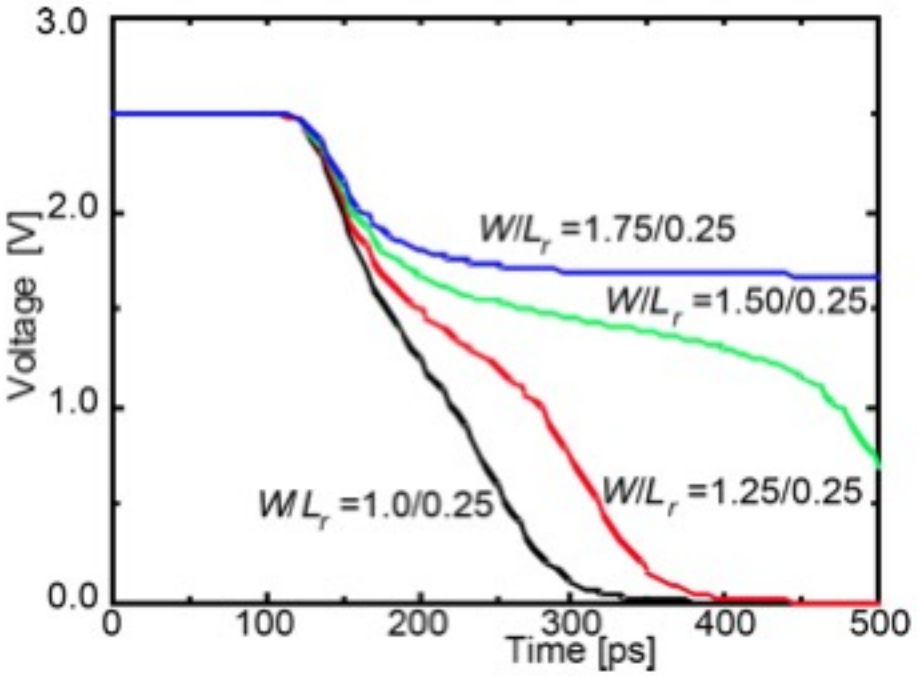
Evaluate phase

Domino Logic



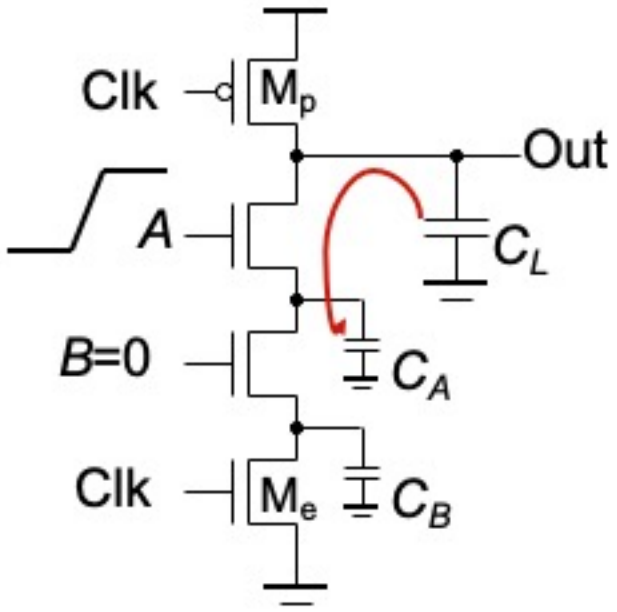
Level Restoring Transistor





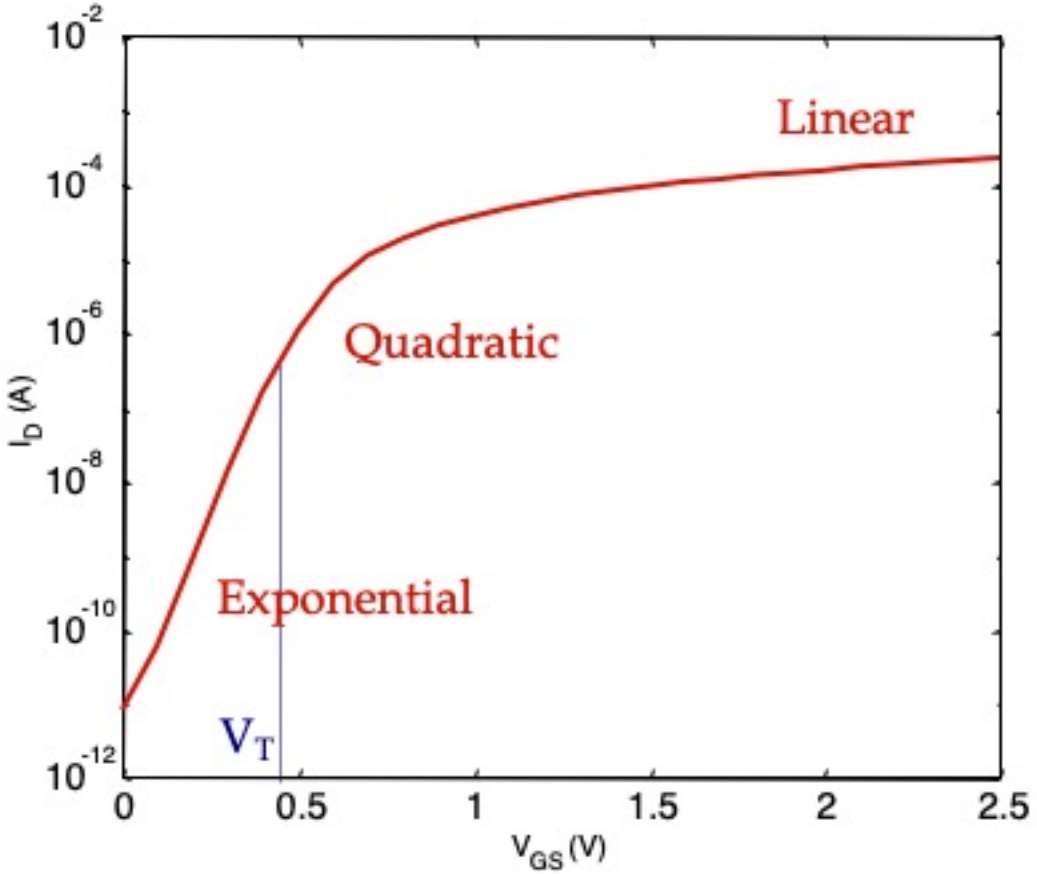
Useful in CPL and Domino logic

Charge Sharing



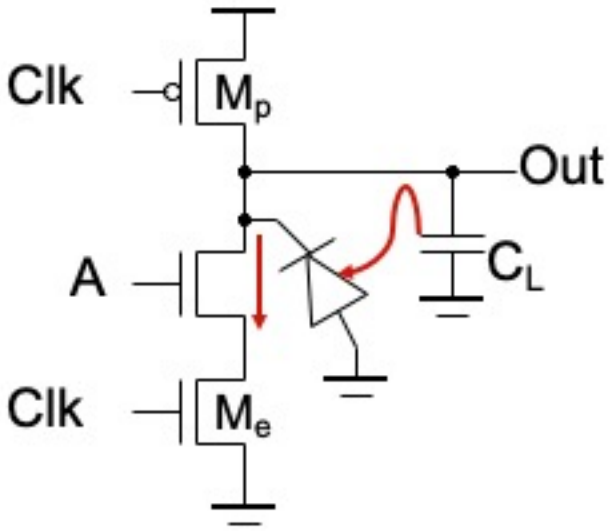
Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

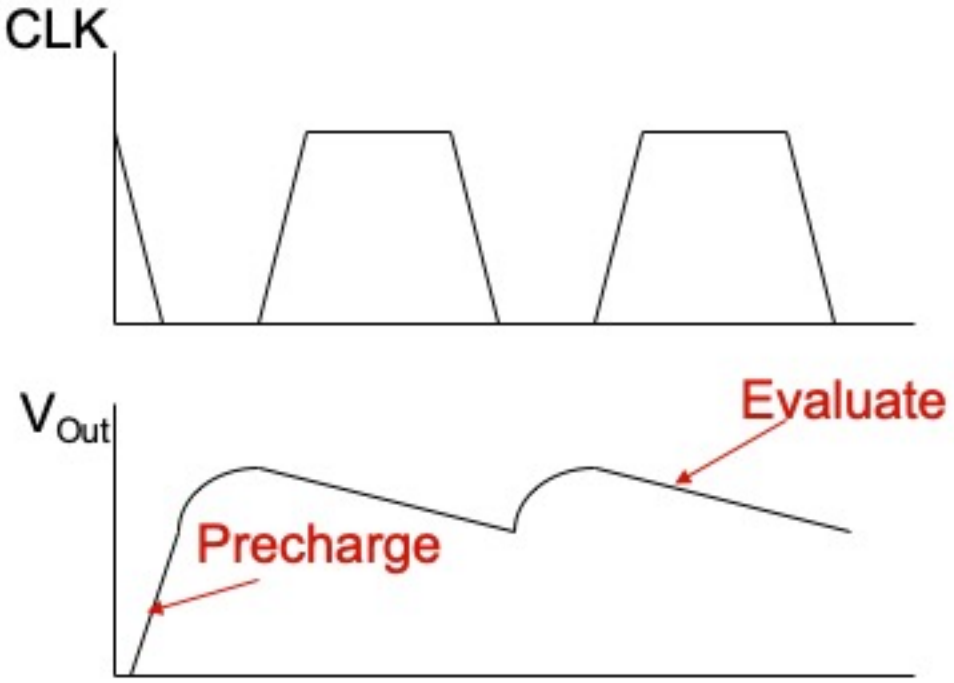
Sub-Threshold Conduction



$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$

Charge Leakage





Leakage sources

Dominant component is subthreshold current