Parameters for a 0.35 μm process are given in Table 1 below.

Parameter	NMOS	PMOS
μ_0 [cm^2/(Vs)]	400	–130
C_{ox} [F/cm^2]	$4.5 \cdot 10^{-7}$	$4.5 \cdot 10^{-7}$
λ [V^{-1}]	0.03, L = 1 μm	–0.05, L = 1 μm
V_{T0} [V]	0.47	–0.62
γ [V$^{1/2}$]	0.62	–0.41
$2\Phi_F$ [V]	0.86	–0.82
n	1.25	1.25
λ_{sub} [V^{-1}]	0.08	–0.14

Table 1: Process parameters

Exercise 1

Consider the ideal analog integrator circuit in Figure 1 where all current taken from the supply is used to charge the integrating capacitor at the output. The supply voltage is V_{dd} and the output capacitance is C. A sinusoidal signal with frequency f and voltage swing $V_{pp} \leq V_{dd}$ is output. Assume the signal-to-noise ratio to be determined by the thermal noise according to SNR $= 10\log(CV_{pp}^{\,2}) - 10\log(8kT)$, where k is Boltzmann's constant and T is the absolute temperature.

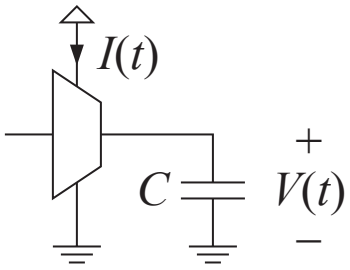


Figure 1. A transconductor.

a) Derive an expression for the power P dissipated.

b) Show that the power-dissipation for the circuit is determined by the requirements on SNR, operating frequency, and temperature.

Exercise 2

Consider the design of analog signal processing systems from a power point of view.

a) Assume that a certain function can be implemented with either analog or digital circuits. What design parameter has a large effect on how the different circuits compare with respect to the power dissipation?

b) What kind of analog system components may have an advantage of being processed in the log-domain with respect to power dissipation?

c) How should high frequency analog circuits be designed to obtain low power consumption?

d) Very low power consumption can be obtained by the use of MOSFETs operating in the subthreshold region. What are the drawbacks with this approach?

Exercise 3

A certain analog circuit consumes the power $\kappa T f 10^{0.1\mathrm{SNR}}$ when processing a signal with bandwidth f and signal-to-noise ratio SNR (log scale). κ is a proportionality constant and T is absolute temperature. The required dynamic range DR is 70 dB, and SNR $\geq$ 55 dB must be maintained. How much relative power can be saved if we use a compander solution that increases the power consumption with $0.25\kappa T f 10^{0.1\mathrm{DR}}$?

Exercise 4

Consider the common source stage of cascode type in Figure 2. Determine $V_{bias,4}$ and the DC level of V_{in}. Also determine suitable values for the bias voltages $V_{bias,2}$ and $V_{bias,3}$. To guarantee a that $M1$ and $M2$ is properly saturated we choose to design so that $V_{SD(M4)} = V_{SG(M4)} - |V_{T(M4)}| + 0.2$ V and $V_{DS(M1)} = V_{GS(M1)} - |V_{T(M4)}| + 0.2$ V. For these values calculate the output range $[V_{out,min}, V_{out,max}]$ (all transistors should be in saturation region). The widths and lengths of all transistors are 50 µm and 1 µm, respectively. The current is I = 50 µA. Neglect the body effect, channel length modulation effect, and short channel effects in the calculations. Use the process parameters in Table 1 and V_{DD} = 3.3 V.

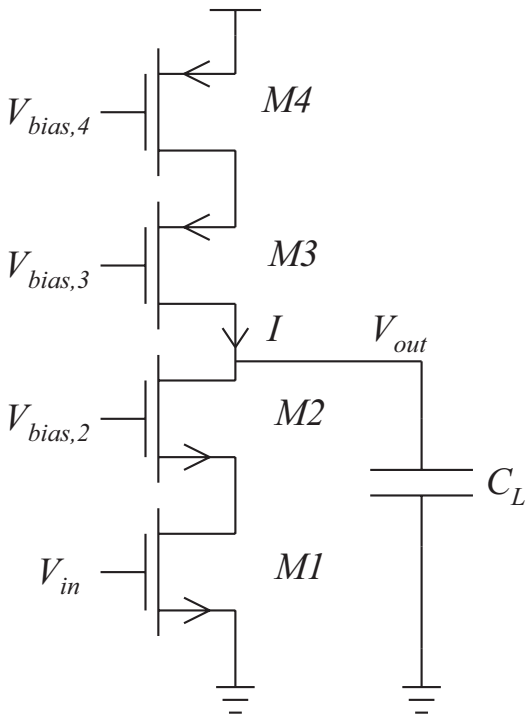


Figure 2. CS amplifier of cascode type.

Exercise 5

The common source amplifier shown in Figure 3 can be designed to operate with the transistors operating either in saturation or subthreshold region. For a low power analog circuit, such the ones in hearing aids, the transistors are usually operated in the subthreshold region or weak inversion. The drain current of an NMOS transistor is given by

$$I_{Dn} = I_{D0n}\frac{W}{L}e^{\frac{V_{GS}-V_T}{n_s V_\Theta}}\left(1+\lambda_n V_{DS}\right)$$

For small gate source voltages (subthreshold operation) the current increases exponentially (a straight line in the logarithmic plot) a further increase in gate source voltage yields a quadratically increase in the current (saturation region). Increasing the gate voltage even more, yields a transistor in the linear operation region. Use the process parameters in Table 1.

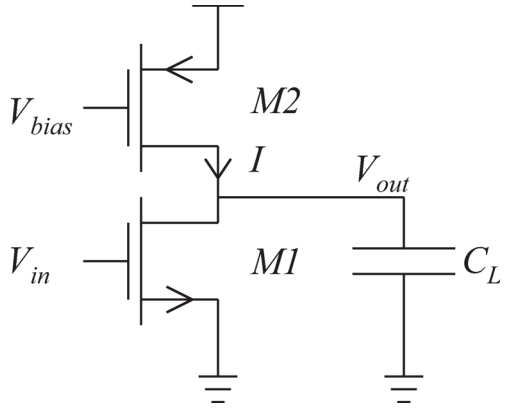


Figure 3. A common source amplifier.

a) Determine the output range of the amplifier shown in Figure 3 assuming that the transistors are biased to operate in the saturation region. Express this in relevant design parameters such as W, L, I_D, and V_{DS}.

b) Derive the DC gain. Assume that the transistors are biased to operate in the saturation region. (In saturation: $g_{ds} = \lambda I_D$, $g_m = 2I_D / V_{eff}$)

c) Derive a small signal model of the amplifier operating in the subthreshold region and derive the DC gain.

d) Which parameters should you change to increase the DC gain of a common source amplifier when the transistors are operating in the saturation region and the subthreshold region, respectively.

e) In which region should you bias the amplifier if you would like to have a large unity-gain frequency?

f) In which region should you bias the amplifier if you would like to have a low power consumption?

Exercise 6

The minimum power consumption of a single-pole low-pass filter with bandwidth B should be compared for analog and digital implementations. Due to thermal noise an analog implementation must consume at least the power $8k_bT \cdot B \cdot 10^{0.1\mathrm{SNR(dB)}}$, where k_b is Boltzmann's constant, T is the absolute temperature, and SNR(dB) is the signal-to-noise ratio. A corresponding digital implementation consumes approximately the power $72n^2E_tB$ at a minimum, where n is the data word length, and E_t is the energy consumed per bit transition. Assume the signal-to-quantization noise ratio is SQNR(dB) ≈ $6.0n$.

a) What fundamental limit bounds the minimum energy E_t per bit transition of the digital implementation? What is the magnitude of the fundamental limit?

b) What circuit limit bounds the minimum energy E_t per bit transition of the digital implementation? What is the magnitude of the circuit limit?

c) Assume that thermal noise and quantization noise are the only noise sources in the comparison. Specify the requirements for the analog implementation to have a lower minimum power consumption than the digital implementation. (*Hint:* assuming a required digital signal power that is 4 times the noise power may simplify the calculations.)

Exercise 7

We have a common-source amplifier with an impedance load as shown in Figure 4. The load, Z_L, consists of a 100 Ω resistor in parallel with a 1 pF capacitor. The stage is biased for maximum swing, and the transistor always operate in its saturation region. Only thermal noise is considered in this amplifier stage where the transistor noise is given by $v_n^2 = 4kT\gamma / g_m$ and the resistor noise is $v_n^2 = 4kTR$. Assume T = 300 K, γ = 2/3, and that the output impedance of the transistor is infinite.

Sketch how the total output noise power depends on the input DC operating point described in terms of V_{eff}/V_{DD}. Indicate the boundaries and levels in your plot.

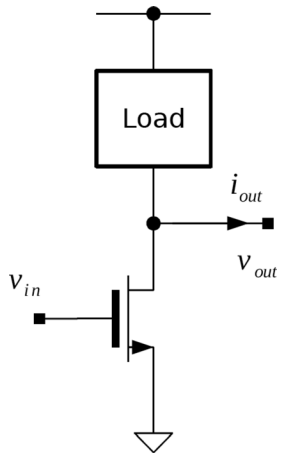


Figure 4. Single-stage common-source amplifier.

Solution 1

a) Power dissipation: $P = I_{av}V_{dd} = QfV_{dd} = CfV_{pp}V_{dd}$

b) Assume $V_{pp} = cV_{dd}$, where $0 \le c \le 1$ is a constant.

Signal-to-noise ratio: $SNR = 10\log\left(\frac{CV_{pp}^2}{8kT}\right) \Rightarrow CV_{pp}^2 = 8kT \cdot 10^{0.1SNR}$

Power dissipation: $P = fCV_{pp}V_{DD} = fCV_{pp}\frac{V_{pp}}{c} = \frac{f \cdot 8kT \cdot 10^{0.1SNR}}{c}$

We see that the power is determined from SNR, f, and T since c and k are constants. These variables should be selected as low as possible for minimum power dissipation, restricted by the respective requirements. Hence, these requirements determines the minimum power dissipation.

Solution 2

a) A low SNR favors an analog implementation while a high SNR favors a digital.

b) Log-domain signal processing is most efficient in cases that require a high dynamic range but only a low signal-to-noise ratio.

c) Ways to reduce power of high-frequency analog
- Select architecture with few devices operating
- Amplify signals early in the signal chain
- Use subsampling if possible

d) Analog circuits using subthreshold MOSFETs generally suffer from low bandwidth, high drain-bulk and source-bulk leakage, and poor linearity.

Solution 3

A direct solution requires SNR = DR = 70 dB, yielding the consumption $P_d = \kappa Tf10^7$. Denoting the amount of compression/expansion x (log scale), the total power consumption for a compander solution is

$P_c = \kappa Tf10^{0.1(\mathrm{DR}-x)} + 0.25\kappa Tf10^{0.1\mathrm{DR}} = \kappa Tf \cdot 10^7 \cdot (10^{-0.1x} + 0.25)$, $0 < x \le 15$ dB

Relative power is $P_r(x) = P_c/P_d = (10^{-0.1x} + 0.25)$

Relative power saving is $P_s = 1 - P_r(15) \approx 72\%$

Solution 4

We define the effective gate-source voltage of an NMOS transistor as $V_{eff,n} = V_{GSn} - V_{Tn}$ and, similarly, the effective source-gate voltage of a PMOS transistor as $V_{eff,p} = V_{SGp} - |V_{Tp}|$

We have the simplified current equation for a saturated transistor $I_D \approx \beta V_{eff}^2/2$

Since the transistor sizes are equal for $M1$ and $M2$, and they have the same drain current, they will also have the same V_{eff}. Similarly, $M3$ and $M4$ will have the same V_{eff}

For NMOS transistors $M1$ and $M2$, $V_{eff,n} = \sqrt{2I_D/\beta_n} \approx 0.105$ V and for PMOS transistors $V_{eff,p} = \sqrt{2I_D/\beta_p} \approx 0.185$ V

Thus, $V_{in,DC} = V_{eff,n} + V_{Tn} = 0.105 + 0.47$ V ≈ 0.58 V

$V_{bias,2}$ is not determined by the current alone, we also need to know V_{DS} for $M1$.
We have $V_{bias,2} = V_{DS,1} + V_{GS,2} = V_{DS,1} + V_{eff,n} + V_{Tn}$

To ensure that $M1$ is properly saturated we choose $V_{DS,1} = V_{eff,n} + 0.2$ V
and thus $V_{bias,2} = 2V_{eff,n} + V_T + 0.2$ V ≈ 0.88 V

We make a similar analysis for the PMOS part and find that
$V_{bias,4} = V_{DD} - (V_{eff,n} + |V_{Tp}|) = V_{DD} - (0.185 + 0.62)$ V

To ensure that $M4$ is properly saturated we set $V_{SD,4} = V_{eff,p} + 0.2$ V and find that
$V_{bias,3} = V_{DD} - (2V_{eff,n} + |V_{Tp}| + 0.2\text{ V}) \approx 3.3 - (2\cdot 0.185 + 0.62 + 0.2)$ V $= 2.11$ V

The output range is now given by the following relations
$V_{out} \geq V_{DS,1} + V_{eff,n} = 2V_{eff,n} + 0.2$ V ≈ 0.41 V
$V_{out} \leq V_{DD} - (V_{SD,4} - V_{eff,p}) = V_{DD} - (2V_{eff,n} + 0.2\text{ V}) \approx 2.73$ V

Solution 5

a) Neglecting channel length modulation factor: $\sqrt{\frac{2I}{\beta_n}} < V_{out} < V_{DD} - \sqrt{\frac{2I}{\beta_n}}$

b) DC gain: $-\frac{g_m}{g_{dsp} + g_{dsn}} = -\frac{2}{(V_{GS} - V_{Tn})(\lambda_p + \lambda_n)}$

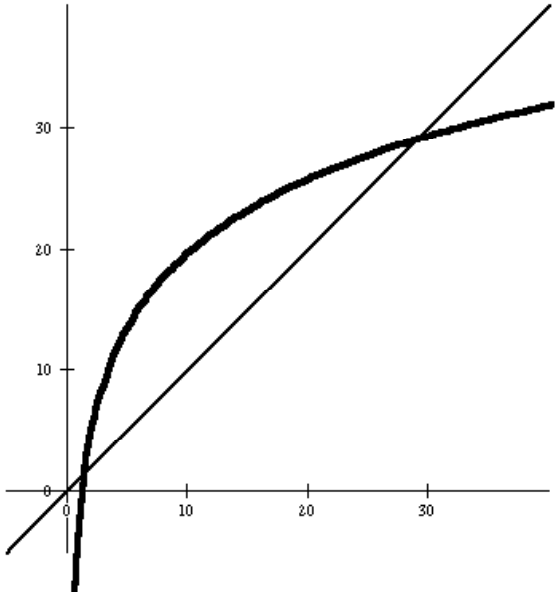
c) DC gain: $-\frac{g_m}{g_{dsp} + g_{dsn}} = -\frac{1/(nV_\Theta)}{\lambda_p + \lambda_n}$ . . . d), e), f) *not available yet*

Solution 6

a) The switching energy must be larger than the thermal noise energy k_bT.

b) The circuit gain must be larger than one, which for static CMOS logic requires a voltage swing $V_{min}=\beta k_bT/q$, where β typically is between 2 and 4. The energy for moving a single electron through the minimum potential is then $qV_{min}=\beta k_bT$.

c) Analog power consumption: $P_A = 8k_bTB\cdot 10^{0.1\text{SNR(dB)}}$
Using $\beta=4$ and $n^2=\text{SQNR(dB)}^2/6.0^2 \Rightarrow$
Digital P: $P_D = 72n^2E_tB = 4\cdot 72\cdot\text{SQNR(dB)}^2k_bTB/36$
Set $P_A < P_D$ and SNR(dB) = SQNR(dB) = $x \Rightarrow$
$8kTB\cdot 10^{0.1x} < 4\cdot 72\cdot x^2k_bTB/36 \Leftrightarrow 10^{0.1x} < x^2 \Rightarrow x = 20\log(x)$. Equation has two solutions; see plot on next page, where heavy line is $y_{right}=20\log(x)$ and the other is $y_{left}=x$.
Solve e.g. using iteration $x_{i+1} = 20\log(x_i)$, $x_0 = 10$ dB $\Rightarrow x_5 \approx x_4 \approx 29$ dB
Second solution x ≈ 1.1 dB can e.g. be obtained from iteration of $x_{i+1} = 10^{0.05x_i}$
However, the second solution will result in an uninteresting specification since SNR would be close to 0 dB (and n close to zero bits). Hence the analog system may be designed with lower minimum power consumption if the requirements on SNR<29 dB (corresponding to $n < \lceil 29/6.0 \rceil = 5$ bits).



Solution 7

Noise for resistor: $i_r^2(j\omega) = 4kT/R_L$

Noise for transistor: $i_r^2(j\omega) = 4kT\gamma g_m$

Noise bandwidth: $p_1/4 = 1/4\, R_L C_L$

Max swing means output is biased at $V_{OUT} = V_{DD}/2$

This means $V_{OUT} = V_{DD}/2 = V_{DD} - R_L I_D \Rightarrow 2R_L I_D = V_{DD}$

Therefore $i_n^2(j\omega) = i_r^2(j\omega) + i_t^2(j\omega) = 4kT/R_L + 4kT\gamma g_m$ such that (using Norton equivalent) the "input" noise voltage source (at the output of the transistor) becomes

$v_n^2(j\omega) = R_L^2\left[i_r^2(j\omega) + i_t^2(j\omega)\right] = 4kTR_L + 4kT\gamma g_m R_L^2$

The total noise power is the integrated noise over the noise bandwidth:

$$P_{tot} = \left(4kTR_L + 4kT\gamma g_m R_L^2\right)\cdot\frac{p_1}{4} = \frac{kT}{C}\left(1+\gamma g_m R_L\right)$$

We know that g_m is given by $g_m = 2I_D/V_{eff}$ where V_{eff} is the effective gate voltage on the transistor. We can refer to this voltage as the input voltage. Combining these equations gives us

$$P_{tot} = \frac{kT}{C}\left(1+\frac{\gamma 2 I_D R_L}{V_{eff}}\right)$$

Due to the biasing we know that it can be written as $P_{tot} = \dfrac{kT}{C}\left(1+\dfrac{V_{DD}}{V_{eff}}\right)$

We know k and C, T, and γ. Remaining is the V_{DD} and V_{eff}. The total output noise is sketched for the ratio V_{DD}/V_{eff} in e.g. log scale. Typical limits would be 0 and V_{DD}, or possibly V_{DD} to $V_{DD} + V_T$.

$P_{tot}(x) \approx 4\left(1+\dfrac{1}{x}\right)$, where $x = V_{eff}/V_{DD}$