Exercise 1

In Figure 1 the propagation delay of a full adder is plotted as a function of supply voltage. What is the lowest supply voltage that can be used for a 4-bit Ripple Carry Adder (RCA) that should have a delay of at most 2 ns?

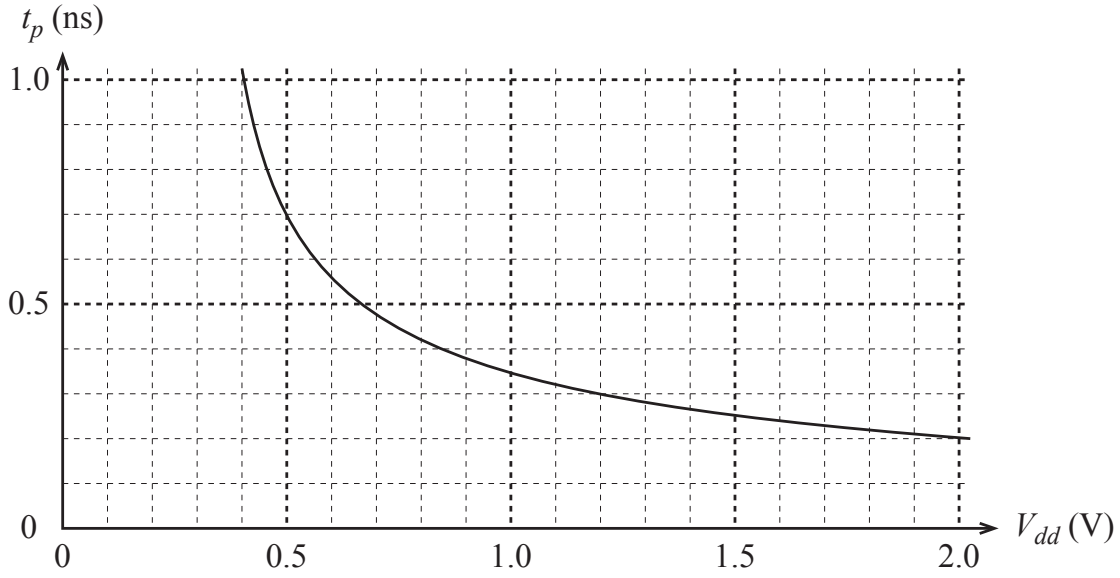


Figure 1. $t_p(V_{dd})$ of an FA.

Exercise 2

a) Write the functions s_j and c_{j+1} of a full adder (FA) as a Boolean function consisting of a_j, b_j, c_j, AND, OR, and XOR.

b) Make a sketch of the FA (on gate level). Assume that only two-input AND, OR and XOR gates are used.

c) Write the function for carry out of a 4-bit Ripple Carry Adder (RCA) and determine the critical path. Denote the inputs as a_j, b_j, and c_0, and the outputs as s_j and c_4 (carry out) where $j = 0, 1, 2, 3$.

Hint: Use the sketch from 2b) when determining the critical path.

d) Design a Carry-Lookahead Adder (CLA) using propagate and generate functions $P_j = a_j \oplus b_j$ and $G_j = a_j b_j$, respectively. Expand the expressions for c_3 and c_4. Use tree structures to decrease the propagation delay. Determine the new propagation delays of s_3 and c_4. Assume that the delay of AND and OR are equal.

e) What is the relative change in propagation delay of the CLA in 2d) compared with the RCA in 2c)? Assume that the delays of all two-input gates are equal.

Exercise 3

In Figure 2 a 16-bit Carry Select Adder (CSL) is shown. The propagation delays of a 4-bit RCA and a multiplexer are $4t_a$ and $t_m = 0.5t_a$, respectively.

a) Determine the propagation delay of the output signals s_3, s_7, s_{11}, s_{15}, and c_{16}.

b) Compare the propagation delay and the area with a 16-bit Ripple Carry Adder assuming the area of a multiplexer is one third of a full adder.

c) How much relative power can be saved if we scale the supply voltage so that the Carry Select Adder obtains the same delay as the Ripple Carry Adder operating at a supply voltage of 2.0 V? Assume that the delay t_a of a full adder varies with supply voltage according to the graph shown in Figure 1, and the switched capacitances of an FA and a multiplexer are C_{FA} and $C_{MUX} = C_{FA}/3$, respectively.

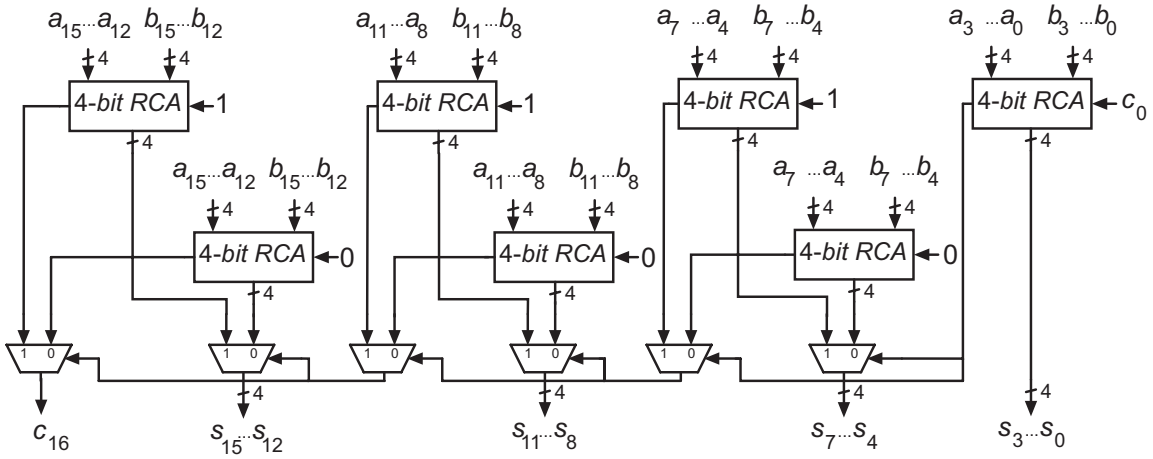


Figure 2. 16-bit Carry Select Adder.

Exercise 4

Consider the 16-bit Carry Skip Adder (CSK) shown in Figure 3. Using a power supply voltage of 2.0 V, the propagation delay of a full adder and a multiplexer are $t_{FA} = 0.40$ ns and $t_M = 0.20$ ns, respectively. Assume that the propagation delays of the select signals to the multiplexers are less than $4t_{FA}$. The maximal allowed propagation delay of the carry-skip adder is 5.0 ns. $P_j = a_j \oplus b_j$.

a) Explain how the circuit works.

b) Determine the propagation delay of signals s_3, s_7, s_{11}, s_{15}, and c_{16}.

c) How much relative power can be saved if a lower power supply voltage is used? Assume $V_T = 0.32$ V and $r = 1.4$.

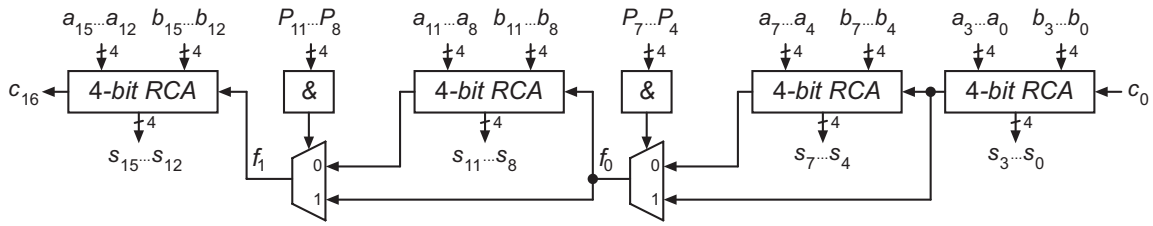


Figure 3. 16-bit Carry Skip Adder.

Exercise 5

A circuit used for adding three 6-bit binary numbers $X = \langle x_5, \ldots, x_0 \rangle$, $Y = \langle y_5, \ldots, y_0 \rangle$, $Z = \langle z_5, \ldots, z_0 \rangle$ and computing a sum $S = \langle s_5, \ldots, s_0 \rangle$ is shown in Figure 4. The inputs come from registers. A full adder (FA) has the propagation delay 60 ps for all inputs to all outputs. To solve the problems below you may use 2:1 multiplexers that have a propagation delay of 50 ps, and inverters that have a propagation delay of 30 ps.

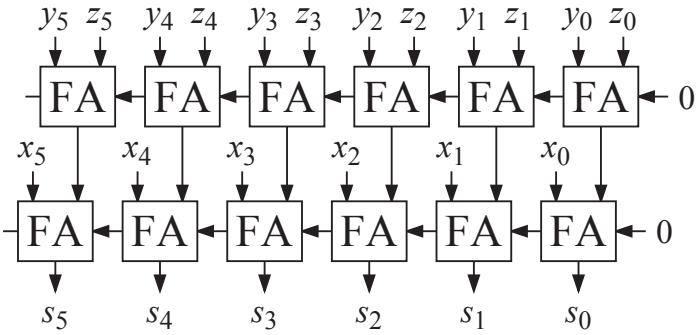


Figure 4. Adder schematic.

a) Explain why different delays in the paths to an FA cause extra power to be consumed.

b) Estimate how much power that could be saved by delay balancing the circuit. For simplicity, assume that the dynamic power dissipation of an inverter is 20% of the power of an FA. Further assume that the power dissipation of an FA doubles with every 100 ps difference in maximum skew at the inputs.

c) Interleave the circuit with a factor of 2. How much power can be saved from voltage scaling if the original throughput is maintained? Assume $V_{DD} = 1.0$ V, $V_t = 0.25$ V and $r = 1.5$. Neglect capacitance from extra multiplexers and registers.

Exercise 6

Make a sketch of a Carry Save Adder CSA tree where the number of inputs are 9. Assume a full adder delay is t_{FA} and the input and output wordlength is n bits.

a) What is the critical path through the CSA tree?

b) What is the critical path through a corresponding adder tree consisting of RCAs?

c) What n yields a relative delay for the CSA that is twice of the tree with RCAs?

Exercise 7

a) In memories a row decoder is used to select a word. Compare briefly the speed and power consumption for a precharged NAND based decoder and a precharged NOR based decoder.

b) Describe how half-vdd precharge of the data lines in a memory works. What are the possible power savings compared with full-vdd precharge?

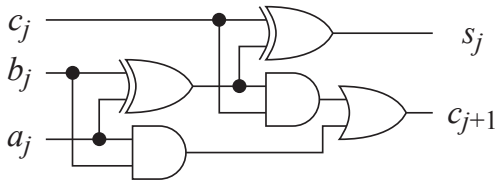
Solution 1

Four FAs need to be cascaded in the 4-bit RCA. For a total delay of 2 ns, each FA can at most have a delay of 0.5 ns. Hence the minimum supply voltage that can be used for the FAs is approximately 0.7 V according to Figure 1.

Solution 2

a) $s_j = a_j \oplus b_j \oplus c_j$
$c_{j+1} = a_j b_j + (a_j \oplus b_j) c_j$

b)



c) $c_4 = a_3 b_3 + (a_3 \oplus b_3)(a_2 b_2 + (a_2 \oplus b_2)(a_1 b_1 + (a_1 \oplus b_1)(a_0 b_0 + (a_0 \oplus b_0) c_0)))$
The critical path is 1 XOR, 4 OR and 4 AND (using gates with two inputs)
$t_{C_4} = 4t_{OR} + 4t_{AND} + t_{XOR}$
$t_{S_3} = 3t_{OR} + 3t_{AND} + 2t_{XOR}$

d) $c_1 = G_0 + P_0 c_0$
$c_2 = G_1 + P_1 c_1 = G_1 + P_1 G_0 + P_1 P_0 c_0$
$c_3 = G_2 + P_2 c_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0$
$c_4 = G_3 + P_3 c_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0$
$s_j = P_j \oplus c_j$
$t_{c_4} = 5t_{AND,\,OR} + t_{XOR}$
$t_{c_3} = 4t_{AND,\,OR} + t_{XOR}$
$t_{s_3} = 4t_{AND,\,OR} + 2t_{XOR}$

e) Assuming same delay t_g for all two-input gates
$\frac{t_{CLA}}{t_{RCA}} = \frac{6t_g}{8t_g} = 0.75 \Rightarrow$ relative change is -25%

Solution 3

a) s_3: $4t_a$
s_7: $4t_a + t_m$
s_{11}: $4t_a + 2t_m$
s_{15}: $4t_a + 3t_m$
c_{16}: $4t_a + 3t_m$

b) Approximating delay $t_m \approx t_a/2$ and area $A_m \approx A_a/3 \Rightarrow t_{CSL}/t_{RCA} \approx (4+3/2)t_a//(16t_a) \approx 0.34$ and $A_{CSL}/A_{RCA} \approx (28+6/3)A_a//(16A_a) \approx 1.94$

c) Full adder delay @ $V_{dd} = 2.0$ V is $t_a \approx 0.2$ ns

$$t_{CSL} = t_{RCA} \Rightarrow \left(4 + 3 \cdot 0.5\right)t_{new} = 16t_a \Rightarrow t_{new} = \frac{16}{5.5}t_a \approx 0.58 \text{ ns}$$

Voltage @ $t_{FA} \approx 0.58$ ns is $V_{new} \approx 0.6$ V

$$\frac{P_{CSL}}{P_{RCA}} = \frac{\left(28 + 6/3\right)C_{FA}fV_{CSL}^2}{16C_{FA}fV_{RCA}^2} = \frac{31 \cdot 0.6^2}{16 \cdot 2.0^2} \approx 0.17 \Rightarrow 83\% \text{ savings}$$

Solution 4

a) If $P_7P_6P_5P_4 = 1$, the carry out c_{out0} of the first 4-bit RCA will propagate to the carry out c_{out1}, resulting in $c_{out1} = c_{out0}$. This means that it is possible to choose c_{out0} as carry in to the third 4-bit RCA instead of c_{out1}. c_{out0} is valid after $4t_{FA}$.

If $P_7P_6P_5P_4 = 0$, the carry out c_{out1} of the second 4-bit RCA is independent of c_{out0}, resulting in that c_{out1} is valid after $4t_{FA}$. Depending on the function $P_7P_6P_5P_4$ we choose between c_{out0} and c_{out1} as carry in f_0 to the third 4-bit RCA. Hence, the propagation delay of the internal signal f_0 is $4t_{FA} + t_M$.

b) Propagation times
s_3: $4t_{FA} = 1.6$ ns
s_7: $8t_{FA} = 3.2$ ns
s_{11}: $8t_{FA} + t_M = 3.4$ ns
s_{15}: $8t_{FA} + 2t_M = 3.6$ ns
c_{16}: $8t_{FA} + 2t_M = 3.6$ ns

c) The propagation time for the 16-bit carry-skip adder is 3.6 ns. This gives us the ability to increase the propagation delay from 3.6 ns to 5.0 ns, which means that the propagation delay can be increased by 39%.

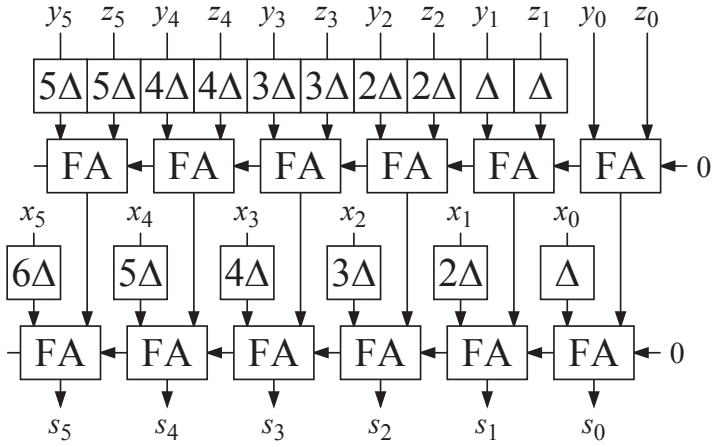
Perform supply voltage scaling $\frac{V_{dd(new)}}{\left(V_{dd(new)} - V_T\right)^{1.4}} = 1.39\frac{V_{dd(old)}}{\left(V_{dd(old)} - V_T\right)^{1.4}}$,

Solving for $V_{dd(new)}$ yields $V_{dd(new)} \approx 1.3$ V.
The relative power saving becomes $1–1.3^2/2.0^2 \approx 58\%$.

Solution 5

a) When the inputs switch at different times, the FA will operate on the wrong input during the time difference. This could potentially cause a glitch with extra energy consumption $E_g = CV_gV_{DD}$, where V_g is the amplitude of the glitch.

b) A delay balanced adder where Δ can be implemented with two cascaded inverters is shown below.

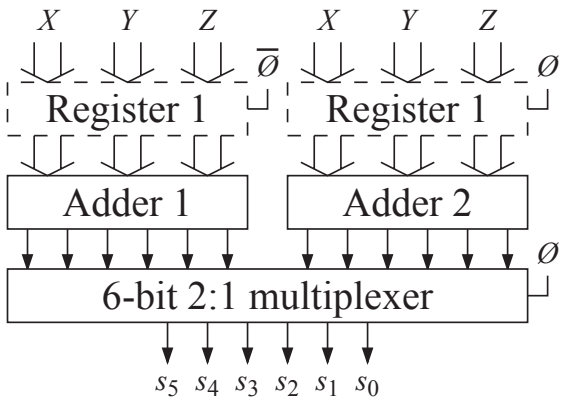


The power dissipation of a basic circuit increases as $P(\tau) = P \cdot 2^{\tau/k}$, where τ is the skew. Since τ = 100 ps ⇒ $\tau/k = 1$, k = 100 ps. Assume P consumption of inverter is P_0. The original adder have 12 FAs with skews {0,1,1,2,2,3,3,4,4,5,5,6} times 60 ps, yielding the power dissipation $P_{\text{old}} = 5P_0(1\cdot 2^0+2\cdot 2^{0.6}+2\cdot 2^{1.2}+2\cdot 2^{1.8}+2\cdot 2^{2.4}+2\cdot 2^{3.0}+2^{3.6}) = 271.36P_0$.

In the delay balanced adder, all skews are zero, yielding a power dissipation for the FAs that is $P_{add} = 12\cdot 5P_0 = 60P_0$. However, the additional delay of 3(1+2+3+4+5)+6 times 60 ps requires 2[3(1+2+3+4+5)+6] = 102 inverters drawing the power $P_\Delta = 102P_0$. Total power is Pnew = $162P_0$.

Power saving is $1-P_{new}/P_{\text{old}} \approx 0.40 = 40\%$.

c) An interleaved adder is shown below



Neglecting registers and registers, critical path is $t_c = 7t_{\text{FA}} = 7\cdot 60$ ps = 420 ps. Since the interleaved obtains twice the throughput, the supply voltage can be scaled until $t_{new} = 2t_c$ for maintained throughput.

Hence

$$\frac{t_{new}}{t_{old}} = \frac{2t_c}{t_c} = \frac{V_{new}}{\left(V_{new} - V_t\right)^{1.5}} \frac{\left(V_{old} - V_t\right)^{1.5}}{V_{old}} = \frac{V_{new}}{\left(V_{new} - 0.25\right)^{1.5}} \frac{\left(1.0 - 0.25\right)^{1.5}}{1.0} \Rightarrow$$

$$V_{new} \approx 0.58 \text{ V } \left(+ \text{ imaginary roots}\right)$$

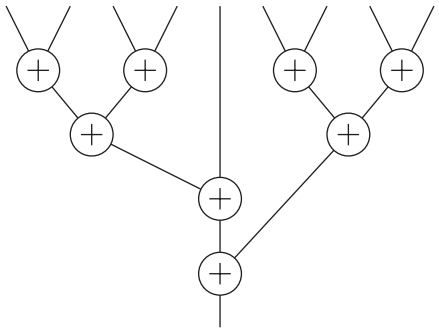
Approximately twice the C is switched at double f, yielding P savings

$$1 - \frac{\frac{f}{2} 2CV_{new}^2}{fCV_{old}^2} \approx 0.67 = 67\%$$

Solution 6

a) The critical path through the carry save adder tree is $4t_{FA}$. Note that the carry and sum vector must be added to achieve the result of the addition in two's complement.

b) Adder tree



The critical path using RCAs is $(4+n)t_{FA}$.

c) Relative delay is $4/(4+n)$. Equating this expression to 1/2 yields $n = 4$.

Solution 7

a) Consider an N-bit decoder. A NAND-based decoder results in N+1 NMOS in series. Only one node is discharged during evaluation. This decoder is slow and not so power hungry. A NOR-based decoder results in 2 NMOS in series. All but one node are discharged during evaluation (N^2–1). This decoder is fast and power hungry.

b) Differential datalines are assumed in both approaches. In full-vdd precharge, both data lines are precharged to vdd and then the data is read by letting one of the lines go low depending on data. In half-vdd precharge both data lines are precharged to half vdd and then the data is read by letting one line go high and the other go low. The differential voltage swing is the same in both cases but only half the energy (power) is needed in the half-vdd scheme since a data line dissipates $CV_{DD}\Delta V$ in an average transition, where ΔV is half in that case.