Exercise 1

a) Which are the two currents that result in the static power dissipation?

b) How is the static power consumption related to the area of a circuit?

c) How does interleaving affect the static power consumption?

d) How does pipelining affect the static power consumption?

e) Discuss the relative effect of interleaving vs. pipelining on static power consumption.

f) Calculate the relative change in gate oxide leakage current I_G if the oxide thickness t_{ox} is reduced from 4 nm to 3 nm. Assume $k_2 = 10 \cdot 10^9$ and $V_{ox} = 2.0$ V.

Exercise 2

a) Describe a method that reduces the power consumption by *decreasing* the threshold voltage V_T.

b) Describe a method that reduces the power consumption by *increasing* the threshold voltage V_T.

c) How can the threshold voltages of MOSFETs be adjusted without changing the doping levels?

Exercise 3

Assuming a subthreshold slope $S = \ln(10) n_s kT/q = 100$ mV/decade, estimate the relative reduction in drain current when V_T is increased from 0.25 V to 0.40 V for a MOSFET with $V_{GS} = 0$ and $\lambda \approx 0$.

Exercise 4

Calculate the subthreshold leakage current for the inverter shown in Figure 1, for both with and without sleep transistor. $V_{DD} = 1.8$ V, $V_{Tp} = -0.3$ V, $V_{Tn} = 0.3$ V, $V_{T,sleep} = 0.6$ V, $I_{0n} = 4.7$ µA, $I_{0p} = -1.6$ µA, $k = 1.381 \cdot 10^{-23}$ J/K, $q = 1.602 \cdot 10^{-19}$ C, $T = 300$ K, $n_s = 1.48$. Neglect channel length modulation effects.

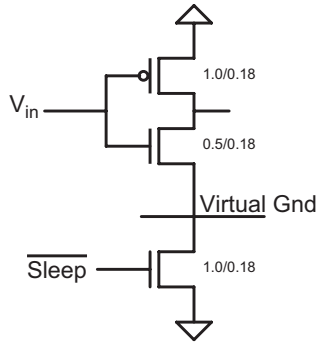

Figure 1. Inverter with sleep transistor.

Exercise 5

Consider an NMOS transistor where the source is connected to ground.
The threshold voltage can be calculated as:

$$V_{Tn} = V_{T0n} + \gamma_n(\sqrt{(V_{SB} + 2|\Phi_{Fp}|)} - \sqrt{2|\Phi_{Fp}|})$$

where $V_{T0n} = 0.34$ V, $\gamma_n = 0.79$ V, $\Phi_{Fp} = -0.30$ V, and $V_{dd} = 1.8$ V.
Voltages between $-V_{dd}$ and V_{dd} are available on chip due to DC/DC-converters.

a) Determine an upper bound of the threshold voltage.

b) Determine a lower bound of the threshold voltage given that we do not want to forward-bias the *pn* junctions.

c) Which bulk voltage should be used to limit the leakage current?

d) Which bulk voltage should be used to achieve maximal speed?

e) What is the ratio of the subthreshold current in c) compared with the current in d)? ($n_s = 1.5$, $kT/q \approx 26$ mV)

Exercise 6

A static CMOS circuit build in a 0.35 μm process has a variable bulk voltage both for the NMOS nets and the PMOS nets. The power supply voltage is 2.5 V. Some process parameters are listed in Table 1. Consider an inverter and determine bulk voltages that result in an 80% reduction of static leakage currents compared with the case where the bulk voltages can not be adjusted. Neglect the currents in the reversed biased pn-junctions. Assume that $V_\theta = kT/q \approx 26$ mV.

Parameter	NMOS	PMOS
μ_0 [cm^2/(Vs)]	400	–130
C_{ox} [F/cm^2]	$4.5 \cdot 10^{-7}$	$4.5 \cdot 10^{-7}$
V_{T0} [V]	0.47	–0.62
γ [V$^{1/2}$]	0.62	–0.41
$2\lvert\Phi_F\rvert$ [V]	0.86	–0.82
n_s	1.25	1.20

Table 1: Process parameters

Exercise 7

Identify all parasitic capacitances in the circuit shown in Figure 2. Redraw the schematic and include the capacitors. Neglect the interconnect capacitance at the input and the output node. The bulk of the PMOS transistors are connected to the power supply while the NMOS are connected to ground. Assume that the input voltage makes a fast transition. Calculate the consumed energy due to charging and discharging parasitic capacitances.

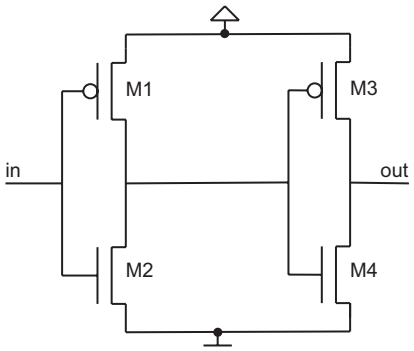

Figure 2. Cascaded inverters.

Exercise 8

In the lower dashed box in Figure 3 an inverter driving a capacitive output load is shown. In the upper dashed box a power supply voltage regulator, consisting of a PMOS transistor and a comparator, is shown. The capacitor C_{dec} is large and it is used to stabilize the local power supply voltage. The transition activity of the input signal *In* is α. When the circuit is not used the local power supply voltage can be turned off by grounding the reference voltage of the voltage regulator (see Figure 3).

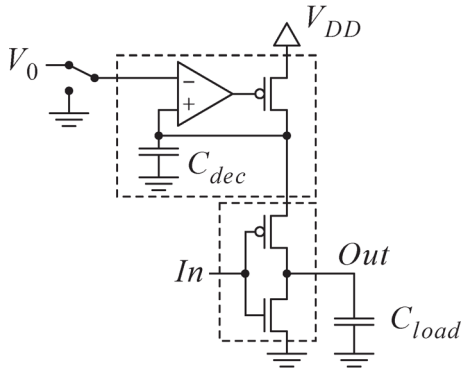

Figure 3. Inverter with local power supply.

a) Determine the dynamic power consumption due to the capacitive output load C_{load}. Compare your result with the case where the inverter in Figure 3 is directly connected to the power supply V_{DD} (i.e. the global power supply is used instead of a local power supply).

b) Determine the average dissipated energy per clock cycle in each transistor.

c) Suggest a technique to keep the static power consumption low while the circuit is turned off.

Solution 1

a) Subthreshold leakage and gate leakage currents.

b) The static power consumption is approximately proportional to the area.

c) Assuming the active area is increased to about the double of the original circuit, then the leakage currents and static power increase to about the double of the original.

d) Since the active area increases due to addition of registers, the leakage currents and static power consumption increase correspondingly.

e) Commonly registers use less area than the logic blocks, hence the pipelined algorithm should leak less than the interleaved algorithm.

f) $\frac{I_1}{I_0} = \left(\frac{t_0}{t_1}\right)^2 e^{\frac{k_2(t_0 - t_1)}{V_{ox}}} = \left(\frac{4}{3}\right)^2 e^{\frac{10(4-3)}{2.0}} \approx 260$

Solution 2

a) By decreasing the threshold voltages the $V_{GSn}-V_{Tn}$ and $|V_{GSp}-V_{Tp}|$ increases. According to the MOSFET current equations, the currents through the transistors increases and therefore the charging and discharging of capacitive loads take shorter times. The extra time margin can be used for scaling of the power supply voltage V_{dd}. Since the dynamic power consumption is in proportion to V_{dd}^2, power will be saved with a lower V_{dd}.

b) When a digital circuit is not doing any operations and when the clock signal is turned off, the circuit still consumes power due to leakage currents. These currents are in proportion to $e^{-q|V_T|/(nkT)}$. Hence, by increasing the threshold voltages, the power consumption due to leakage currents can be reduced.

c) V_T is dependent on the bulk voltage according to $V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{|2\Phi_F|}\right)$.

d) By the use of separate biasing voltages for the bulks of the PMOS and the NMOS transistors, the threshold voltages can be controlled.

Solution 3

$S = \ln(10) n_s kT/q = 0.1 \Rightarrow q/(nkT) = 10\ln(10)$

$$\lambda \approx 0 \Rightarrow \frac{I_{D1}}{I_{D0}} \approx \frac{e^{-\frac{qV_{T1}}{n_s kT}}}{e^{-\frac{qV_{T0}}{n_s kT}}} = \frac{e^{-10\ln(10)V_{T1}}}{e^{-10\ln(10)V_{T0}}} = e^{10\ln(10)(V_{T0}-V_{T1})} = e^{10\ln(10)(0.25-0.4)} \approx 0.030$$

The drain current is reduced with approximately 97%.

Solution 4

$I_{Dn} = 5.15$ nA

$I_{Dp} = -3.5$ nA

With sleep transistor, $I_D = 4.1$ pA. The leakage currents are reduced with the factors of 862 and 1270, respectively.

Solution 5

a) $V_{Tn} \leq 0.95$ V

b) Reverse-biased pn junctions $\Rightarrow V_{SB} \geq 0 \Rightarrow V_{Tn} \geq 0.34$ V

c) $V_B = -1.8$ V

d) $V_B = 0$

e) $$\frac{I_{Dn2}}{I_{Dn1}} = \frac{I_{D0n}\frac{W_n}{L_n}e^{-\frac{V_{Tn2}}{n_s V_\theta}}\left(1+\lambda V_{DS}\right)}{I_{D0n}\frac{W_n}{L_n}e^{-\frac{V_{Tn1}}{n_s V_\theta}}\left(1+\lambda V_{DS}\right)} = \frac{e^{-\frac{V_{Tn2}}{n_s V_\theta}}}{e^{-\frac{V_{Tn1}}{n_s V_\theta}}} = e^{\frac{V_{Tn1}-V_{Tn2}}{n_s V_\theta}} = 1.6\cdot 10^{-7}$$

Solution 6

When the input is logic low the NMOS device determines the static leakage current. The threshold voltage of the transistor should be increased so that the current through the NMOS is reduced with 80%.

$$V_{GSn} = 0 < V_{Tn} \Rightarrow I_{Dn} = I_{D0n}\frac{W_n}{L_n}e^{-\frac{V_{Tn}}{n_s V_\theta}}\left(1+\lambda V_{DS}\right)$$

Let I_{Dn1} denote the original current and I_{Dn2} the current when the threshold voltage has been adjusted.

$$\frac{I_{Dn2}}{I_{Dn1}} = \frac{I_{D0n}\frac{W_n}{L_n}e^{-\frac{V_{Tn2}}{n_s V_\theta}}\left(1+\lambda V_{DS}\right)}{I_{D0n}\frac{W_n}{L_n}e^{-\frac{V_{Tn1}}{n_s V_\theta}}\left(1+\lambda V_{DS}\right)} = \frac{e^{-\frac{V_{Tn2}}{n_s V_\theta}}}{e^{-\frac{V_{Tn1}}{n_s V_\theta}}} = e^{\frac{V_{Tn1}-V_{Tn2}}{n_s V_\theta}} = 1-0.80 = 0.20$$

$$\Rightarrow V_{Tn2} = V_{Tn1} - n_s V_\theta \ln\left(0.20\right) = 0.47 - 1.25\cdot 0.026\ln\left(0.20\right) \text{ V} \approx 0.52 \text{ V}$$

$$V_{T0n} + \gamma_n\left(\sqrt{V_{Sn} - V_{Bn} + 2\left|\Phi_{Fp}\right|} - \sqrt{2\left|\Phi_{Fp}\right|}\right) = 0.47 + 0.62\left(\sqrt{0 - V_{Bn} + 0.86} - \sqrt{0.86}\right) \text{ V} = 0.52 \text{ V}$$

$$\Rightarrow V_{Bn} \approx -0.16 \text{ V}$$

When the input is logic high the PMOS device determines the static leakage current. Let I_{Dp1} denote the original current and I_{Dp2} the current when the threshold voltage has been adjusted.

$$V_{GSp} = 0 < \left|V_{Tp}\right| \Rightarrow \frac{I_{Dp2}}{I_{Dp1}} = \frac{e^{-\frac{\left|V_{Tp2}\right|}{n_s V_\theta}}}{e^{-\frac{\left|V_{Tp1}\right|}{n_s V_\theta}}} = e^{\frac{\left|V_{Tp1}\right| - \left|V_{Tp2}\right|}{n_s V_\theta}} = 0.20$$

$$\Rightarrow \left|V_{Tp2}\right| = \left|V_{Tp1}\right| - n_s V_\theta \ln\left(0.20\right) = 0.62 - 1.20 \cdot 0.026 \ln\left(0.20\right)\ \text{V} \approx 0.67\ \text{V}$$

$$V_{Tp2} = -0.62 - 0.41\left(\sqrt{V_{BSp} - 0 + 0.82} - \sqrt{0.82}\right)\ \text{V} \approx -0.67\ \text{V}$$

$$\Rightarrow V_{BSp} \approx 0.23\ \text{V} \Rightarrow V_{Bp} = V_{dd} + V_{BSp} = 2.5 + 0.23\ \text{V} = 2.73\ \text{V}$$

Solution 7

The parasitic capacitors are shown in Figure 4.

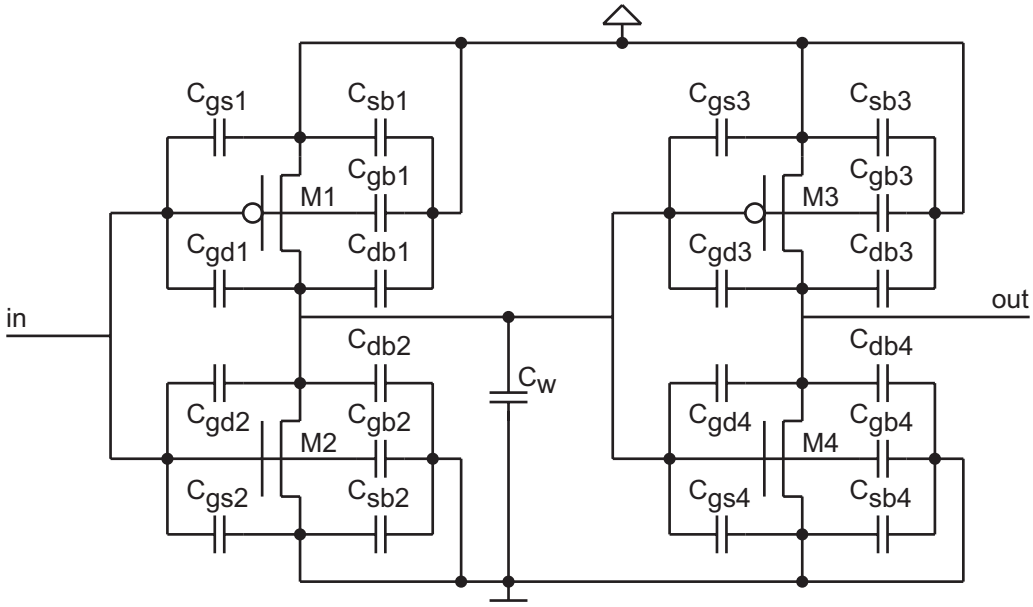

Figure 4. Circuit with parasitic capacitances.

The charge required to change the voltage over a capacitor is $Q = |C\Delta V|$. During the changing of the input signal, all source-bulk capacitance are left unchanged. For gate-source, gate-bulk and drain-bulk capacitance the voltage change is $-V_{dd}$ or V_{dd}. The gate-drain transistors will experience a change of $2V_{dd}$ since the potential is dropping from V_{dd} to ground on one plate while the other is changed from ground to V_{dd}.

$$E = \left(\sum_{i=1}^{4} C_{gsi} + C_{dbi} + C_{gbi} + 2C_{gdi}\right)\frac{V_{dd}^2}{2} + C_w\frac{V_{dd}^2}{2}$$

Solution 8

a) Consider the charging of the output load from 0 V to V_0

Charges taken from power supply: $Q = C_{load}V_0$

Energy taken from power supply: $E_{ps} = C_{load}V_0V_{DD}$

Hence: $P = \alpha_{01}fC_{load}V_0V_{DD} = \alpha fC_{load}V_0V_{DD}/2$

Comparing this power consumption with the case where the inverter is directly connected to the power supply V_{DD}:

$$\frac{P}{P'} = \frac{V_0}{V_{DD}}$$

b) Average energy dissipation in the PMOS in the voltage regulator:

$Q = C_{load}V_0$ (if charging)

$E_1 = \alpha C_{load}V_0(V_{DD} - V_0)/2$

Average energy dissipation in the PMOS in the inverter:

$E_2 = \alpha C_{load}V_0^2/4$

Average energy dissipation in the NMOS in the inverter:

$E_3 = \alpha C_{load}V_0^2/4$

c) A higher threshold PMOS could be used in the voltage regulator. For example a multiple threshold CMOS process could be used or an extra voltage that is higher than V_{DD} could be connected to the body of the PMOS when the local power supply is turned off.