Exercise 1

What is a glitch? How can glitches be reduced in digital circuits?

Exercise 2

a) The propagation time t_d (the time required to drive the output voltage from V_{dd} to $V_{dd}/2$ or from ground to $V_{dd}/2$) for the XNOR gates in Figure 1 is 10 ns. Sketch the signals in node *f* and *x* as functions of time when the inputs <*a*,*b*,*c*> changes from <0,1,1> to <0,0,0>. Consider *a*, *b*, and *c* as ideal.

b) Calculate the dissipated energy due to the two capacitances C_L.

c) A delay of 10 ns is introduced for signal *c* relative to *a* and *b*. Sketch the output signal and calculate the dissipated energy.

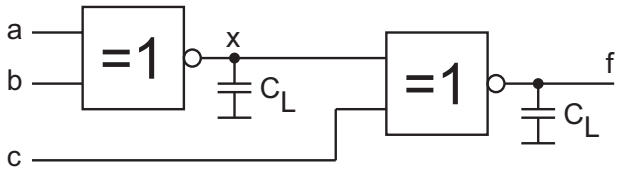

Figure 1. Cascaded XNOR gates.

Exercise 3

In Figure 2 an *N*-bits ripple carry adder is shown. The input signals *a*, *b* and c_0 are random and synchronized to a global clock signal. The propagation times for both sum and carry of a full adder is t_a. The full adder is free from glitches if its inputs are synchronized. The probability that an input bit is high is 0.5 (i.e. $P(a_j=1) = P(b_j=1) = P(c_0=1) = 0.5$ where $0 \le j \le N-1$). Assume short rise and fall times of all signals.

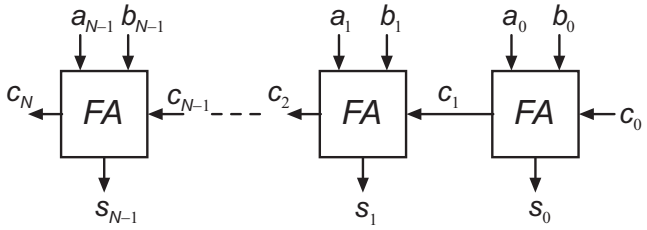

Figure 2. N-bit ripple carry adder.

a) Determine $P(s_0)$ and $P(c_1)$.

b) Assume that the signals a_j and b_j are stable and that c_j makes one transition. Determine the probability of a transition for s_j and c_{j+1}, respectively.

c) Determine the transition activity of s_j and c_{j+1} when *a*, *b* and c_0 are random and synchronized to a global clock signal.

d) The propagation delay of a 16-bits ripple carry adder is due to pipelining decreased from $16t_a$ to $4t_a + t_D$ where t_D is the propagation delay of one D flip-flop. Sketch how the pipelining is implemented

Exercise 4

The circuit in Figure 3 realizes the logic function $F = AC + BC$. Even with identical gates the circuit can produce undesired glitches at the output node F. For example assume $A = B = C = 1$. At this stage the output $F = 1$. If C goes low, the output F can make an undesired transition $1 \rightarrow 0 \rightarrow 1$ due to the finite propagation time of the inverter that generates C. Redesign the circuit so that a logic transition on one of the inputs will not cause glitches at the output.

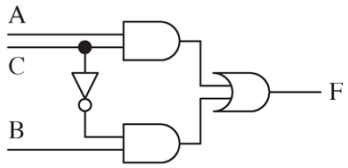

Figure 3. Digital circuit.

Exercise 5

Design a digital circuit according to Table 1 where the output signal must be glitch free for single input changes.

ab\cd	**00**	**01**	**11**	**10**
00	1	1	1	1
01	0	1	-	-
11	0	1	1	0
10	0	-	0	0

Table 1: Truth table for the digital circuits.

Exercise 6

a) Determine the transition activity α_f of the output node of a static CMOS NAND gate where the two input signals a and b has the transition activities α_a and α_b, respectively ($P(a) = P(b) = 1/2$). Assume that the input signals are outputs from a register.

b) Calculate the transition activity at the output node for the four cases below.

1) $\alpha_a = \alpha_b = 1/2$, 2) $\alpha_a = \alpha_b = 1/4$, 3) $\alpha_a = 1/2$, $\alpha_b = 1/4$, 4) $\alpha_a = 0$

c) Is the answer in the fourth case in b) reasonable?

Exercise 7

In the dashed box in Figure 4 a precharged gate is shown. The input capacitances of this gate are estimated to C_A, C_B and C_C, respectively and the output capacitance is estimated to C_F. *A* and *B* are uncorrelated. During the precharge phase *A* and *B* are always zero. During the evaluation phase $P(A=1) = 0.64$ and $P(B=1) = 0.35$.

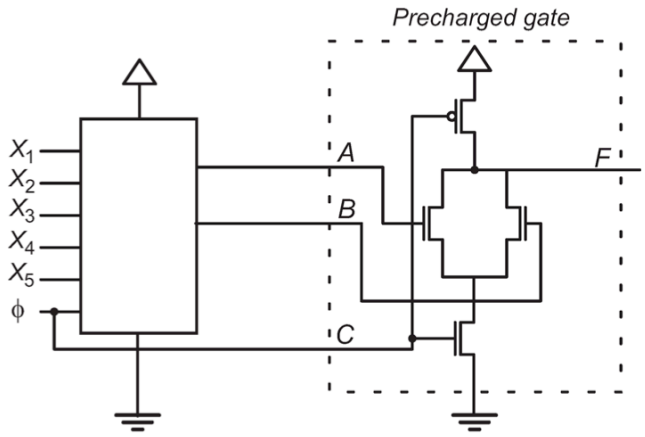

Figure 4. Precharged gate.

a) Determine the transition activity α_F.

b) Determine the transition activities α_A, α_B and α_C.

c) Determine the switching activity *a* and the switched capacitance C_{sw}.

d) Determine the power consumption and explain where and how the energy is dissipated.

e) Determine the power consumption when *A* and *B* are constants.

f) Compare the results with Exercise 6.

Exercise 8

A logic circuit is shown in Figure 5. Determine the power consumption due to charging and discharging of the capacitors C_a, C_b, C_c, C_x and C_F associated with nodes *a*, *b*, *c*, *x*, and *F*. Assume static CMOS logic and a power supply of V_{DD}. The input signals are glitch free, uncorrelated, and random, the clock frequency is *f* and the supply voltage is V_{DD}. $P(a=1) = 0.4$, $P(b=1) = 0.5$, $P(c=1) = 0.6$.

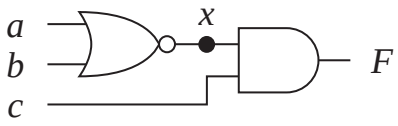

Figure 5. Logic circuit.

a) Solve the problem assuming a zero-delay model.

b) Solve the problem assuming a unit-delay model.

Solution 1

a) Glitches are unwanted transitions that may occur before the signal settles to its intended value.

b) By delay balancing of input signals (see exercise 2).
By adding redundant logic (see exercise 4).
Shorten the logic depth of combinational logic by registers.

Solution 2

a)

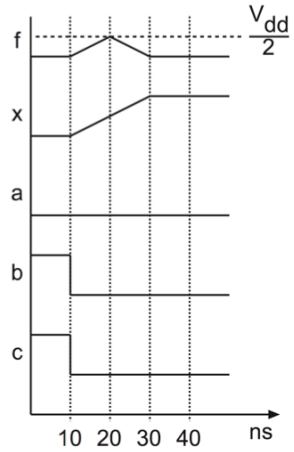

Figure 6. Glitch in node f.

b) $E = \frac{V_{dd}^2 C_L}{2} + \frac{V_{dd}^2 C_L}{2} = V_{dd}^2 C_L$

c)

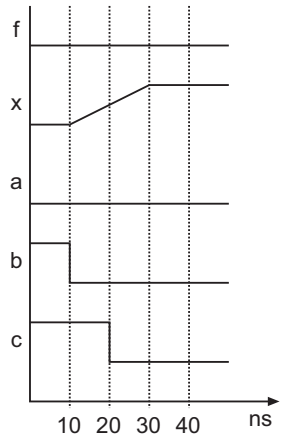

Figure 7. Glitch eliminated.

$E = \frac{V_{dd}^2 C_L}{2}$

Solution 3

a) $P(s_0) = P(c_1) = 1/2$

b) Truth table for analyzing carry transitions:

$a_j\, b_j$	c_{j+1}	s_j	P_{state}
00	0	c_j	1/4
01	c_j	c_j'	1/4
10	c_j	c_j'	1/4
11	1	c_j	1/4

P("$\boldsymbol{s_j}$ makes one transition when $\boldsymbol{c_j}$ makes one transition") = 1
P("$\boldsymbol{c_{j+1}}$ makes one transition when $\boldsymbol{c_j}$ makes one transition") = 1/4+1/4 = 1/2

c) When inputs a_j and b_j get new values, input c_j keeps its old value during the delay time of one FA ($j \geq 1$). Table with state transitions due to update of inputs a_j and b_j:

c_j	$a_j\, b_j$	c_{j+1}	s_j	P_{state}
0	00→00	0→0	0→0	1/32
0	00→01	0→0	**0→1**	1/32
0	00→10	0→0	**0→1**	1/32
0	00→11	**0→1**	0→0	1/32
0	01→00	0→0	**1→0**	1/32
0	01→01	0→0	1→1	1/32
0	01→10	0→0	1→1	1/32
0	01→11	**0→1**	**1→0**	1/32
0	10→00	0→0	**1→0**	1/32
0	10→01	0→0	1→1	1/32
0	10→10	0→0	1→1	1/32
0	10→11	**0→1**	**1→0**	1/32
0	11→00	**1→0**	0→0	1/32
0	11→01	**1→0**	**0→1**	1/32
0	11→10	**1→0**	**0→1**	1/32
0	11→11	1→1	0→0	1/32

c_j	$a_j\, b_j$	c_{j+1}	s_{j+1}	P_{state}
1	00→00	0→0	1→1	1/32
1	00→01	**0→1**	**1→0**	1/32
1	00→10	**0→1**	**1→0**	1/32
1	00→11	**0→1**	1→1	1/32
1	01→00	**1→0**	**0→1**	1/32
1	01→01	1→1	0→0	1/32
1	01→10	1→1	0→0	1/32
1	01→11	1→1	**0→1**	1/32
1	10→00	**1→0**	**0→1**	1/32
1	10→01	1→1	0→0	1/32
1	10→10	1→1	0→0	1/32
1	10→11	1→1	**0→1**	1/32
1	11→00	**1→0**	1→1	1/32
1	11→01	1→1	**1→0**	1/32
1	11→10	1→1	**1→0**	1/32
1	11→11	1→1	1→1	1/32

Determine the transition activities for the output considering that the carry input is not changed until after t_{FA}

$$\alpha_{C_1} = P\left(\overline{C_1}\right)P\left(C_1\right) + P\left(C_1\right)P\left(\overline{C_1}\right) = \frac{1}{2}$$

$$\alpha_{C_2} = \frac{3}{8} + \frac{\alpha_{C_1}}{2} = \frac{3}{8} + \frac{1}{2}\cdot\frac{1}{2}$$

$$\alpha_{C_3} = \frac{3}{8} + \frac{\alpha_{C_2}}{2} = \frac{3}{8}\left(1+\frac{1}{2}\right) + \frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{2}$$

$$\alpha_{C_4} = \frac{3}{8} + \frac{\alpha_{C_3}}{2} = \frac{3}{8}\left(1+\frac{1}{2}+\frac{1}{4}\right) + \frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{2}\cdot\frac{1}{2}$$

$$\alpha_{C_j} = \frac{3}{8}\sum_{i=0}^{j-1}\frac{1}{2^i} + \frac{1}{2^j} = \frac{3}{8}\cdot 2\left(1-2^{-j}\right) + 2^{-j} = \frac{3+2^{-j}}{4}$$

$$\alpha_{S_0} = P\left(\overline{S_0}\right)P\left(S_0\right) + P\left(S_0\right)P\left(\overline{S_0}\right) = \frac{1}{2},\ \alpha_{S_j} = \frac{1}{2} + 1 \cdot \alpha_{C_j} = \frac{5 + 2^{-j}}{4}$$

Answer: $\alpha_{S_j} = \frac{5 + 2^{-j}}{4}$ and $\alpha_{C_j} = \frac{3 + 2^{-j}}{4}$ for $j \geq 1$

Solution 4

A glitch-free realization of *F* when one of *A*, *B*, and *C* is changed is shown below.

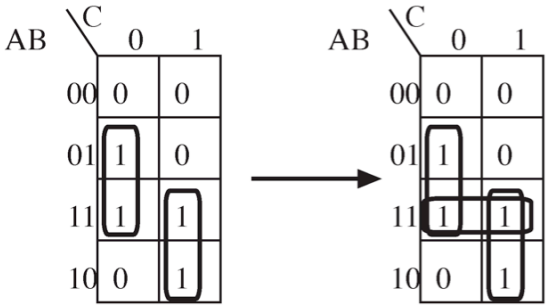

Figure 8. Carnaugh maps.

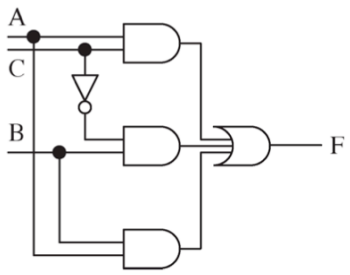

Figure 9. A glitch-free circuit using redundant logic.

Solution 5

The two areas marked by solid lines (two prime implicants) in Truth table for the digital circuits. are enough to realize the desired function ($f = (a \cdot \overline{b}) + (b \cdot d)$), but a change of the input signals from (*a*, *b*, *c*, *d*) = (0, 1, 0, 1) to (*a*, *b*, *c*, *d*) = (0, 0, 0, 1) is not within any marked area. This means that we can not guarantee that the output signal is glitch free for a single input change.

ab\cd	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

Table 2. Karnaugh map.

The digital circuit is glitch free if the input signals starts and ends in the same marked area. In Table 3 three areas is marked (three prime implicants) corresponding to $f = (\bar{a} \cdot \bar{b}) + (b \cdot d) + (\bar{a} \cdot d)$. With this solution, a single input change can not produce a glitch. The digital circuit is shown in Figure 10.

ab\cd	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

Table 3: Karnaugh map.

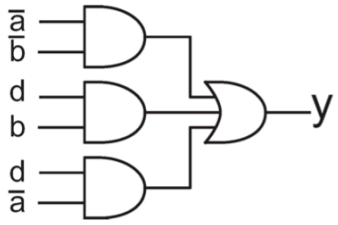

Figure 10. Two complementary bit lines.

Solution 6

a) $\alpha_a = \alpha_{a(01)} + \alpha_{a(10)}$
$\alpha_b = \alpha_{b(01)} + \alpha_{b(10)}$

Let $P\{(a_j, b_j) \rightarrow (a_{j+1}, b_{j+1})\}$ denote the probability of the scenario $(a_j, b_j) \rightarrow (a_{j+1}, b_{j+1})$

There are six scenarios which results in a transition at the output $f = \overline{ab}$

$P\{(0,0) \rightarrow (1,1)\} = \alpha_{a(01)}\alpha_{b(01)}$
$P\{(0,1) \rightarrow (1,1)\} = \alpha_{a(01)}\alpha_{b(11)}$
$P\{(1,0) \rightarrow (1,1)\} = \alpha_{a(11)}\alpha_{b(01)}$
$P\{(1,1) \rightarrow (0,0)\} = \alpha_{a(10)}\alpha_{b(10)}$
$P\{(1,1) \rightarrow (0,1)\} = \alpha_{a(10)}\alpha_{b(11)}$
$P\{(1,1) \rightarrow (1,0)\} = \alpha_{a(11)}\alpha_{b(10)}$

$$\alpha_f = \alpha_{f(01)} + \alpha_{f(10)} = 2\left(\frac{\alpha_a\alpha_b}{4} + \frac{\alpha_a(1-\alpha_b)}{4} + \frac{\alpha_b(1-\alpha_a)}{4}\right)$$

$$\alpha_f = \frac{1}{2}(\alpha_a + \alpha_b - \alpha_a\alpha_b)$$

b) 3/8, 7/32, 5/16, $a_b/2$

c) $\alpha_a = 0$ means that a is constantly equal to 0 or 1. $P(a{=}1) = P(a{=}0) = 0.5$

$a = 0 \Rightarrow \alpha_f = 0$

$a = 1 \Rightarrow \alpha_f = \alpha_b$

The probability of $\alpha_f = 0$ is 1/2 and the probability of $\alpha_f = \alpha_b$ is also 1/2.

Hence, the expected value of the transition activity: $\alpha_f = \frac{0 + \alpha_b}{2} = \alpha_b / 2$

Solution 7

a) Transition activity $\alpha_F = \alpha_{F01} + \alpha_{F10}$

$P(A{=}1) = 0.64$, $P(B{=}1) = 0.35 \Rightarrow P(A{=}0) = 0.36$, $P(B{=}0) = 0.65$

F is always one at the end of the precharge phase. In Table 4 the probability of the four possible states, at the end of the evaluation phase, are listed.

State (AB)	F	Probability
00	1	$0.36 \cdot 0.65 = 0.234$
01	0	$0.36 \cdot 0.35 = 0.126$
10	0	$0.64 \cdot 0.65 = 0.416$
11	0	$0.64 \cdot 0.35 = 0.224$

Table 4: Two uncorrelated bit lines.

Assume that F is precharged to 1. During the evaluation phase the probability of F being discharged to 0 is $0.126 + 0.416 + 0.224 = 0.766$. If F is discharged to 0 it will then be charged to 1 during the next precharge phase. Hence, if F is discharged it will make two transitions during one clock cycle (see Figure 11).

Hence, $\alpha_F = \alpha_{F10} + \alpha_{F01} = 0.766(1 + 1) = 1.532 \approx 1.53$.

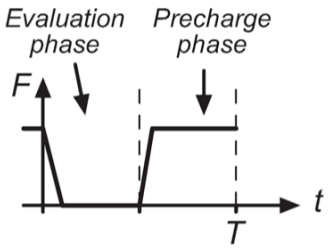

Figure 11. Discharge and charge of F.

b) $\alpha_{A01} = 1 \cdot 0.64 = 0.64$, $\alpha_{A10} = 0.64 \cdot 1 = 0.64 \Rightarrow \alpha_A = \alpha_{A01} + \alpha_{A10} = 1.28$
$\alpha_{B01} = 1 \cdot 0.35 = 0.35$, $\alpha_{B10} = 0.35 \cdot 1 = 0.35 \Rightarrow \alpha_A = \alpha_{A01} + \alpha_{A10} = 0.70$
$\alpha_C = \alpha_{C01} + \alpha_{C10} = 2$

c) $$a = \frac{\sum_i \alpha_{i01} C_i}{\sum_i C_i} = \frac{\alpha_{A01}C_A + \alpha_{B01}C_B + \alpha_{C01}C_C + \alpha_{F01}C_F}{C_A + C_B + C_C + C_F} =$$

$$\frac{0.64C_A + 0.35C_B + C_C + 0.766C_F}{C_A + C_B + C_C + C_F}$$

d) $$C_{sw} = a\sum_i C_i = 0.64C_A + 0.35C_B + C_C + 0.766C_F$$

$$P = faCV_{dd}^2 = f(0.64C_A + 0.35C_B + C_C + 0.766C_F)V_{dd}^2$$

When a signal is rising, energy is dissipated as heat in the p-net. When a signal is falling, energy is dissipated as heat in the n-net.

e) $A = B = 0$ during the precharge phase. $A = A_0$, $B = B_0$ during evaluation phase, where A_0 and B_0 are constants.

There are four cases:

1) $AB = 00 \Rightarrow \quad P = faCV_{dd}^2 = fC_CV_{dd}^2$

2) $AB = 01 \Rightarrow \quad P = faCV_{dd}^2 = f(C_B + C_C + C_F)V_{dd}^2$

3) $AB = 10 \Rightarrow \quad P = faCV_{dd}^2 = f(C_A + C_C + C_F)V_{dd}^2$

4) $AB = 11 \Rightarrow \quad P = faCV_{dd}^2 = f(C_A + C_B + C_C + C_F)V_{dd}^2$

Solution 8

a) Assume a zero-delay model:

$$P(x) = P(\bar{a})P(\bar{b}) = (1-0.4)(1-0.5) = 0.3$$

$$P(F) = P(x)P(c) = 0.3 \cdot 0.6 = 0.18$$

$$\alpha_{a01} = [1-P(a)]P(a) = (1-0.4)\cdot 0.4 = 0.24$$

$$\alpha_{b01} = [1-P(b)]P(b) = (1-0.5)\cdot 0.5 = 0.25$$

$$\alpha_{c01} = [1-P(c)]P(c) = (1-0.6)\cdot 0.6 = 0.24$$

$$\alpha_{x01} = [1-P(x)]P(x) = (1-0.3)\cdot 0.3 = 0.21$$

$$\alpha_{F01} = [1-P(F)]P(F) = (1-0.18)\cdot 0.18 \approx 0.15$$

$$C_{sw} = C_a\alpha_{a01} + C_b\alpha_{b01} + C_c\alpha_{c01} + C_x\alpha_{x01} + C_F\alpha_{F01}$$

$$P = fV_{dd}^2C_{sw}$$

b) Introducing delay will delay x and cause glitches at the output F. The table below shows all transition cases (x', c', F'' denote a previous value, and F' a transient value):

$x'c' \rightarrow x'c \rightarrow xc$	$F'' \rightarrow F' \rightarrow F$
00→00→00	0→0→0
00→01→01	0→0→0
00→00→10	0→0→0
00→01→11	0→0→1
01→00→00	0→0→0
01→01→01	0→0→0
01→00→10	0→0→0
01→01→11	0→0→1

$x'c' \rightarrow x'c \rightarrow xc$	$F'' \rightarrow F' \rightarrow F$
10→10→00	0→0→0
10→11→01	0→1→0
10→10→10	0→0→0
10→11→11	0→1→1
11→10→00	1→0→0
11→11→01	1→1→0
11→10→10	1→0→0
11→11→11	1→1→1

From the table it can be seen that there will be a glitch for the case $x'c' \rightarrow xc$ = 10→01. The probability for this state is

$$P(\text{glitch}) = P(x)P(\bar{c})P(\bar{x})P(c) = 0.3(1-0.6)(1-0.3)0.6 = 0.0504 \approx 0.05$$

Adding the glitch to the switch activity yields

$$C_{sw+g} = C_{sw} + C_F P(\text{glitch}) \text{ and } P = fV_{dd}^2 C_{sw+g}$$