Ripple carry adder (RCA)

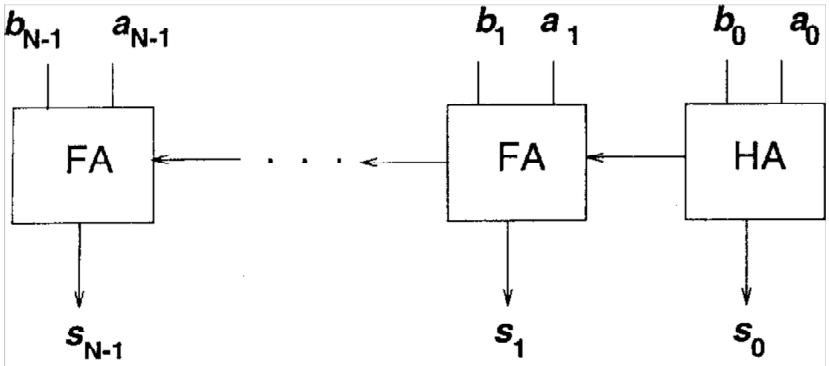
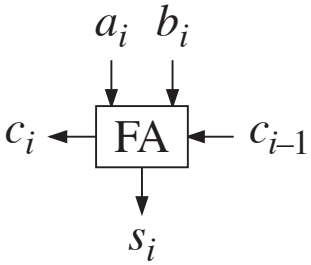


Fig. 1. Ripple carry adder.

Carry acceleration

- Consider an FA operation



- Investigate carry function

a_i	b_i	c_i	Function
0	0	0	Kill
0	1	c_{i-1}	Propagate
1	0	c_{i-1}	Propagate
1	1	1	Generate

- Rewrite carry function

$$c_i = a_i b_i + \left(a_i \oplus b_i\right) c_{i-1} = G_i + P_i c_{i-1}$$

Note that G_i and P_i do only depend on the input

Manchester carry chain adder (MCC)

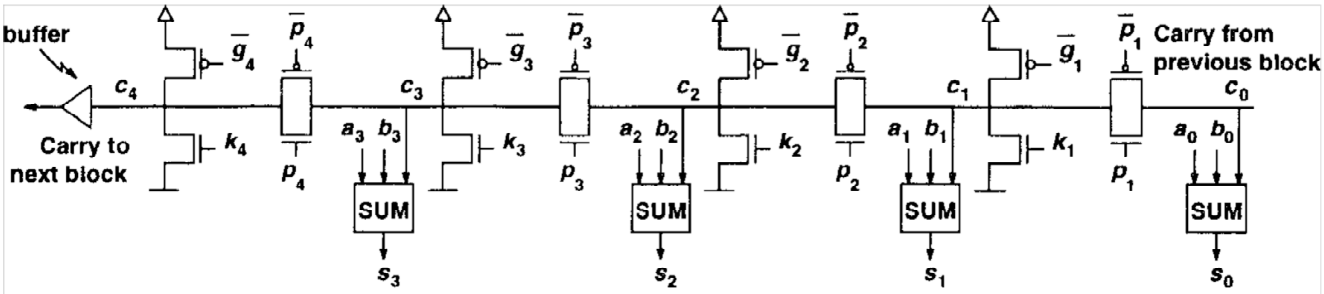


Fig. 3. A 4-b block of a Manchester Carry Chain Adder.

Carry skip adder (CSK/VSK)

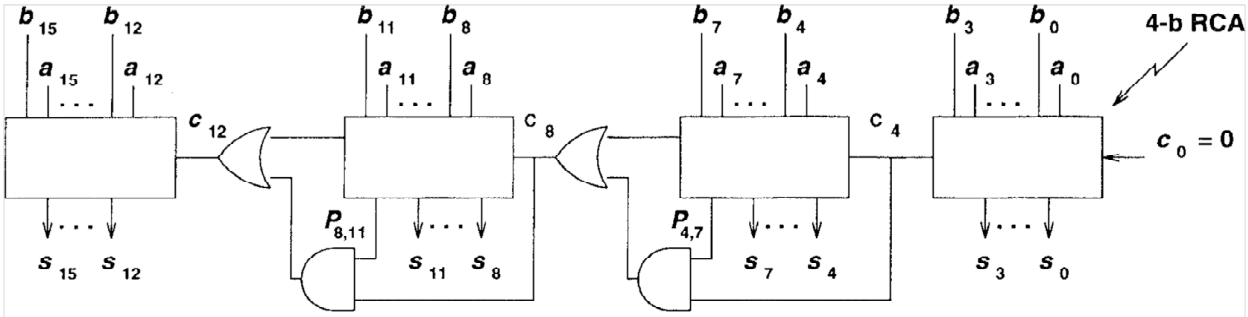


Fig. 4. A 16-b Carry Skip Adder.

Carry select adder (CSL)

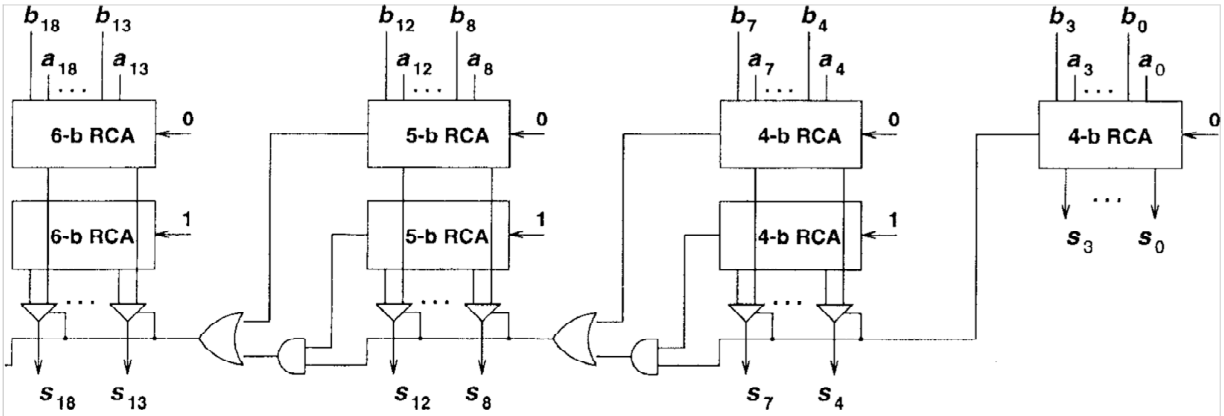


Fig. 5. A 19-b Carry Select Adder.

Carry look-ahead adder (CLA)

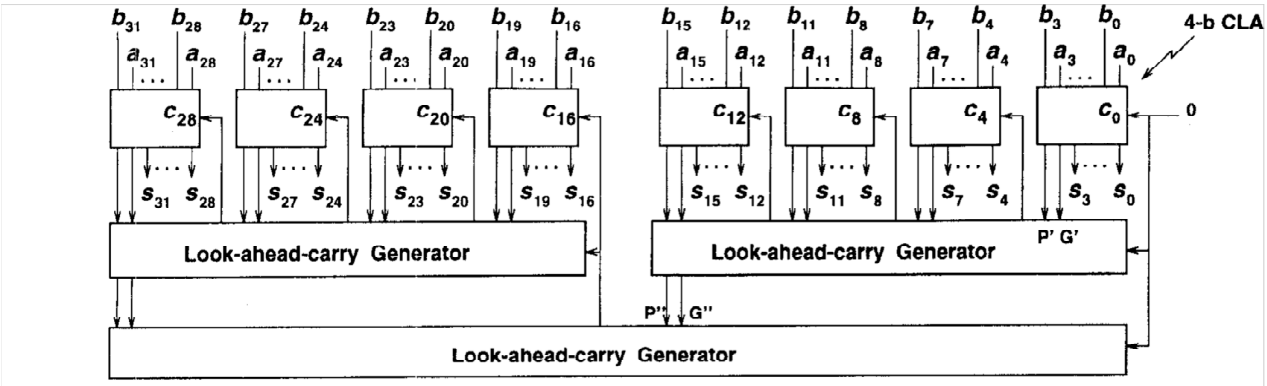


Fig. 6. A 32-b Carry Lookahead Adder.

CLA with high regularity — ELM

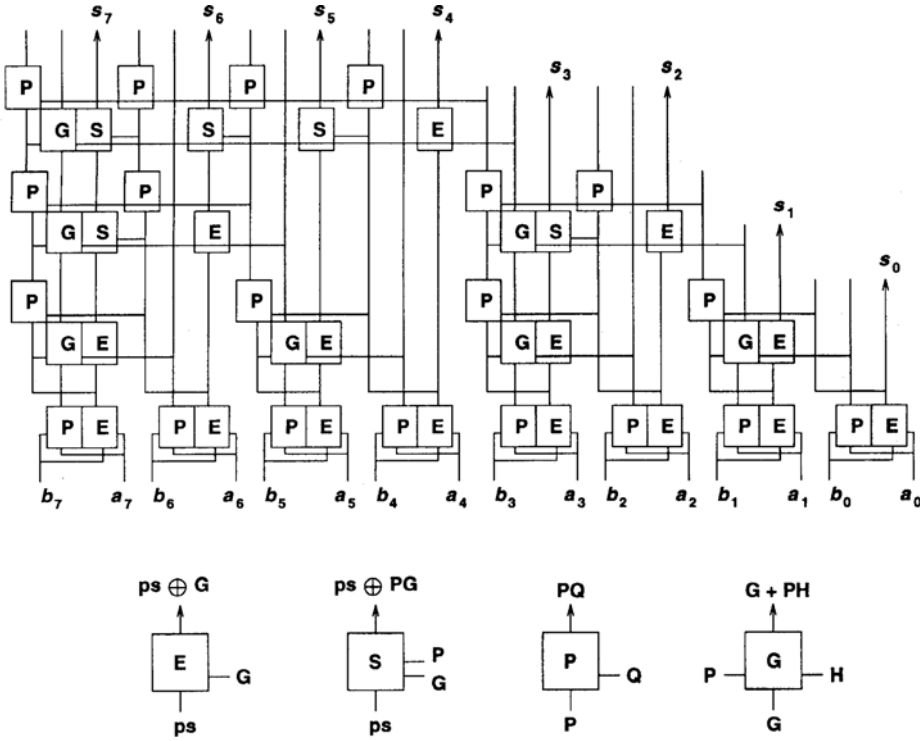


Fig. 7. An 8-b ELM adder.

Signed-digit addition

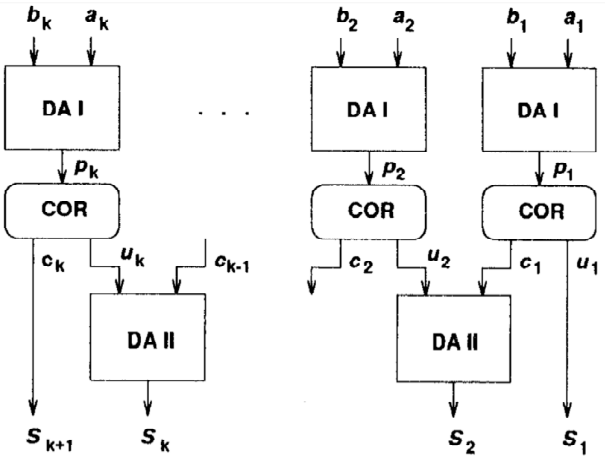
- Use a signed-digit number system with
  - digits $d_i \in \{-\alpha, \ldots, -1, 0, 1, \ldots, \alpha\}$
  - base $r \geq 3$, where
  - value $D = \sum_{i=0}^{k-1} d_i r^i$
- Addition algorithm

Signed Digit Addition (A, B, S)
For $i = 0$ to m do

1. Compute a temporary sum digit $p_i = a_i + b_i$.
2. Compute an interim sum digit u_i and a carry digit c_{i+1}: $r \cdot c_{i+1} + u_i = p_i$ such that $|u_i| \leq r - 2$ and $|c_{i+1}| \leq 1$.
3. Compute the final sum: $s_i = u_i + c_{i+1}$.

Fig. 8. The radix-r OSD addition algorithm.

Signed-digit adder (SD-r)



(a)

Base r	# digits k	# bits/digit b
128	5	8
64	6	7
32	7	6
16	8	5
8	11	4
4	16	3

n = 32 bits

(b)

Fig. 9. Signed digit adder. (a) SDA. (b) Values of k and b for different r.

Carry-save addition (CSA)

- Represent *A* with a sum vector *AS* **and** a carry vector *AC*

$$A = \sum_{i=0}^{n} (ac_i + as_i) r^i$$

- Add numbers **without** propagating the carry

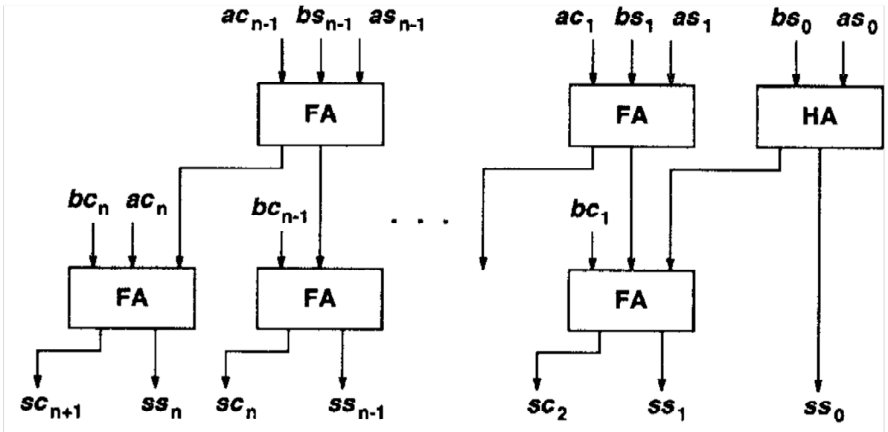


Fig. 10. Carry save adder.

Adder experiment

- Automatic layout generation for gate matrix with in-house tool
- Power estimation with HSPICE

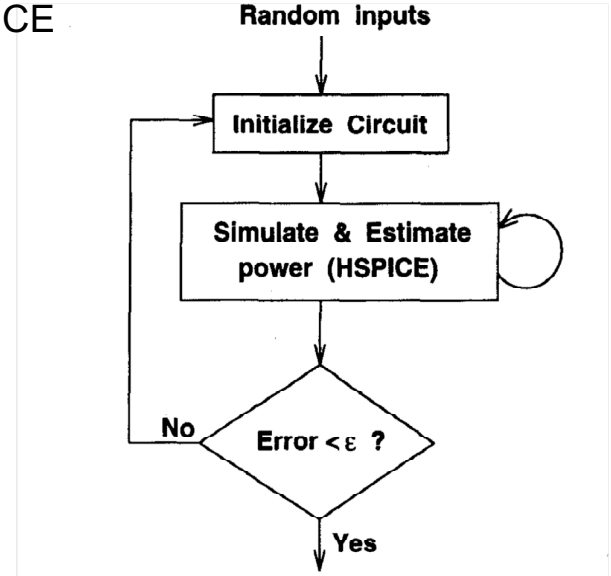


Fig. 15. Measuring average power dissipation.

Transistors and area in the adder circuits

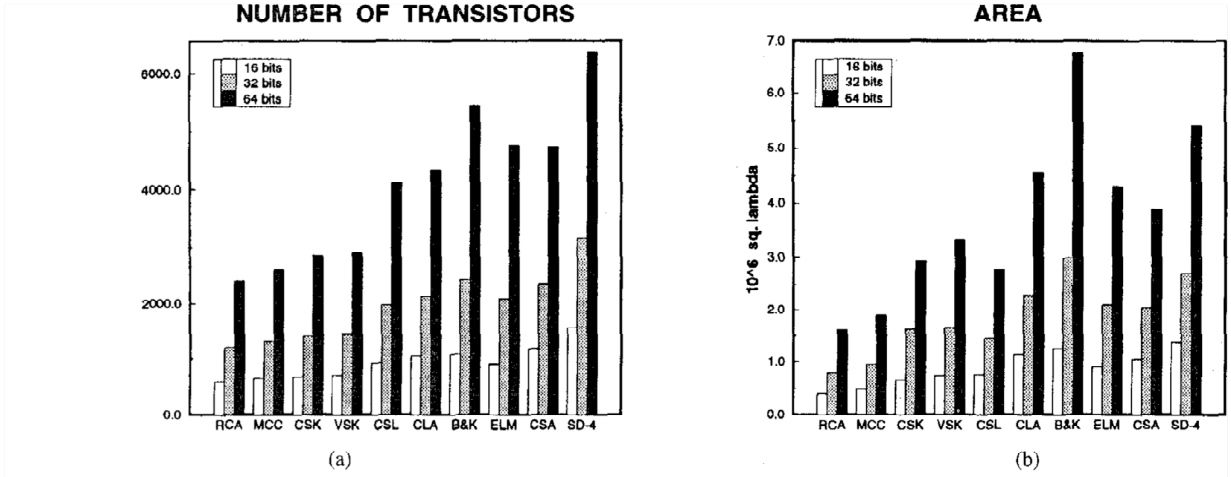
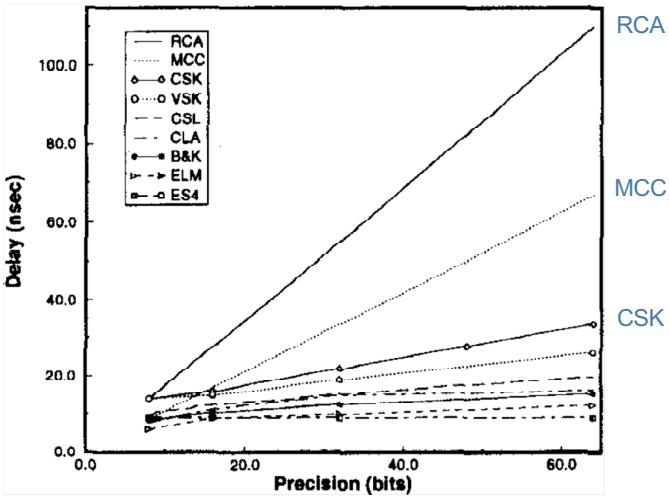
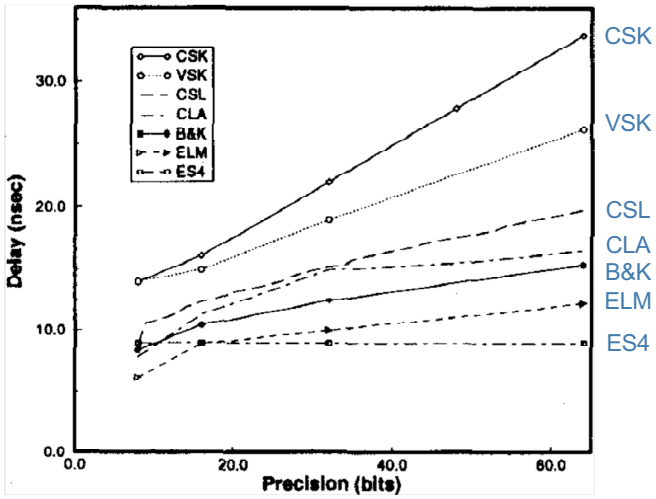


Fig. 13. (a) Number of transistors. (b) Area.

Delay of the adder circuits



RCA
MCC
CSK

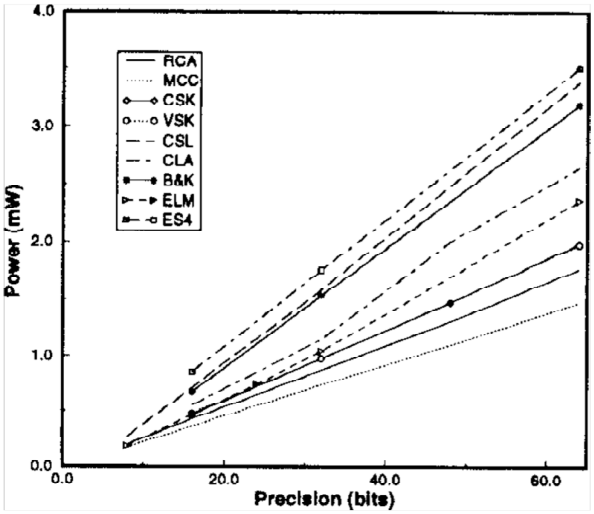


CSK
VSK
CSL
CLA
B&K
ELM
ES4

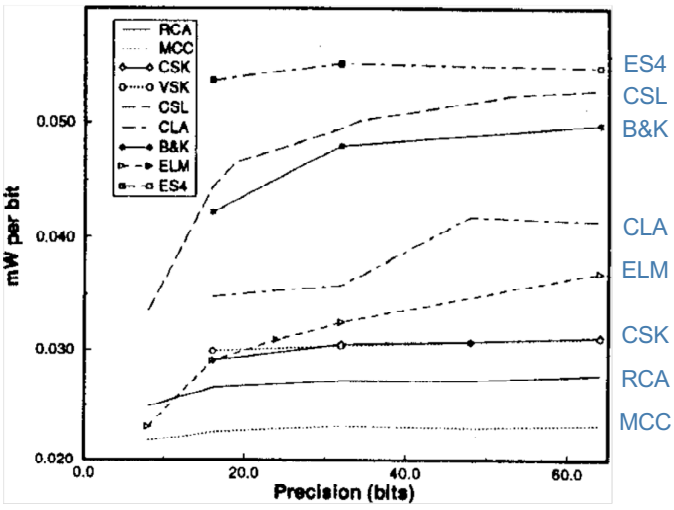
Fig. 21 (a) Delay with precision

(b) Detail of the faster adders

P consumption of the adder circuits



ES4
CSL
B&K
CLA
ELM
CSK
RCA
MCC



ES4
CSL
B&K
CLA
ELM
CSK
RCA
MCC

Fig. 21 (a) P with precision

(b) P per bit

PDP of the adder circuits

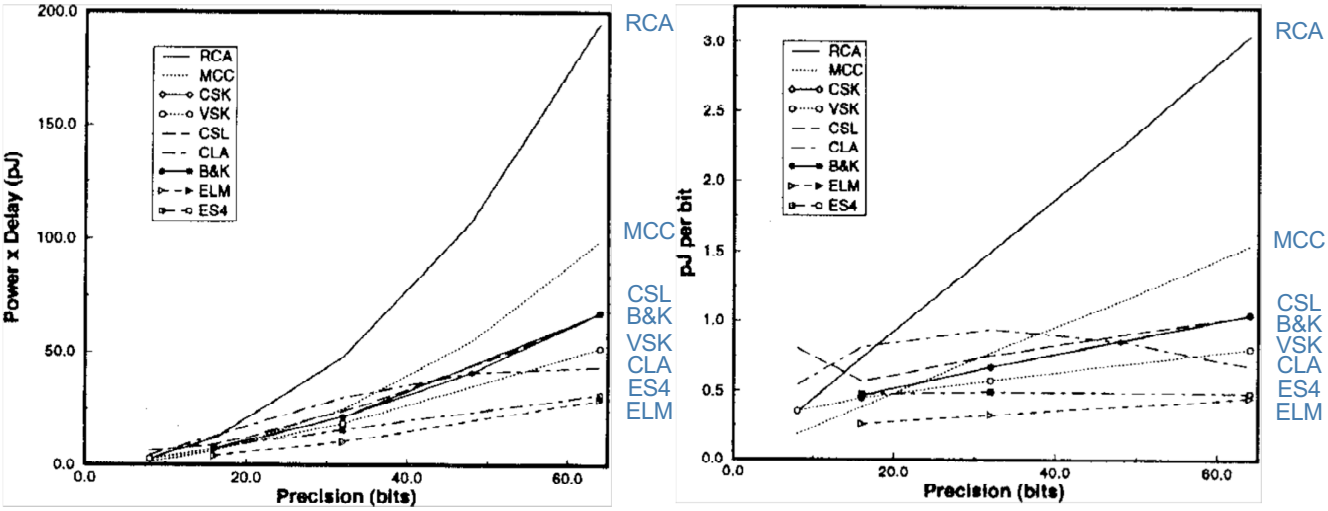


Fig. 22 (a) P*delay with precision (b) P*delay per bit

Sub-V_T leakage in memories

- Leakage in SRAM cell
- Worst case bitline leakage

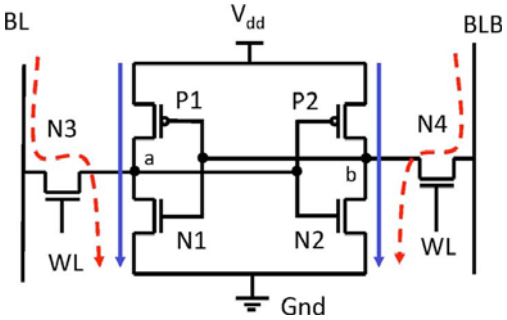


Fig. 2

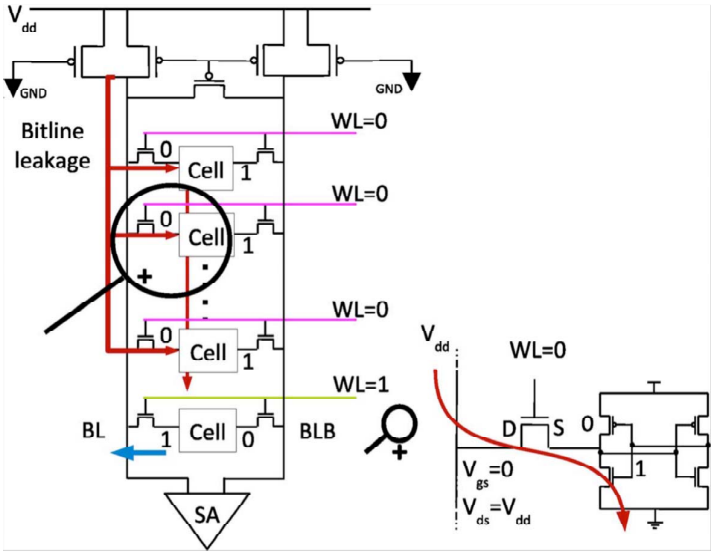


Fig. 4

Bitline design

- Precharge *BL* to low
- $V_{GS} < 0$ reduces leakage

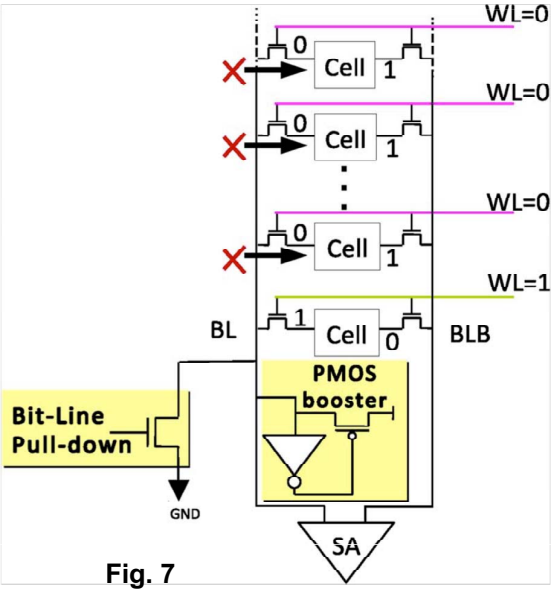


Fig. 7

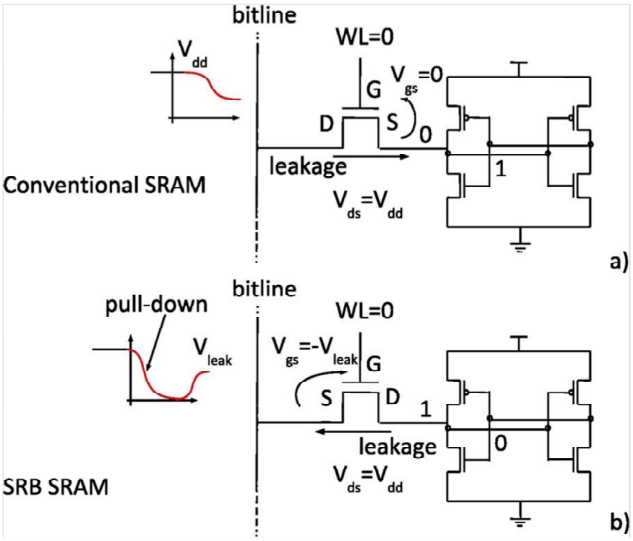


Fig. 8

Wordline design

- Negative voltage of wordline reduces leakage

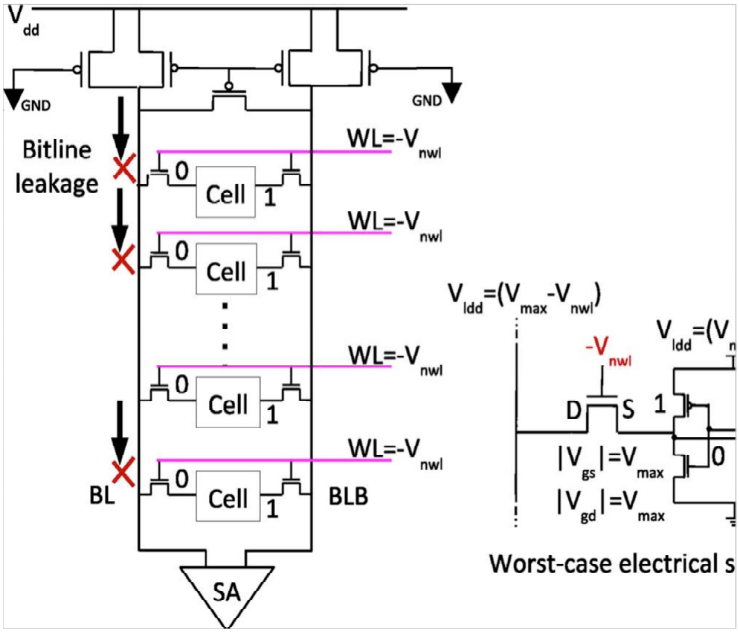


Fig. 10

Power gating

- High-V_T sleep transistor
- Dynamic voltage scaling

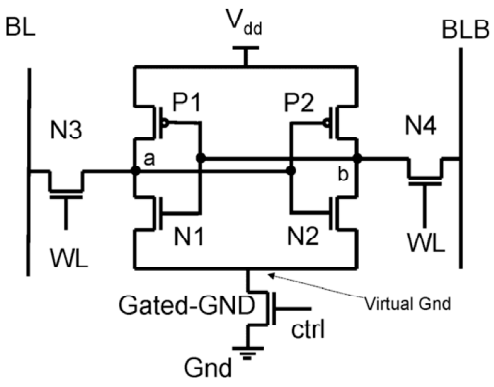


Fig. 15

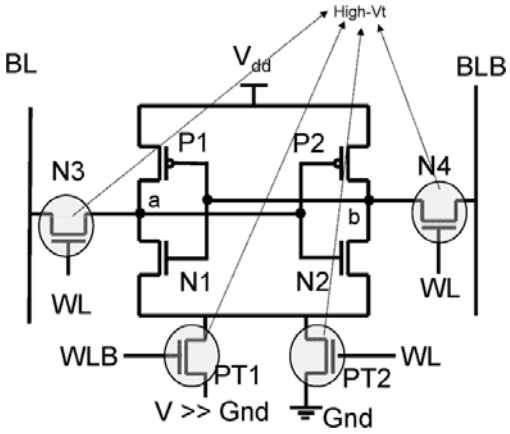


Fig. 17

Asymmetric bitcell design

- Use preferred state, e.g. 0, to reduce leakage

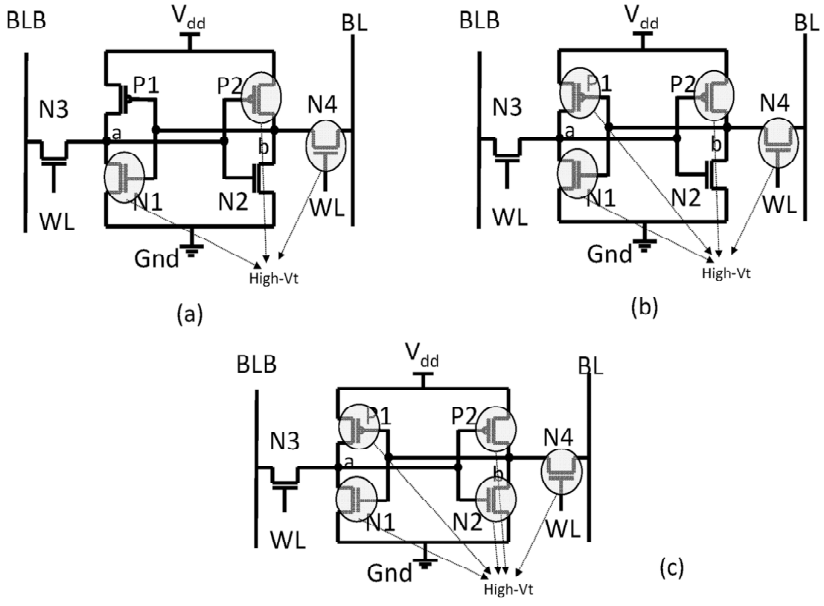


Fig. 12

SRAM cell body-bias

- Controlling V_T of SRAM cell

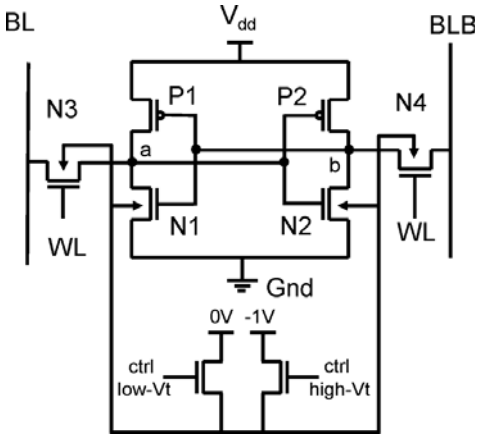


Fig. 18

Power, variability, and scalability results

- Comparison of leakage reduction strategies

Strategy	LP	Robustness	Scalability
Power gating	++	+++	+++
Body-biasing	+++	++	+
Wordline design	+	++	+++
Bitcell design	+++	+	+
Bitline design	+	+	+++
Dynamic V_{DD} scaling	++	+	+

Reorganized Table IV

Cache memory

- Resizable cache

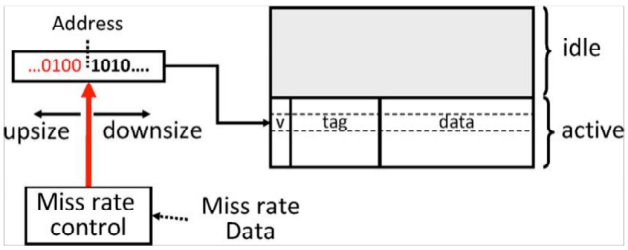


Fig. 27

- Multibank partitioning

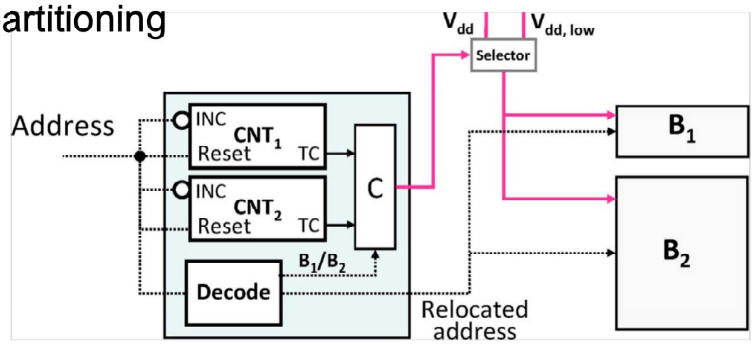


Fig. 28

Cache memory body-bias

- Controlling V_T of cache lines

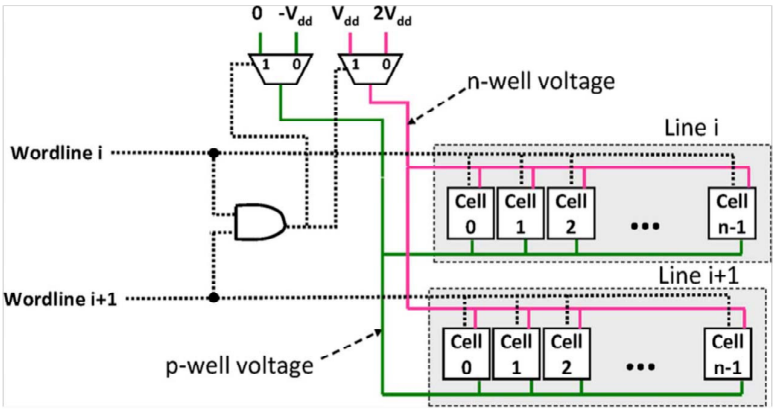


Fig. 26

References

10.pdf **Area-time-power tradeoffs in parallel adders**

C. Nagendra, M.J. Irwin, and R.M. Owens

IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, volume 43, issue 10, Oct. 1996, pages 689-702

11.pdf **Design techniques and architectures for low-leakage SRAMs**

A. Calimera, A. Macii, E. Macii, and M. Poncino

IEEE Transactions on Circuits and Systems I: Regular Papers, volume 59, issue 9, Sep. 2012, pages 1992-2007