Greatest Common Divisor (GCD) circuit

TABLE I

Block	Power Consumed (% of total)
Functional units	9.08
Random Logic	4.67
Registers	39.55
Multiplexers	46.70

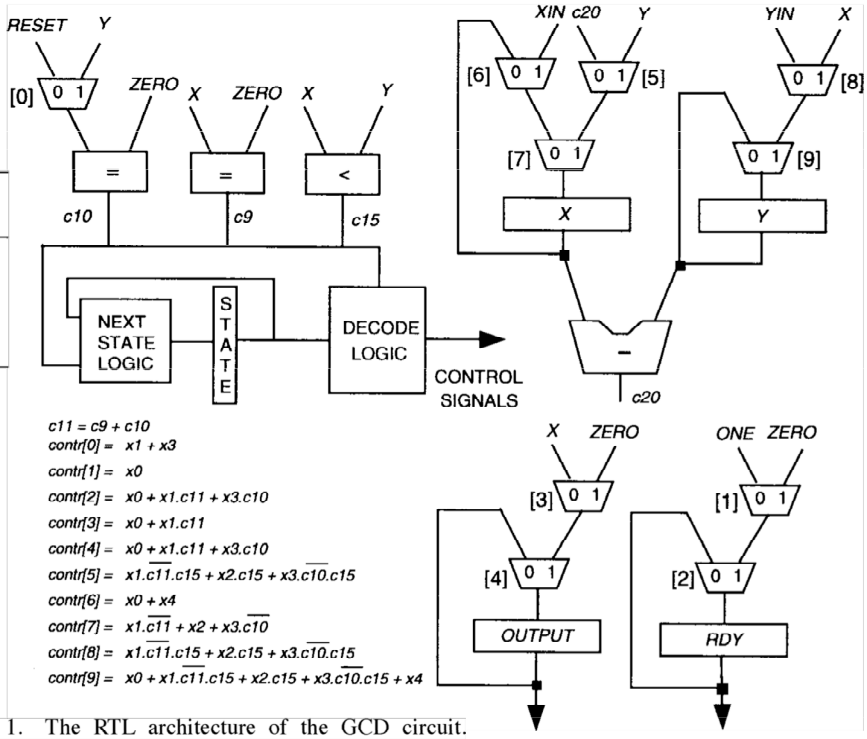


Fig. 1. The RTL architecture of the GCD circuit.

Power due to glitches in GCD

TABLE II
ACTIVITIES WITH/WITHOUT GLITCHING FOR VARIOUS SIGNALS OF THE GCD

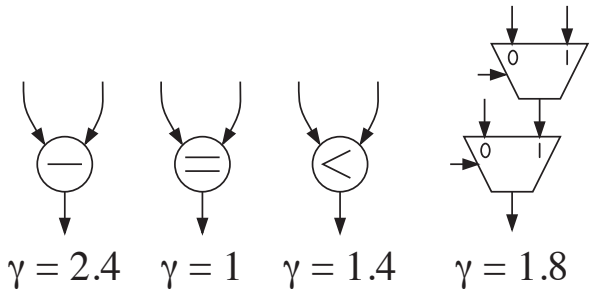
Signal	Activity	
	With Gl.	Without Gl.
Control Signals		
contr[0]	71	70.5
contr[1]	22	22
contr[2]	72	20
contr[3]	42	20
contr[4]	72	20
contr[5]	55.5	54
contr[6]	22	22
contr[7]	50	20
contr[8]	55.5	54
contr[9]	77	70.5
Data Path Signals		
*dp*2[7..0]	71.5	21.5
*dp*4[7..0]	92	26
*dp*5[7..0]	1124.5	247
*dp*7[7..0]	1044.5	273
*dp*9[7..0]	321.5	80.5

Glitch generation

- The glitch factor is (Mark's def)

$$\gamma = \frac{\#\text{ of actual transitions}}{\#\text{ of trans. with zero-delay model}}$$

- Assume ideal input in simulation of different blocks ⇒



$\gamma = 2.4$ $\gamma = 1$ $\gamma = 1.4$ $\gamma = 1.8$

Multiplexer restructuring in data path

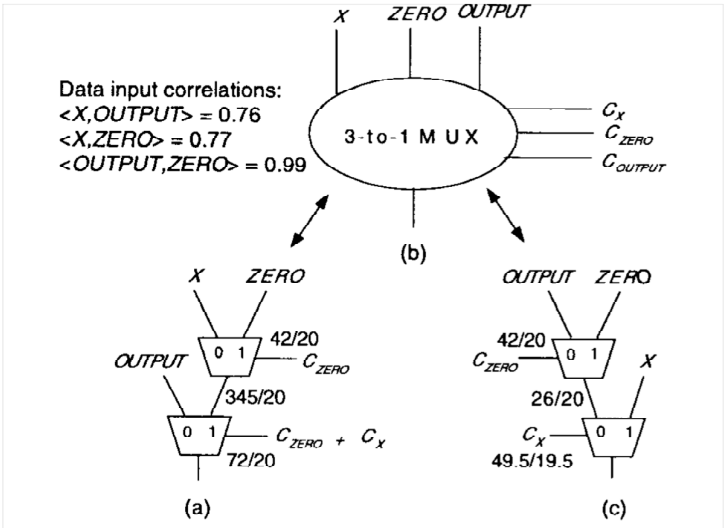
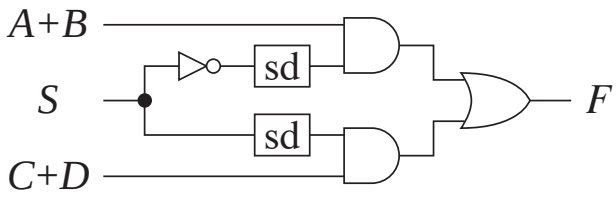


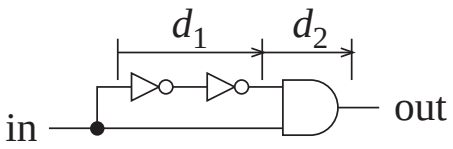
Fig. 10. Multiplexer restructuring to enhance data correlations: (a) initial multiplexer network, (b) abstract 3 : 1 multiplexer, and (c) restructured network.

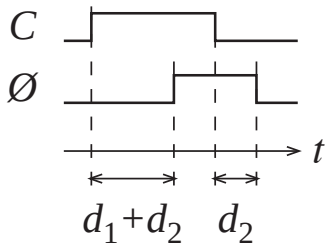
Glitch reduction in data path

- Insert selective delays (sd) in MUX to stop glitch propagation



where sd is





$\Rightarrow P' \approx 0.85P$

Multiplexer restructuring in control path

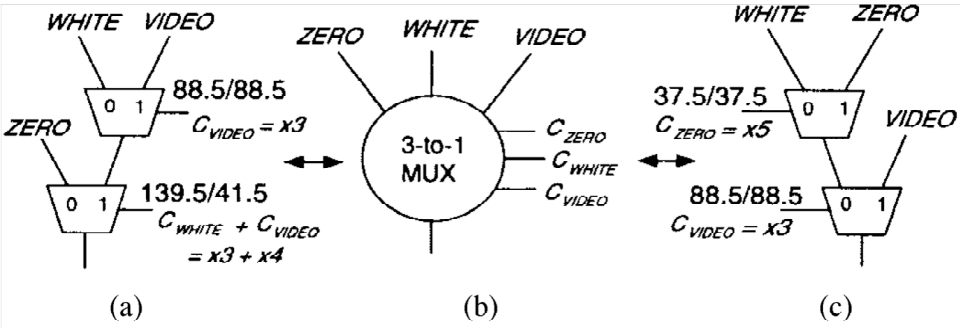
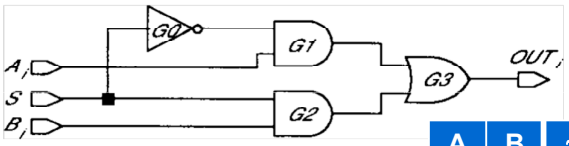


Fig. 11. Eliminating glitchy control signals: (a) initial multiplexer network, (b) abstract 3 : 1 multiplexer, and (c) restructured network.

Glitch reduction in control path

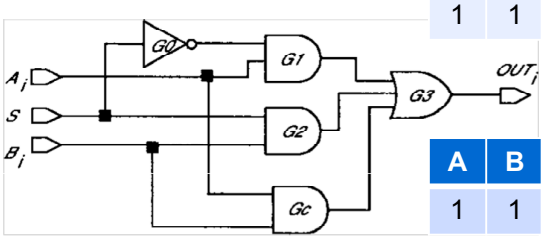
Fig. 8. Propagation of glitches on a multiplexer select signal for various values of data signals.



A	B	γ
0	0	1
0	1	3
1	0	3
1	1	7

Glitches on S ⇒

Fig. 9. Effect of adding the consensus term on glitch propagation.

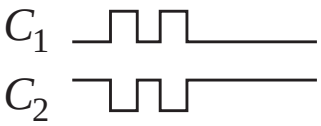


A	B	γ
1	1	1

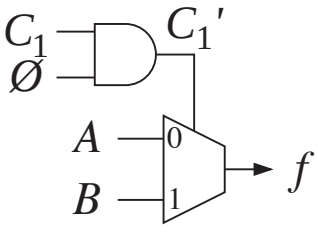
⇒ $P' \approx 0.82\,P$

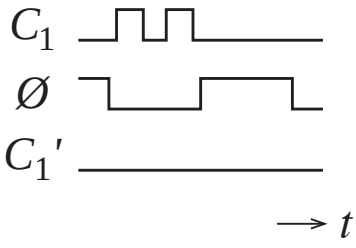
Gating control signals

- Control signals with glitches

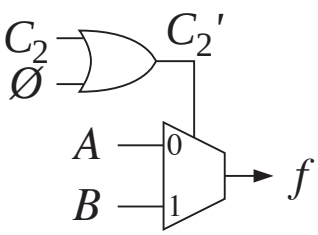


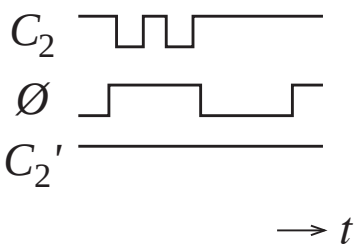
- $P(C=1)$ low





- $P(C=1)$ high





Clock gating for registers

- Find clock gating condition for register

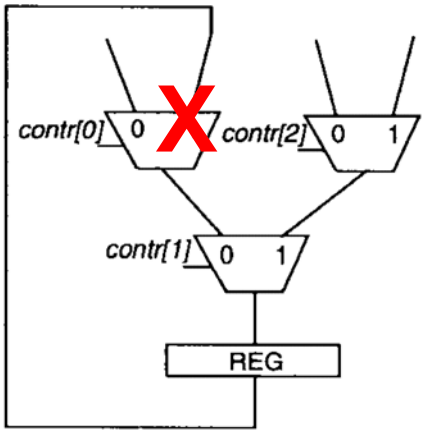


Fig. 18. Deriving clock gating conditions for registers.

$$disable = contr[0] \cdot \overline{contr[1]}$$

Optimization flow

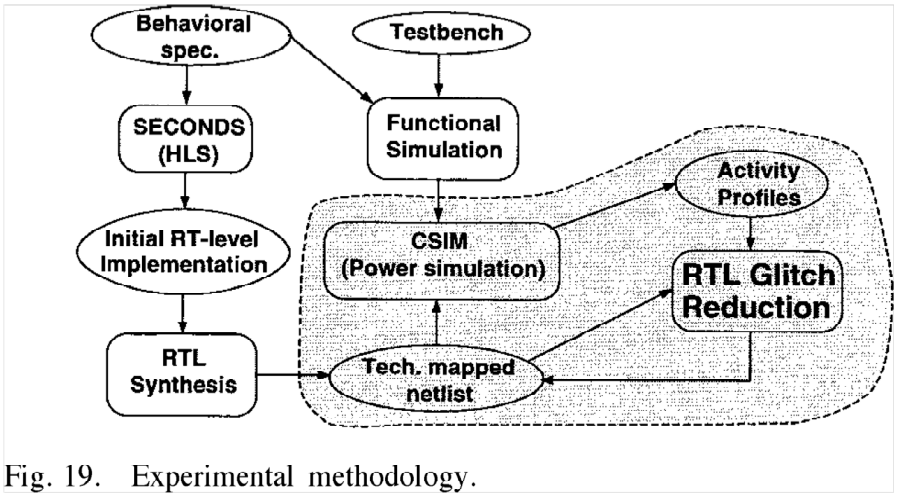


Fig. 19. Experimental methodology.

Power optimized GCD

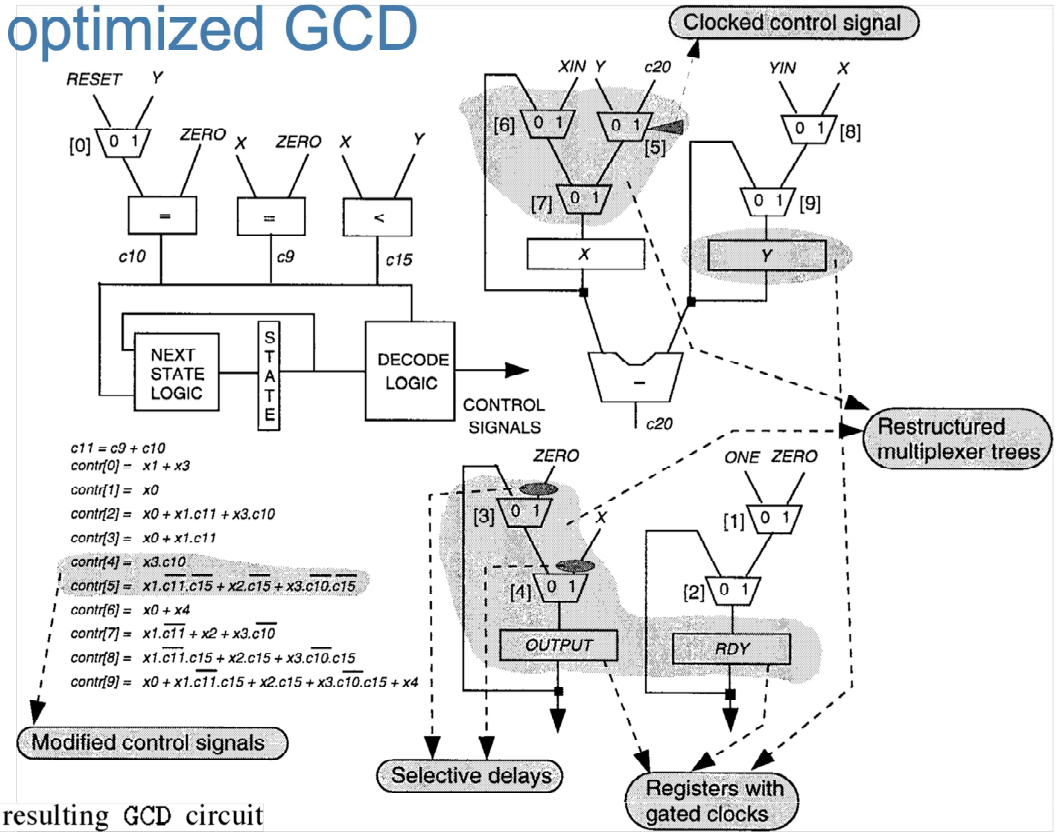


Fig. 20. The resulting GCD circuit

Experimental results

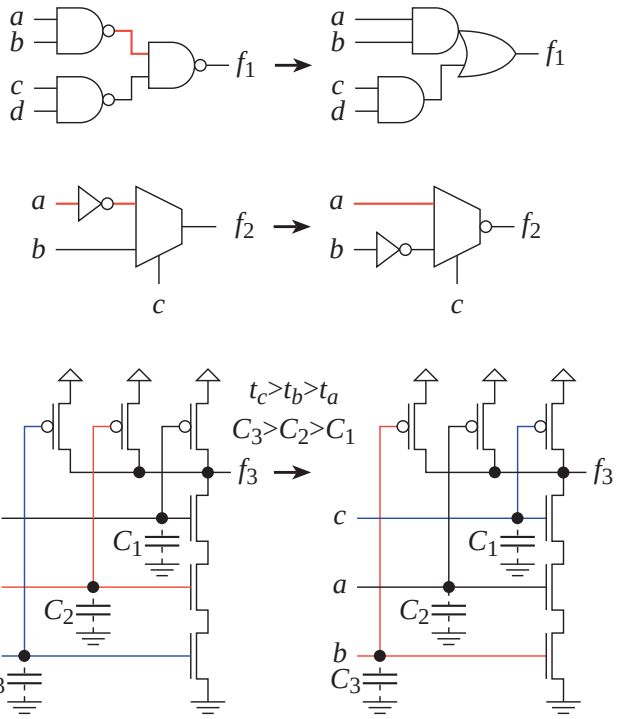
TABLE III
EXPERIMENTAL RESULTS

Circuit	Original			Optimized			Power Red. (%)	CPU
	Power	Area	Delay	Power	Area	Delay		
GCD	8.738mW	1037	32.29ns	7.229mW	1034	31.94ns	17.27%	427s
Barcode	9.409mW	1945	49.73ns	7.770mW	1968	47.29ns	17.42%	671s
UAV	10.878mW	1954	83.48ns	8.023mW	1967	83.15ns	26.25%	619s
Vendor	10.471mW	1595	70.13ns	7.725mW	1617	71.63ns	26.22%	545s
Graphics	9.653mW	3865	132.60ns	6.751mW	3914	132.68ns	30.06%	1,128s
X.25	2.056mW	2409	129.53ns	1.658mW	2434	135.11ns	19.36%	858s
Dot_Prod	19.704mW	3341	98.69ns	15.521mW	3347	97.78ns	21.23%	1,017s

Local transformations

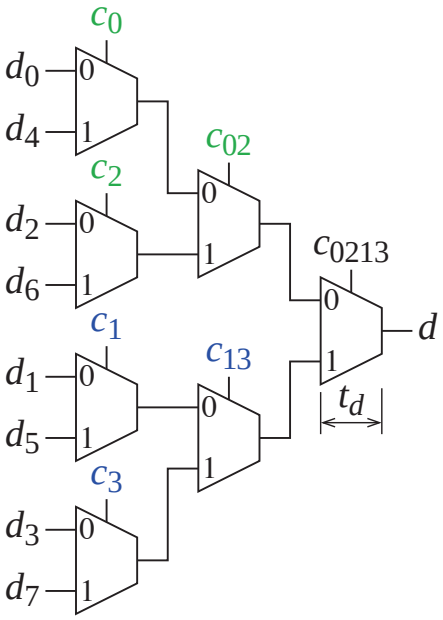
[Ben'01]

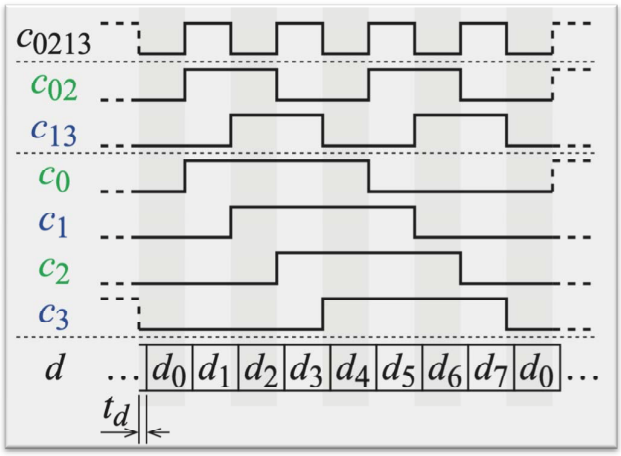
- Remapping
  - Red node has high activity
- Phase assignment
  - Red node has high activity
- Pin swapping
  - Red node has high activity
  - Blue node arrives late



Multiplexer design

- Assign control signals to minimize t_d in interleaving





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05.pdf **Register transfer level power optimization with emphasis on glitch analysis and reduction**

A. Raghunathan, S. Dey, and N.K. Jha

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, volume 18, issue 8, Aug. 1999, pages 1114-1131

[*Ben'01*] **Designing Low-Power Circuits: Practical Recipes**

L. Benini, G. De Micheli, and E. Macii

IEEE Circuits and Systems Magazine, volume 1, issue 1, 2001, pages 6-25