# Multiple voltage design

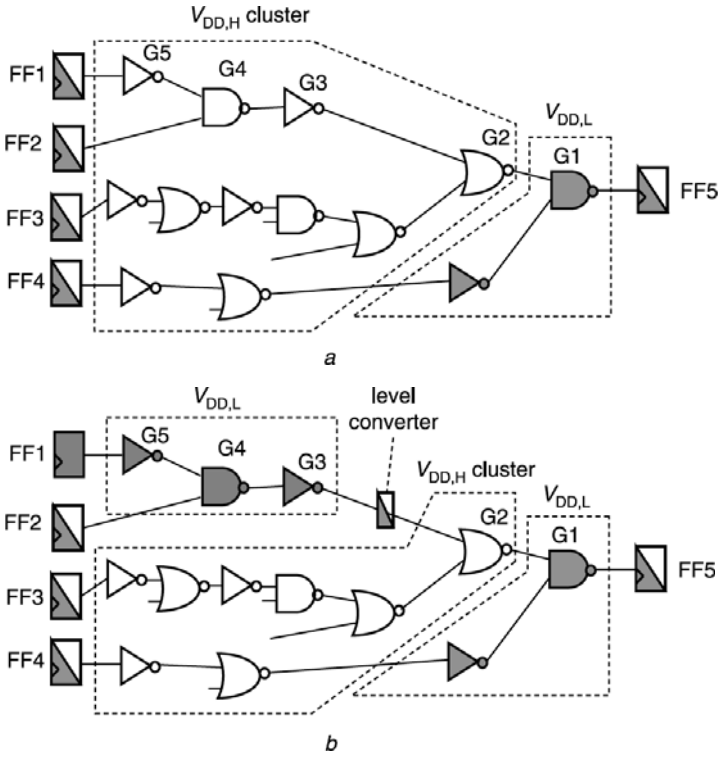



**Fig. 2** *Examples*
*a* CVS solution
*b* ECVS solution



# Level converter

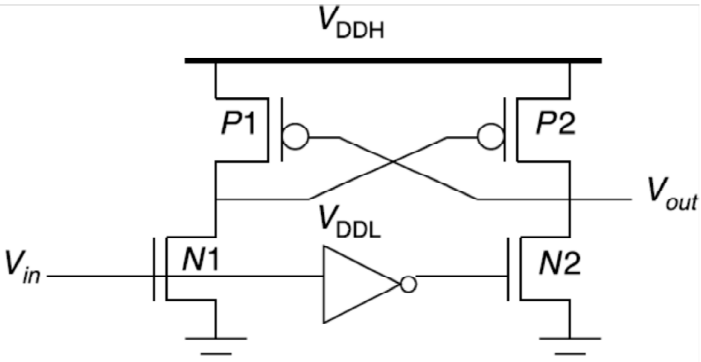



**Fig. 1** *Typical level-converter design*

# Precomputation of combinational logic

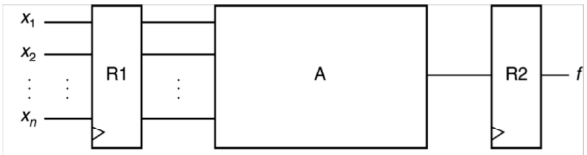



**Fig. 3** *Pipeline stage of a data path*

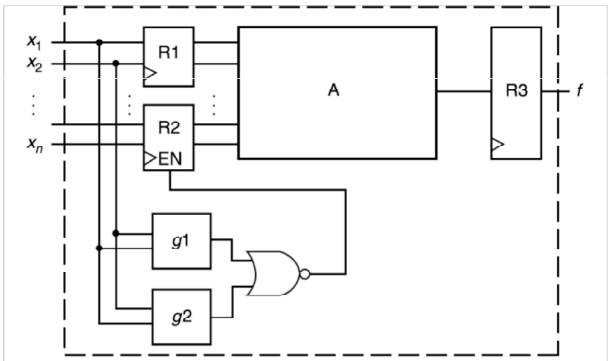



**Fig. 4** *Precomputation logic realisation of the pipeline stage (subset-input disabling architecture)*

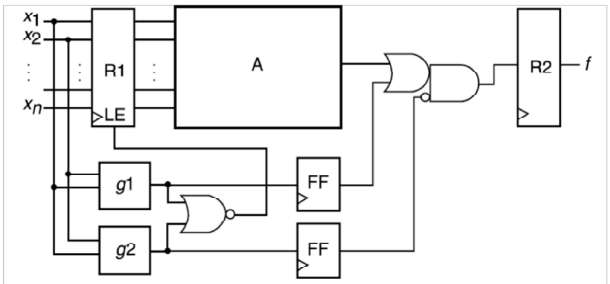



**Fig. 5** *Example of a complete input-disabling precomputation architecture*



# Precomputation enable set

- Computation of predictor functions

  Denote a logic function $f(x_0, x_1, \ldots, x_{n-1})$

  The cofactor of $f$ with respect to $x_0$ is then $f_{x0}(1, x_1, \ldots, x_{n-1})$

  The observability don't care set for input $x_0$ is $\mathrm{ODC}_{x0} = f_{x0} \cdot f_{\overline{x0}} + \overline{f_{x0}} \cdot \overline{f_{\overline{x0}}}$

  This set indicates when $x_0$ is redundant in the computation of $f$

- The loading of inputs $x_0, x_1, \ldots, x_{n-1}$ can be disabled using

$$g = \prod_{i=0}^{n-1} \mathrm{ODC}_i$$

# Clock gating

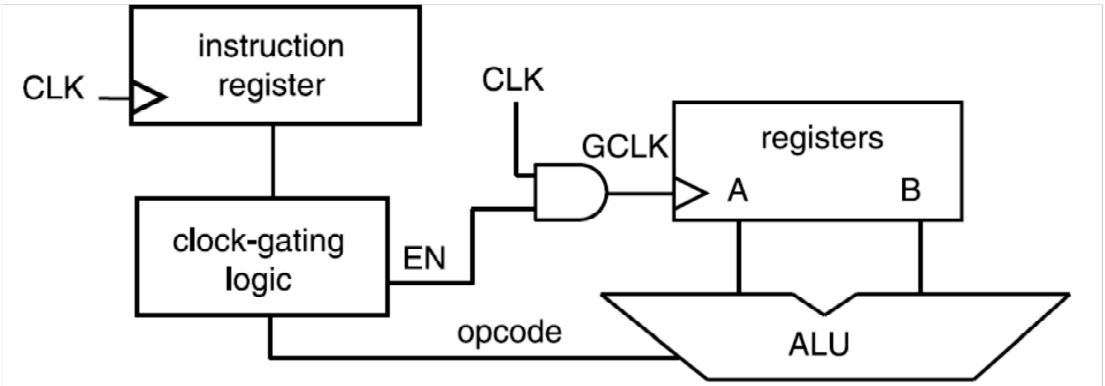



**Fig. 6** *Clock gating logic for ALU in a typical processor microarchitecture with negative-edge triggered flip-flops*



# Disabling clock

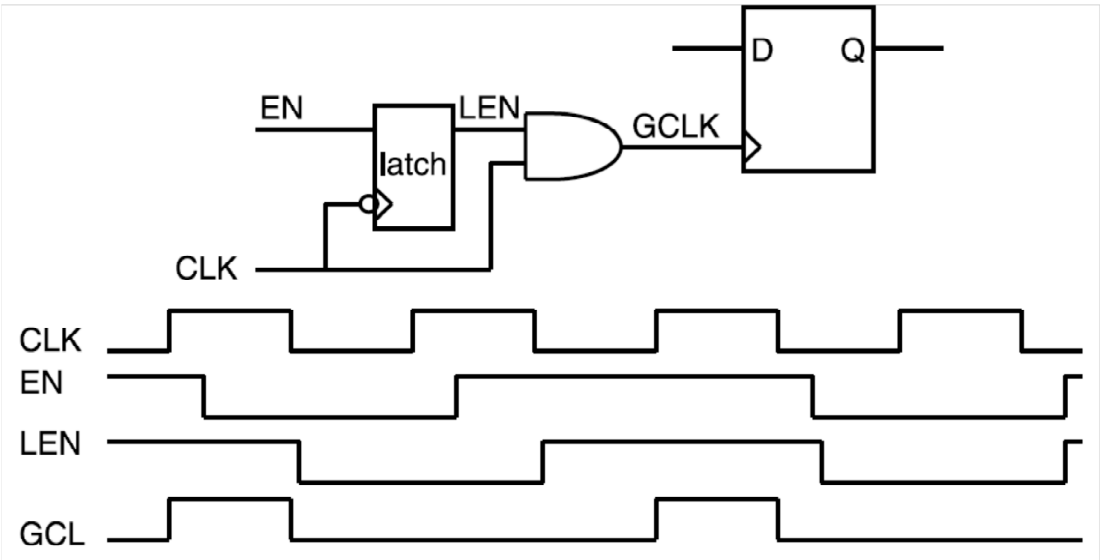



**Fig. 7** *Clock is disabled when EN = 0; furthermore, a hazard on EN will be stopped from reaching GCLK*

# Computational FSM kernels

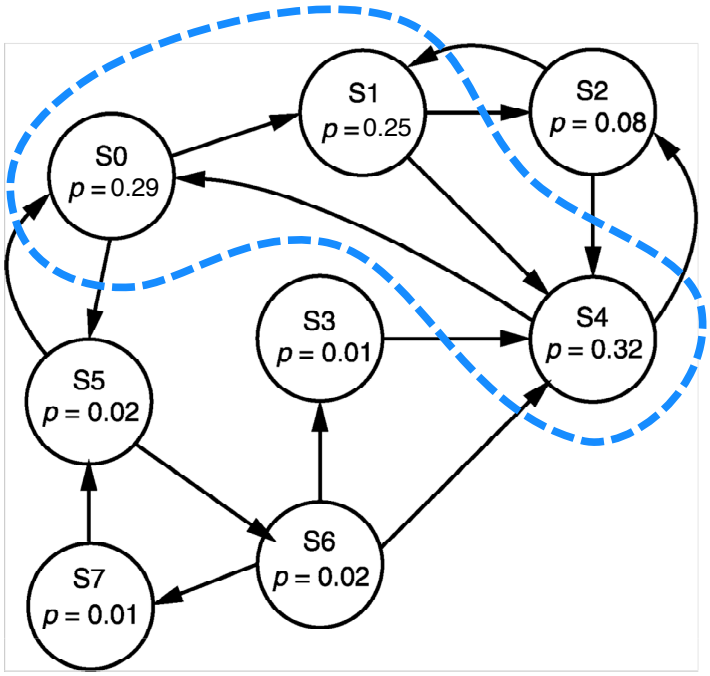



**Fig. 8** *Moore-type FSM*



# Kernel-based optimization

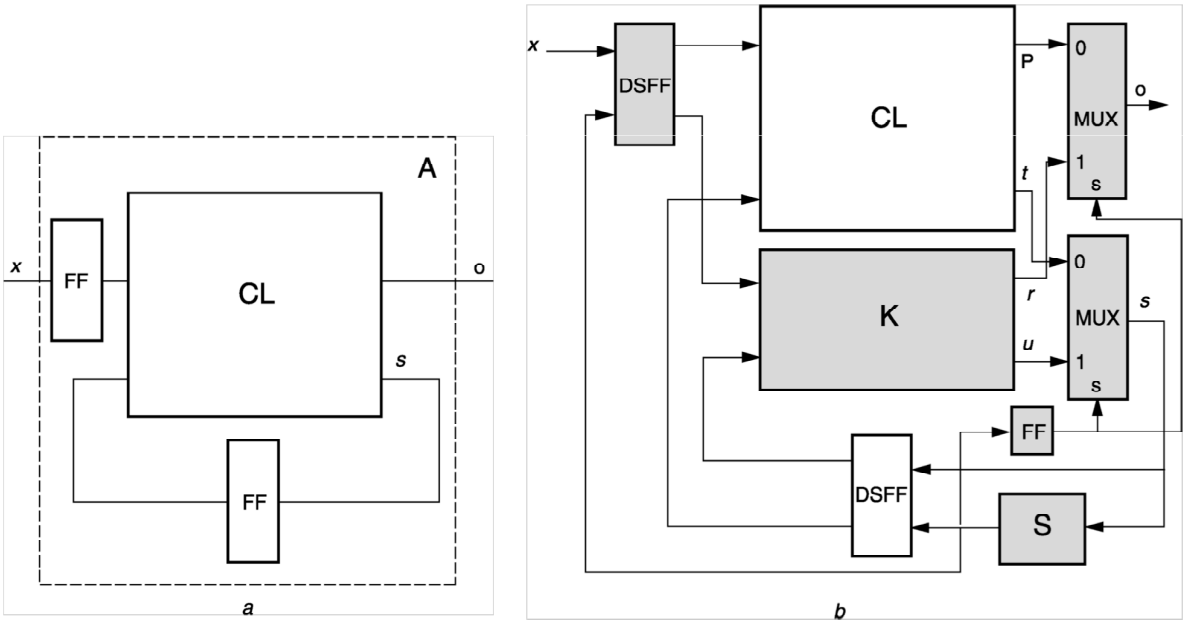



**Fig. 9** *Kernel-based optimised architecture*

# Decomposition of FSMs

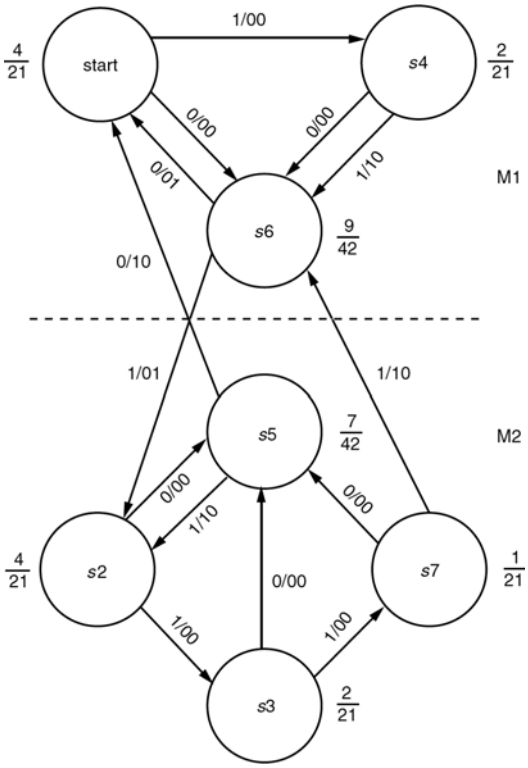
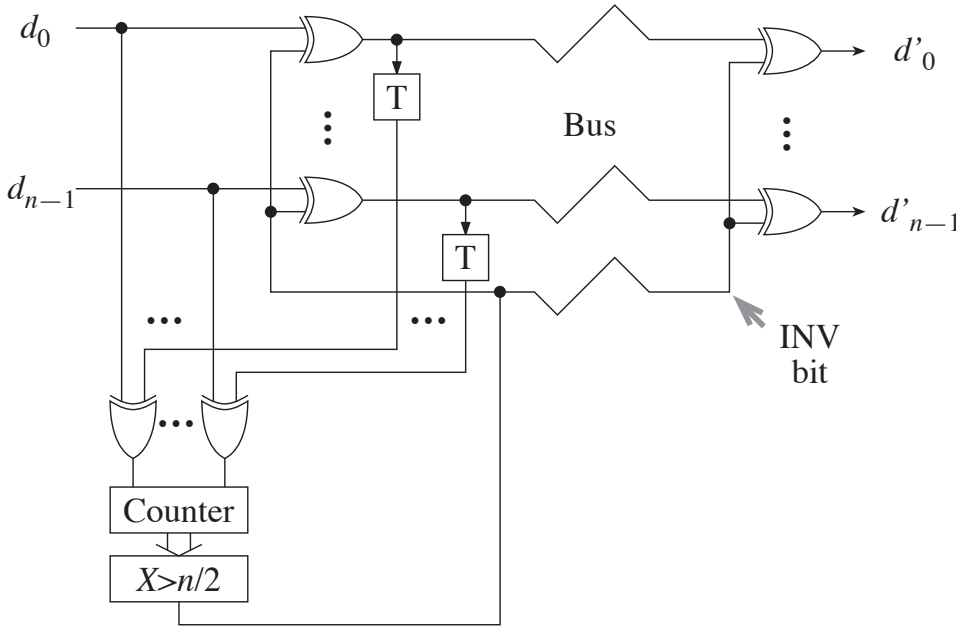



**Fig. 10** *Example of an FSM (dk27) that may be decomposed into two sub-FSMs such that one sub-FSM can be shut off when the other is active and vice versa*



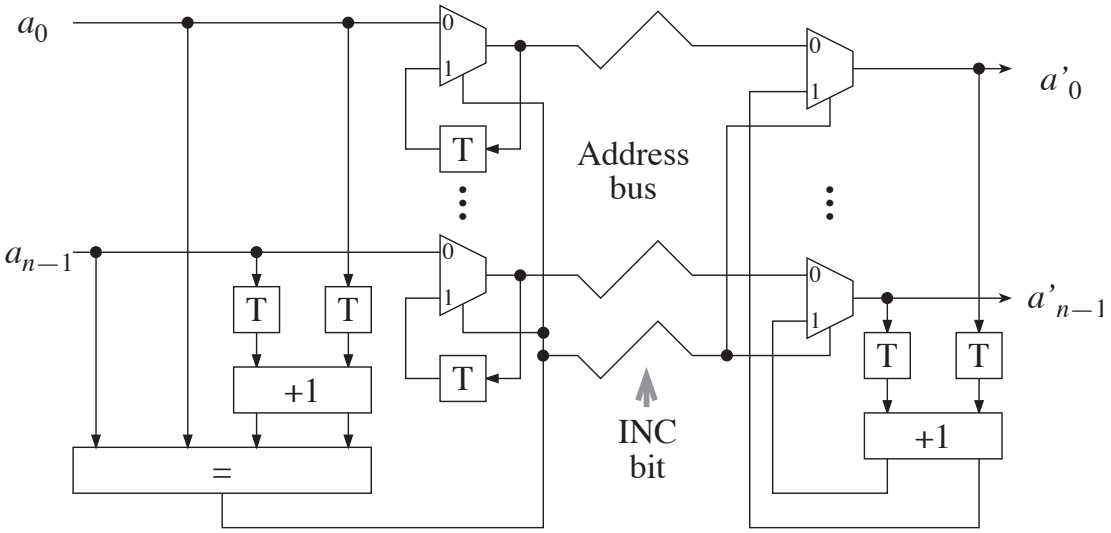
# Bus-invert code

- Invert extra bus bit when this action will save power



# T0 code

- Keep bus state when next value (address) is anticipated

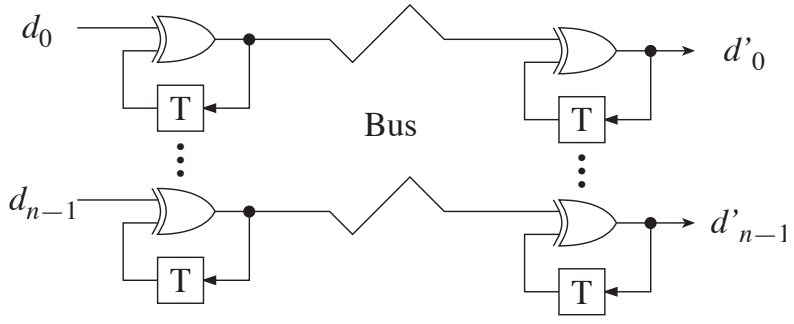





# Level vs. transition signaling

- Level signaling
  - Active-low: "1" is represented by a low voltage
  - Active-high: "1" is represented by a high voltage
- Transition signaling
  - "0" is represented by no transition
  - "1" is represented by a transition

$\Rightarrow$ only 1's consume power



# Limited-weight codes

- Design code with few 1's [Stan'97]

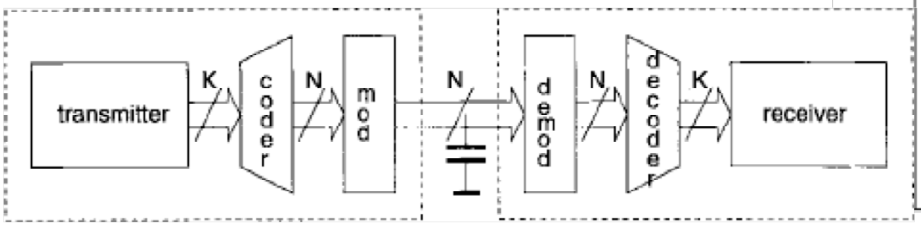
*from ["Low-power encodings for global communication in CMOS VLSI," by M.R. Stan and W.P. Burleson, IEEE TVLSI, vol. 5, no. 4, pp. 444-455]*

TABLE II
$M$ VERSUS $N$ FOR GIVEN $K$

| information bits ($K$) | 2 | 4 | 4 | 8 | 8 | 8 | 8 | 16 |
|---|---|---|---|---|---|---|---|---|
| maximum nr. of 1's ($M$) | 1 | 1 | 2 | 1 | 2 | 3 | 4 | 8 |
| codeword length ($N$) | 3 | 15 | 5 | 255 | 23 | 11 | 9 | 17 |

TABLE III
2-LWC AND 1-LWC FOR A 16-SYMBOL SOURCE

| symbol | minimally encoded | 2-LWC | 1-LWC |
|---|---|---|---|
| 0 | 0000 | 00000 | 000000000000000 |
| 1 | 0001 | 00001 | 000000000000001 |
| 2 | 0010 | 00010 | 000000000000010 |
| 3 | 0011 | 00011 | 000000000000100 |
| 4 | 0100 | 00100 | 000000000001000 |
| 5 | 0101 | 00101 | 000000000010000 |
| 6 | 0110 | 00110 | 000000000100000 |
| 7 | 0111 | 11000 | 000000001000000 |
| 8 | 1000 | 01000 | 000000010000000 |
| 9 | 1001 | 01001 | 000000100000000 |
| 10 | 1010 | 01010 | 000001000000000 |
| | 1011 | 10100 | 000010000000000 |
| | 1100 | 01100 | 000100000000000 |
| | 1101 | 10010 | 001000000000000 |
| | 1110 | 10001 | 010000000000000 |
| | 1111 | 10000 | 100000000000000 |






# References

**04.pdf** **Low-power RT-level synthesis techniques: a tutorial**

*M. Pedram and A. Abdollahi*

IEE Proceedings on Computers and Digital Techniques, volume 152, issue 3, May 2005, pages 333-343

**[Stan'97]** **Low-power encodings for global communication in CMOS VLSI**

*M.R. Stan and W.P. Burleson*

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, volume 5, issue 4, Dec. 1997, pages 444-455