Chapter 1.2

CMOS Low-Power Analog Circuit Design

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Abstract

This chapter covers device and circuit aspects of low-power analog CMOS circuit design. The fundamental limits constraining the design of low-power circuits are first recalled with an emphasis on the implications of supply voltage reduction. Biasing MOS transistors at very low current provides new features but requires dedicated models valid in all regions of operation including weak, moderate and strong inversion. Low-current biasing also has a strong influence on noise and matching properties. All these issues are discussed, together with the particular aspects related to passive devices and parasitic effects. The design process has to be supported by efficient and accurate circuit simulation. To this end, the EKV compact MOST model for circuit simulation is shortly presented. The use of the basic concepts such as pinch-off voltage, inversion factor and specific current are highlighted thanks to some very simple but fundamental circuits and to an effective use of the model. New design techniques that are appropriate for low-power and/or low-voltage circuits are presented with an emphasis on the analog floating point technique, the instantaneous companding principle, and their application to filters.

1.2.1 Introduction

The current trend towards low-power design is mainly driven by two forces [1]: the growing demand for long-life autonomous portable equipment, and the technological limitations of high-performance VLSI systems. For the first category of products, low-power is the major goal for which speed and/or dynamic range might have to be sacrificed. High speed and high integration density are the objectives for the second application category, which has experienced a dramatic increase of heat dissipation that is now reaching a fundamental limit. These two forces are now merging as portable equipment grows to encompass high-throughput computationally intensive products such as portable computers and cellular phones.

The most efficient way to reduce the power consumption of digital circuits is definitely to reduce the supply voltage, since the average power consumption of CMOS digital circuits is proportional to the square of the supply voltage. On the other hand, the reduction of the supply voltage is also required to maintain the electric field at an acceptable level. The resulting performance loss can be overcomed for standard CMOS

technologies by introducing more parallelism [2][3][4] and/or to modify the process and optimize it for low supply voltage operation [4][5][6].

The rules for analog circuits are quite different than those applied to digital circuits. In order to clarify these differences, the fundamental limits to the reduction of the power consumption are recalled in Section 1.2.2. It is shown that decreasing the supply voltage does unfortunately not reduce the power consumption of analog circuits. This is mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required signal-to-noise ratio (SNR) and the frequency of operation (or the required bandwidth). A first-order analysis also shows that the absolute minimum power consumption required to process analog signals is almost independent of the supply voltage reduction. In addition to these fundamental limits, some practical limits and additional obstacles to the power reduction are also discussed.

This trend towards low-power has emphasized some aspects of MOS modelling for low-voltage and low-current analog circuit design and simulation. Particularly, the necessity to have a clear understanding of the MOS transistor operating at very low-current and to correctly model the operation of the device in the weak and moderate inversion regions, which have been ignored by most designers for years, has become a must. The availability of a good MOS transistor model has thus become a real issue for the efficient design and simulation of high performance analog and digital integrated circuits. Section 1.2.3 presents the operation and modeling of the long-channel MOS transistor with a strong emphasis on low-current. Based on this analytical model, a compact MOST model (named the EKV model) has been developed for circuit simulation and is shortly presented in Section 1.2.4.

The advantages of this model are brought out in Section 1.2.5 thanks to some simple but fundamental circuit examples. The basic concepts such as the pinch-off voltage, the specific current, the inversion factor are illustrated and exploited to better understand existing circuits or to develop new ones. They lead to the development of an attractive ratio-based design technique which is portable from one process to another, to MOS only current dividers and to low-voltage cascode bias circuits.

Some additional system considerations are given in Section 1.2.6.2. Some analog signal processing systems like hearing aids for example require a SNR much smaller than the dynamic range. A significant power reduction can be obtained by distinguishing the SNR and the dynamic range and letting the noise follow the signal level to maintain just the necessary value of SNR. This can be achieved thanks to the analog floating point approach which uses a variable gain (or range switcher) at the input and the output of the analog signal processing system to realize the compression and respectively the expansion. Distortion-free operation is obtained thanks to a proper update of all the system's state variables.

Section 1.2.6.3 presents an approach to low-voltage analog signal processing called "log-domain" filtering, where currents are compressed logarithmically when transformed into voltages and expanded exponentially when converted back to currents. The input signal has to be predistorted in order to avoid any distortion due to the non-linear operation. The log and exponential functions are implemented thanks to the exponential current-to-voltage characteristics inherent to the bipolar transistor or to the MOS transistor biased in weak inversion. Both of these techniques seem to be very attractive for low-power and low-voltage circuit design, but still a lot of effort is needed to better understand them and demonstrate their benefits for low-power.

Finally, a summary and some conclusions are drawn in Section 1.2.7.

1.2.2 Limits to low-power for analog circuit design

1.2.2.1 Fundamental limits

Power is consumed in analog signal processing circuits to maintain the signal energy above the fundamental thermal noise in order to achieve the required signal-to-noise ratio (SNR). A representative figure of merit of different signal processing systems is the power consumed to realize a single pole. The minimum power necessary to realize a single pole can be derived by considering the basic integrator presented in Fig. 2.1 assuming an ideal 100% current efficient transconductor, meaning that all the current pulled from the supply voltage is used to charge the integrating capacitor.

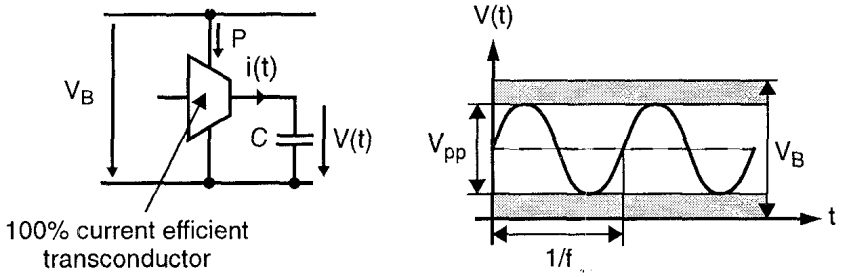


Figure 2.1 Basic integrator used to evaluate the power necessary to realize a single pole

The power consumed from the supply voltage source V_B which is necessary to create a sinusoidal voltage *V(t)* across capacitor C having a peak-to-peak amplitude V_{pp} and a frequency f can be expressed as:

$$P = V_B \cdot fCV_{pp} = fCV_{pp}^2 \cdot \frac{V_B}{V_{pp}} \tag{1}$$

whereas the signal-to-noise ratio is given by:

$$SNR = \frac{V_{pp}^2/8}{kT/C} \tag{2}$$

Combining (1) and (2) yields:

$$P = 8kT \cdot f \cdot SNR \cdot \frac{V_B}{V_{pp}} \tag{3}$$

According to (3), the minimum power consumption of analog circuits at a given temperature is basically set by the required SNR and the frequency of operation (or the required bandwidth). Since this minimum power consumption is also proportional to the ratio between the supply voltage and the signal peak-to-peak amplitude, power efficient analog circuits should be designed to maximize the voltage swing. The minimum power for circuits that can handle rail-to-rail signal voltages ($V_{pp} = V_B$) reduces to [7][8][9]:

$$P_{min} = 8kT \cdot f \cdot SNR \tag{4}$$

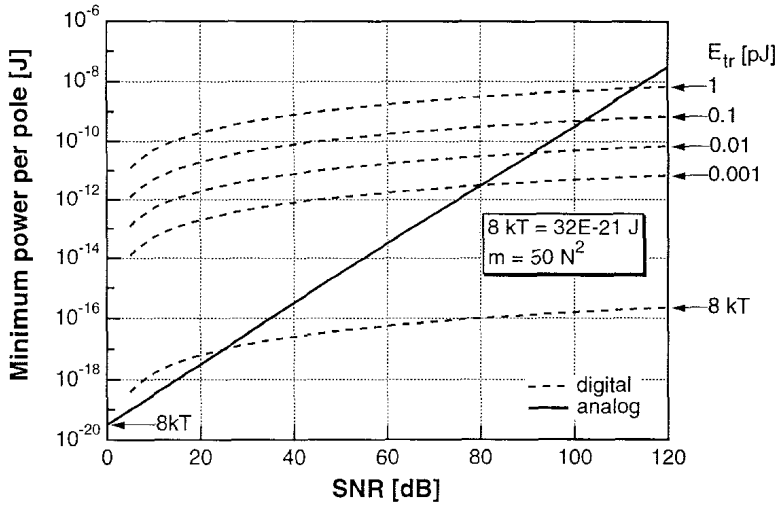


Figure 2.2 Minimum power for analog and digital circuits

This absolute limit is very steep, since it requires a factor 10 of power increase for every 10 dB of signal-to-noise ratio improvement. It applies to each pole of any linear analog filter (continuous or sampled-data as switched capacitors [8]) and is reached in the case of a simple passive RC filter, whereas the best existing active filters are still two orders of magnitude above. High-Q poles in the passband reduce the maximum amplitude at other frequencies and therefore increase the required power, according to (3).

Approximately the same result is found for relaxation oscillators, whereas the minimum power required for a voltage amplifier of gain A_v can be derived considering a single stage common-source (or common-emitter) small-signal amplifier. The signal-to-noise ratio is obtained by comparing the input rms voltage to the input-referred noise voltage:

$$SNR = \frac{V_{in}^2}{4kTR_N \cdot \Delta f} \tag{5}$$

where R_N is the input-referred thermal noise resistance, which is given by:

$$R_N = \frac{\gamma}{g_m} = \frac{\gamma}{I} \cdot \frac{I}{g_m} = \gamma \cdot \frac{V_B}{P} \cdot \frac{I}{g_m} \tag{6}$$

where γ is the noise factor defined by (48) as the product of the input-referred thermal noise resistance and the effective transconductance of the device. It is equal to $n/2$ in the case of a MOS transistor biased in weak inversion where n is the slope factor defined by (19). The power can be expressed as a function of the SNR by combining (5) and (6):

$$P = 4\gamma kT \cdot \Delta f \cdot \frac{V_B}{V_{in}^2} \cdot \frac{I}{g_m} \cdot SNR \tag{7}$$

As will be shown in Section 1.2.3, for a transistor biased in weak inversion the current-to-transconductance ratio I/g_m is equal to nU_T, where $U_T \equiv kT/q$ is the thermodynamic voltage. In this case, the power given by (7) reduces to:

$$P = 2n \cdot kT \cdot \Delta f \cdot \frac{V_B}{V_{in}} \cdot \frac{nU_T}{V_{in}} \cdot SNR \tag{8}$$

Since the peak-to-peak amplitude of the output voltage $A_v \cdot 2\sqrt{2}V_{in}$ is bounded by the supply voltage V_B, the absolute minimum power is given by:

$$P > P_{min} = 8n \cdot kT \cdot \Delta f \cdot A_v \cdot SNR \tag{9}$$

where it has been assumed that the input voltage is maximum and equal to $nU_T/\sqrt{2}$. According to (9), the minimum power for an amplifier is nA_v-times larger than the limit given by (4).

The minimum power for an analog system can be compared to that of a digital system, in which each elementary operation requires a certain number m of binary gate transition cycles, each of which dissipates an amount of energy E_{tr}. The minimum power is then simply given by:

$$P_{min\text{-}digital} = m \cdot f \cdot E_{tr} \tag{10}$$

where f is the signal bandwidth. The number m of transitions is only proportional to some power a of the number of bits N, and therefore power consumption is only weakly dependent on SNR (essentially logarithmically):

$$m \cong N^a \sim [\log (SNR)]^a \tag{11}$$

Comparison with analog is obtained by estimating the number of gate transitions that are required to compute each period of the signal, which for a single pole digital filter can be estimated to be approximately:

$$m \cong 50 \cdot N^2 \tag{12}$$

Immunity to thermal noise imposes an absolute minimum energy per transition E_{trmin} estimated to 8kT, which provides the absolute minimum power limit. However, in practice $E_{tr} = C \cdot V_B^2$ is forced to a much higher value (10^{-15} to 10^{-12} Joules) by the need to recharge the equivalent capacitance C of each gate to the supply voltage V_B. As shown in Fig. 2.2, the minimum power for digital is therefore much higher than the absolute limit $8kT \cong 32\times10^{-21} J$ at room temperature. The minimum gate capacitance is strongly dependent on the process feature size and the supply voltage is imposed by the need to achieve the required delay time and by established standards. Furthermore, if the activation rate of the circuit is very low (very small percentage of the available gates in transition on average), then the standby current of each of the gates may contribute to a non negligible additional static power consumption.

Comparison of these fundamental limits are plotted in Fig. 2.2. They clearly show that analog systems may consume much less power than their digital counterpart, provided a small signal-to-noise ratio is acceptable. But for systems requiring large signal-to-noise ratios, analog becomes very power inefficient. It is worth mentioning that a comparison of chip area basically leads to the same qualitative conclusion.

1.2.2.2 Practical limits

The limits discussed so far are fundamental since they do not depend on the technology nor on the choice of power supply voltage. However, a number of obstacles or technological limitations are on the way to approach these limits in practical circuits:

a) Capacitors increase the power necessary to achieve a given bandwidth. They are only acceptable if their presence reduces the noise power by the same amount (by reducing the noise bandwidth). Therefore, ill-placed parasitic capacitors very often increase power consumption.
b) The power spent in bias circuitry is wasted and should in principle be minimized. However, inadequate bias schemes may increase the noise and therefore require a proportional increase in power. For example, a bias current is more noisy if it is obtained by multiplying a smaller current.
c) According to (3), power is increased if the signal at any node corresponding to a functional pole (pole within the bandwidth, or state variable) has a peak-to-peak voltage amplitude smaller than the supply voltage V_B. Thus, care must be taken to amplify the signal as early as possible to its maximum possible voltage value, and to maintain this level all along the processing path. Using current-mode circuits with limited voltage swings is therefore not a good approach to reduce power, as long as the energy is supplied by a voltage source. It only becomes attractive if voltage companding techniques can be used (see Section 1.2.6.3).
d) The presence of additional sources of noise implies an increase in power consumption. These include 1/f noise in the devices, and noise coming from the power supply or generated on chip by other blocks of the circuit.
e) When capacitive loads are imposed (for example by parasitic capacitors), the current I necessary to obtain a given bandwidth is inversely proportional to the transconductance-to-current ratio g_m/I of the active device. The small value of g_m/I inherent to MOS transistors operated in strong inversion may therefore cause an increase in power consumption.
f) The need for precision usually leads to the use of larger dimensions for active and passive components, with a resulting increase in parasitic capacitors and power.
g) All switched capacitors must be clocked at a frequency higher than twice the signal frequency. The power consumed by the clock itself may be dominant in some applications.

Ways to reduce the effect of these various limitations can be found at all levels of analog design ranging from device to system.

1.2.2.3 Other obstacles to low-power

In addition to the fundamental and practical limitations discussed previously, there are also historical or even psychological barriers to the efficient design of LP analog circuits. The most important can be listed as:

a) Analog blocks must often be taken from existing libraries with bias currents at the milliampere level and with architectures that are not compatible with low-voltage or low-current.
b) The use of very low bias currents is often discarded due to a lack of adequate transistor models and correct characterization of transistors parameters as well as worst case leakage currents. Another obstacle is the fear of breaking the psychological

microampere barrier.

c) The requirements on PSRR are often exaggerated and mistaken for insensitivity to noise generated on chip.

1.2.2.4 Implications of supply voltage reduction

Unlike digital circuits, where the dynamic power decreases with the square of the supply voltage, according to (3), reducing the supply voltage of analog circuits while preserving the same bandwidth and SNR, has no fundamental effect on their minimum power consumption. However, this absolute limit was obtained by neglecting the possible limitation of bandwidth B due to the limited transconductance g_m of the active device. The maximum value of B is proportional to g_m/C. Replacing the capacitor value C by g_m/B in (2) and expressing the product of the SNR times the bandwidth yields:

$$SNR \cdot B = \frac{V_{pp}^2 \cdot g_m}{8kT} \tag{13}$$

In most cases, scaling the supply voltage V_B by a factor K requires a proportional reduction of the signal swing V_{pp}. Maintaining the bandwidth and the SNR is therefore only possible if the transconductance g_m is increased by a factor K^2. If the active device is a bipolar transistor (or a MOS transistor biased in weak inversion), its transconductance can only be increased by increasing the bias current I by the same factor K^2; power $V_B \cdot I$ is therefore increased by K. The situation is different if the active device is a MOS transistor biased in strong inversion. Its transconductance can be shown to be proportional to I/V_P, where V_P is the pinch-off or saturation voltage of the device. Since this saturation voltage has to be reduced proportionally with V_B, increasing g_m by K^2 only requires an increase of current I by a factor K and hence the power remains unchanged.

However, the maximum frequency of operation may be affected by the value of the supply voltage. For a MOS transistor in strong inversion, the frequency f_{max} for which the current gain falls to unity is approximately given by:

$$f_{max} \cong \frac{\mu \cdot V_P}{L^2} \tag{14}$$

Therefore, if the process is fixed (channel length L constant) a reduction of V_B and V_P by a factor K causes a proportional reduction of f_{max}. However, there is no fundamental reason to reduce the supply voltage of an analog circuit in a given process. On the other hand, a reduction of V_B is unavoidable to maintain the electric fields constant when scaling down a process. Both V_P and L are then scaled by the same factor K and the maximum frequency f_{max} is increased by K. For a bipolar transistor, V_P in (14) is replaced by $U_T = kT/q$ and f_{max} does not, in first approximation, depend on the supply voltage V_B.

Low-voltage limitations are not restricted to power or frequency problems. Reducing V_P increases the transconductance-to-current ratio of MOS transistors which in turn increases the noise content of current sources and drastically degrades their precision. Conductance in analog switches is difficult to ensure when the supply voltage falls below approximately the sum of the p- and n-channel transistor threshold voltages. For a given value of time constant, charge injection in a switch does not depend on V_B in absolute

value, but it increases in relative value if V_B and V_{pp} are decreased. The same is true for any constant voltage overhead such as the base-emitter voltage in bipolar transistors or the threshold voltage in MOS transistors.

As already illustrated in the previous discussion on the fundamental limits to LP and LV, many of the problems and solutions encountered in the design of LP-LV analog circuits are directly related to the properties and limitations of the MOS transistor itself, which must therefore be properly understood and correctly modelled down to very low currents. For this reason, the basic operation of the long-channel MOS transistor will be presented in Section 1.2.3, with a strong emphasis on low current and weak inversion operation. A complete but simple analytical model that can be used for the analysis and design of simple analog circuits will be elaborated. Section 1.2.4 will present the use of the MOST long-channel model and its extension to the EKV MOST model, a compact MOST model which includes all the second-order effects (so important in real-world design) and which is dedicated to LP and LV circuits simulation.

1.2.3 MOST basic long-channel static model at low current

1.2.3.1 Drain current, pinch-off voltage and modes of operation

Fig. 2.3 shows the cross-section and the corresponding symbol of an idealized n-channel MOS transistor. The intrinsic geometric and operating symmetry of the device with respect to the source and the drain can be preserved in the model by referring the source voltage V_S, the gate voltage V_G and the drain voltage V_D to the local substrate. This is clearly not the convention adopted for SPICE models for which all potentials are referred to the source electrode. The drain current is defined positive entering the drain electrode which is the most positive electrode between source and drain.

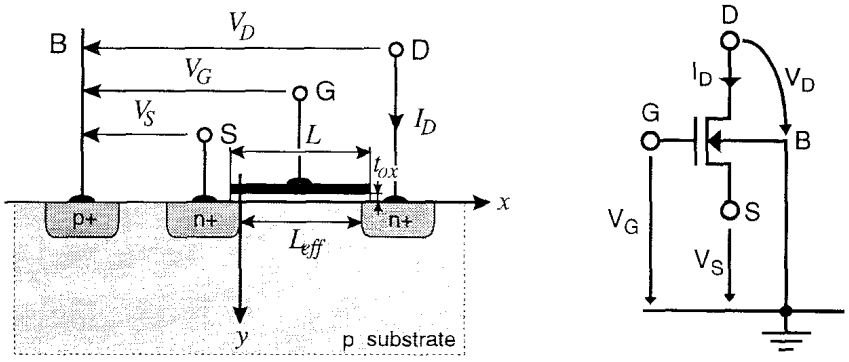


Figure 2.3 Cross-section of an idealized n-channel MOS transistor and the corresponding symbol. All voltages are referred to the local p-type substrate

A general expression for the drain current that includes both the drift and the diffusion transport mechanisms is given by [11][12][13][14][15]:

$$I_D = W \cdot \mu_n \cdot (-Q'_{inv}) \cdot \frac{dV_{ch}}{dx} \tag{15}$$

transconductance of M_2 (in saturation). Factor ξ is defined as the ratio of the forward current of M_2 to the reverse current of transistor M_1:

$$\xi \equiv \frac{g_{ms2}}{g_{md1}} = \frac{I_{F2}}{I_{R1}} = \frac{I}{I_{R1}} = \frac{I_{S2}}{I_{S1}} = \begin{cases} \dfrac{S_2}{S_1} \cdot \exp\left(\dfrac{V_{T01} - V_{T02}}{nU_T}\right) & \textit{in weak inv.} \\ \dfrac{S_2}{S_1} \cdot \left(\dfrac{V_G - V_{T02} - nV_{S2}}{V_G - V_{T01} - nV_{S2}}\right)^2 & \textit{in strong inv.} \end{cases} \tag{92}$$

For transistors having the same threshold voltages $V_{T01} = V_{T02}$ (neither short- nor narrow-channel effects), factor ξ reduces to S_2/S_1 in both weak and strong inversion. If S_2/S_1 is made much larger than 1, factor ξ also becomes much larger than 1 and the output conductance given by (91) tends to that of a traditional cascode stage:

$$g_o \cong g_{ds2} \cdot \frac{g_{ds1}}{g_{ms2}} \qquad \textit{for: } \xi >> 1 \tag{93}$$

This can be realized by choosing an equal channel length for both M_1 and M_2 and by setting the channel width W_2 much larger than W_1. Setting W_1 to the minimum width results in an increase of V_{T01} with respect to V_{T02} due to the narrow-channel effect on M_1 and consequently helps to further increase factor ξ significantly, while maintaining a reasonable S_2/S_1 ratio. Although this is true in both weak and strong inversion, it is really effective mainly in weak inversion thanks to the exponential term in (93).

There are of course other cascode bias circuits, but probably the most compact and current efficient is the one shown in Fig. 2.24. P. Heim proposed a cascode biasing circuit which has the interesting property that it can operate at any current level with a minimal output saturation voltage and independently of the technology since the design is based on ratios [48]. Unfortunately, this circuit requires a relatively large number of transistors and is therefore not suited for dynamic applications but rather to constant current which is in contradiction with its ability to work at any current level.

1.2.6 Some additional system considerations

1.2.6.1 General considerations

Power minimization must already be addressed at the system level. A first aspect is the management of the power delivered to the various blocks of a chip, which will be very important for digital sub-circuits. For analog blocks, voltage is not critically related to power, and power management can be limited to shutting off some functions when they are not needed, and to possibly multiplying (on- or off-chip) the supply voltage if it comes from a very low voltage source.

High-frequency operation tends to require a power much above the limits presented in Section 1.2.2, essentially because of the presence of parasitic capacitors. The architecture of low-power RF receivers should thus be selected to minimize the number of active devices operating at the carrier frequency. An extreme solution would be to directly sample the RF signal at a subharmonic of the usual local oscillator frequency. All the image bands produced by this undersampling process would have to be eliminated by passive SAW filters just after the antenna. Of course, the signal power available after mixing would be reduced by the undersampling factor. The sampling mixer should thus be

preceded by RF amplification stages.

Certain applications such as paging or the Global Positioning System (GPS) do not require full-time operation of the receiver. Indeed, depending on the protocol, the duty cycle may be drastically reduced, with a proportional reduction in power consumption. Commercially available watch pagers already operate continuously for 30 days on a small battery.

1.2.6.2 The analog floating point technique

For continuous operation, and even when high frequency is not an obstacle, it will never be possible to pass the limit given by (4), and at least ten times more power will probably be needed for practical reasons. This means that it will never be possible to realize a 16-bit audio A/D converter (SNR = 98 dB) that consumes less than about 50-100 W, and even more power will be needed for amplifying the analog signal before conversion. On the other hand, a few microwatts per pole will be sufficient to implement the subsequent digital filtering with an advanced process and low-voltage operation. Thus, the necessary analog interfaces will (and do in fact already) consume most of the power in a signal processing chain when a dynamic range larger than 40 to 60 dB is required.

This is true only if the dynamic range must be assimilated with the maximum signal-to-noise ratio SNR that can be achieved in the whole bandwidth. However, in many applications, the SNR necessary for a certain level of signal is much smaller than the full dynamic of the signal. For example, speech transmission only requires a SNR of 40 dB, but the range of signals to be processed can be as large as 100 dB. By letting the noise follow the signal level to maintain just the necessary value of SNR, the 60 dB difference in this example provides the possibility to reduce power consumption by a factor of 10^6!

A well-known solution along this line is to use automatic gain control (AGC), in which the gain is slowly adapted to maintain constant the RMS or peak level of the signal, without affecting its instantaneous wave form. This solution necessarily causes some distortions, which must be minimized by carefully selecting the time constant(s) of the control loop.

Another known approach is the automatic range selection used in instrumentation. This approach can be extended to general analog processing systems by using the architecture shown in Fig. 2.25.

This approach, called analog floating point (AFP), amounts to multiply the instantaneous signal $x(t)$ by a factor K which is adapted to maintain the signal $x'(t)$ entering the processor within a min-max range. The scaled signal x' is then processed to produce a signal y' which is divided by the same factor K. Distortions by the processor are avoided if its state vector z (set of state variables) is multiplied by K^+/K each time the factor changes from K to a new value K^+. This updating of the state vector must be carried out in a time shorter than half the period of the highest frequency to be processed. It can be done between two sampling instants if the system is operating in discrete time.

1.2.6.3 Instantaneous companding and "log-domain" filtering

A possible way to circumvent the dynamic range problems introduced by the reduction of the supply voltage is to use companding. Companding systems traditionally used syllabic compression where the gains of the compressor and the expander are adjusted according to slowly varying characteristics of the signal such as envelope or

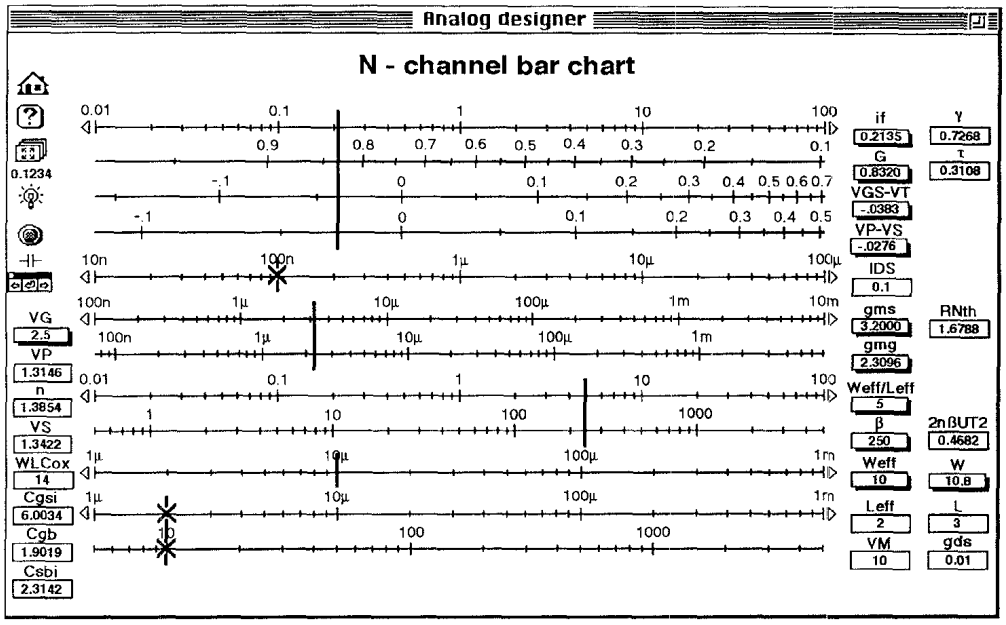


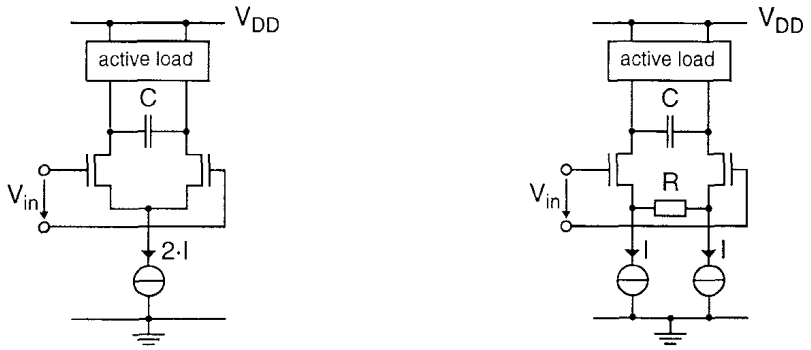
Figure 2.25 The analog floating point technique [49]

power [50]. More recent techniques called voltage companding current-mode filtering or "log-domain" filtering use instantaneously varying gains instead of syllabic detection or in other words non-linear characteristics [53]-[65]. The currents, having inherently a large dynamic range, are compressed when transformed into voltages (for example prior to the integration on a capacitor) and expanded afterwards when transformed back to currents. This technique makes the voltage swings across the integrator's capacitors almost independent of the supply voltage, which can then be reduced to the minimum required for a proper operation of the circuit. The "log-domain" technique additionally exploits the properties of the exponential function that can easily be implemented using either the well known relation between the collector current and the base-emitter voltage of a bipolar transistor or the drain current of a MOS transistor operating in weak inversion.

In addition to a low-voltage operation, voltage-companding also provides the most efficient use of current for implementing a given transconductance. A comparison can be elaborated by considering the g_m/I ratio as a factor of merit. The latter is maximum and equal to unity for a bipolar transconductor operating in small-signal. The maximum g_m/I for a MOST transconductor as the one used in the integrator shown in Fig. 2.26 (a), is obtained in weak inversion but is unfortunately n times smaller than for a BJT. The linear range of the circuit shown in Fig. 2.26 (a) is strongly limited to typically U_T.

The transconductor can of course be linearized in order to get the required dynamic range. Unfortunately, any linearization technique, as for example the one shown in Fig. 2.26 (b), results in a degradation of the effective g_m/I ratio which is proportional to the increase of the linear voltage range with respect to U_T:

$$\frac{g_m \cdot U_T}{I} = \frac{U_T}{R \cdot I} = \frac{U_T}{V_{in\text{-}max}} = \frac{1}{g_m \cdot R} << 1 \qquad (94)$$

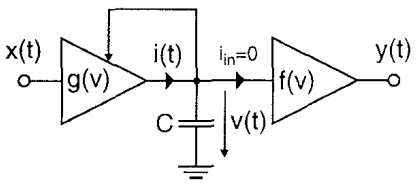


$V_{in\text{-}max} \leq U_T << V_{DD}$ $\qquad$ $U_T << V_{in\text{-}max} \leq R \cdot I$

a) Small-signal integrator $\qquad$ *b) Linearized integrator*

Figure 2.26 Basic MOS integrators

The companding technique allows thus to extend the dynamic range while preserving the maximum g_m/I ratio.



expanding function: $y = f(v)$

companding function: $i = g(v) \cdot x$

linear capacitor: $i = C \cdot \dfrac{dv}{dt}$

Figure 2.27 Basic integrator illustrating the principle of instantaneous companding

The principle of instantaneous companding is illustrated by the integrator presented in Fig. 2.27, where the output signal $y(t)$ is expanded by a given expanding function $f(v)$ from the voltage across the integration capacitor C which is assumed to be linear. In order to preserve a global linear transfer function:

$$y(t) = \frac{1}{\tau} \cdot \int_{-}^{t} x(\tau) \cdot d\tau \qquad or \qquad \tau \cdot \frac{dy}{dt} = x \tag{95}$$

the current $i(t)$ provided by the input current amplifier (or transconductor) has to be predistorted with a non-linear gain function $g(v)$ which should satisfy the following necessary and sufficient condition [51]:

$$g(v) = \frac{C}{\tau} \cdot \left[\frac{df}{dv}\right]^{-1} \tag{96}$$

This general relation demonstrates that it is not necessary to have an exponential expanding function in order to perform companding. Fig. 2.28 shows an example of cubic

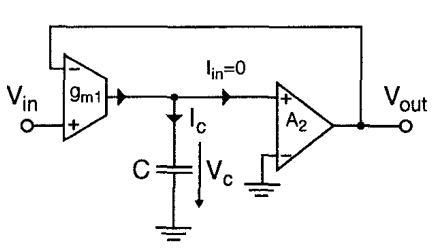
expansion:

$$f(v) = v^3 + v \tag{97}$$

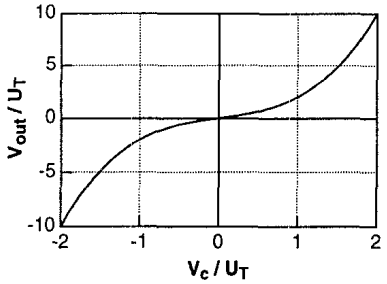
which can be applied to the first-order low-pass filter presented in Fig. 2.28 (a).

The cubic expansion is implemented using a voltage amplifier having a non-linear gain given by:

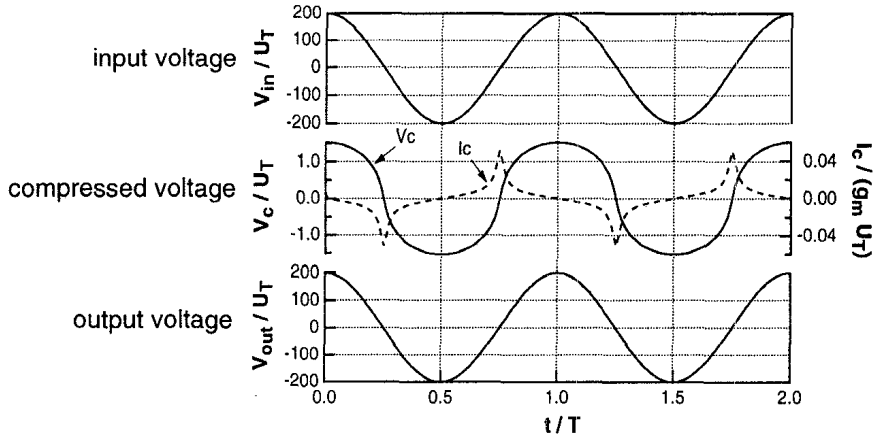
$$A_2 = A_0 \cdot \left[(V_c/U_T)^2 + 1 \right] \tag{98}$$



a) First-order low-pass filter



b) Expansion characteristic



c) Large-signal transient analysis

Figure 2.28 Example of a cubic expansion function

The input signal is predistorted by the input non-linear transconductor having a transconductance equal to:

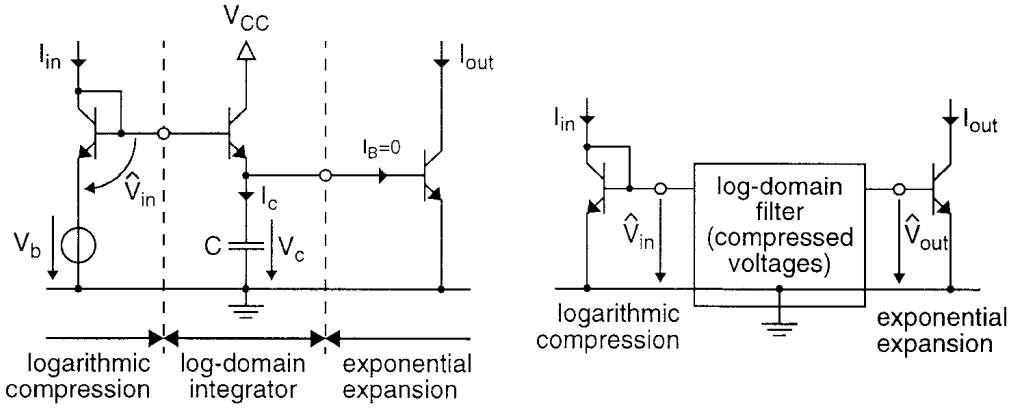
$$g_{m1} = \frac{g_m}{3\,(V_c/U_T)^2 + 1} \tag{99}$$

It is easily verified that the large-signal transfer function corresponds indeed to a first-order low-pass filter having a cut-off frequency given by:

$$f_c = A_0 \cdot \frac{g_m}{2\pi C} \tag{100}$$

The circuit of Fig. 2.28 (a) has been simulated for $A_0 = 1$ and $f_cT = 100$. The voltages are plotted in Fig. 2.28 (c) showing particularly the voltage across the capacitance which looks very distorted but which finally leads to a non-distorted output voltage thanks to the predistortion introduced by the input non-linear transconductor g_{m1} .

Although linear integrators can ideally be built with any expanding function, it requires a non-linear amplifier (or transconductor) satisfying (96) which is not always easy or even possible to realize. The exponential function is very well suited to implement companding circuits thanks to the fact that it is invariant to the differentiation operator. The compressor can therefore be built with the same function as the expander.



a) Basic integrator principle *b) Log-domain filters principle [59][63]*

Figure 2.29 Principle of log-domain filters

Moreover, the exponential function can be implemented with a reasonable accuracy using BJTs or MOSTs in weak inversion. An example of a BJT implementation (without bias circuit) is shown in Fig. 2.29 (a). The expanded output current is given by:

$$y = I_{out} = f(V_c) = I_S \cdot \exp\left[V_c / U_T\right] \tag{101}$$

where I_S is the BJT saturation current (and not the specific current). According to (96), the non-linear gain function $g(V_c)$ is given by:

$$g(V_c) = \frac{C \cdot U_T}{\tau \cdot I_S \cdot \exp\left[V_c / U_T\right]} = \frac{C \cdot U_T}{\tau \cdot I_S} \cdot \exp\left[\frac{-V_c}{U_T}\right] \tag{102}$$

The $\exp\left[-V_c / U_T\right]$ term in (102) can easily be obtained by simply connecting the capacitor to the emitter of a BJT as shown in Fig. 2.29 (a). The current flowing into the capacitor assuming the base current of the expander is negligible is then given by:

$$I_c = I_S \cdot \exp\left[\frac{\hat{V}_{in} + V_b - V_c}{U_T}\right] = I_0 \cdot \frac{\exp\left[\hat{V}_{in} / U_T\right]}{\exp\left[V_c / U_T\right]} = \tag{103}$$

$$= \frac{I_0 \cdot I_{in} / I_S}{\exp\left[V_c / U_T\right]} = g(V_c) \cdot I_{in}$$

where $I_0 = I_S \cdot \exp\left[V_b / U_T\right]$ is the bias current setting the time constant, $\hat{V}_{in} = U_T \ln\left(I_{in} / I_S\right)$ is the compressed input voltage and I_{in} is the input current.

Comparing (103) to (102) allows to determine the integration time constant:

$$\tau = \frac{C \cdot U_T}{I_0} = \frac{C}{g_m} \tag{104}$$

which is equal to the time constant of the integrator working in small-signal but valid also for large-signal operation. Fig. 2.29 (a) shows that a linear current-mode integrator can be realized with an exponential integrator surrounded by a logarithmic voltage compressor and an exponential expander.

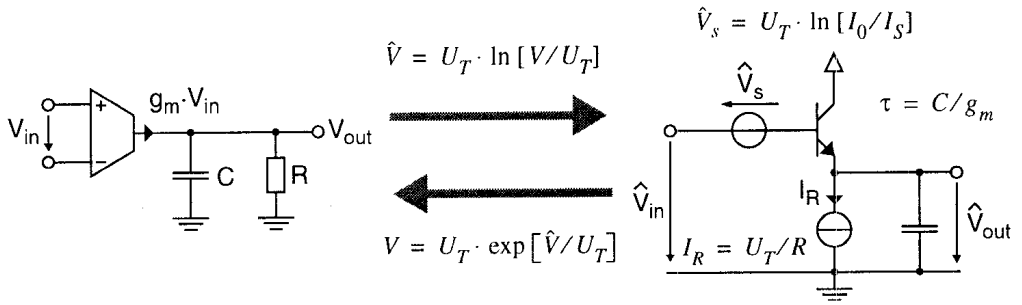


Figure 2.30 Mapping between linear- and log-domain [53][63][64]

As shown in Fig. 2.29 (b), this principle can be extended to higher order filters where the central part is called a log-domain filter since all the voltages are compressed logarithmically [59][63].

Log-domain filters can be designed by simple component substitution from a linear g_m-C filter using the mapping between the linear- and the log-domain [53][64] presented in Fig. 2.30. The mapping is defined by the linear capacitance and the expression of the time constant (or equivalently of the transconductance) being the invariants of the transformation. Note that a resistor in the linear-domain is transformed into a current source in the log-domain. This property can be used to tune the quality factor of a filter or an oscillator.

Log-domain filters can also be implemented in CMOS by simply replacing the bipolar transistors by MOS transistors biased in weak inversion. As an example, Fig. 2.31 (b) shows a MOST version of the log-domain integrator originally proposed by Seevinck [55]. The original bipolar integrator is based on a translinear multiplier which is redrawn with MOS transistors in Fig. 2.31 (a). In order for this MOST multiplier to conform to the translinear principle as described in [66], the source-to-bulk voltages have to be set to zero, which requires that M_3 and M_5 are implemented in separate wells. Writing the equation of the translinear voltage loop yields:

$$-V_{GB1} - V_{GB3} + V_{GB4} + V_{GB2} = 0 \tag{105}$$

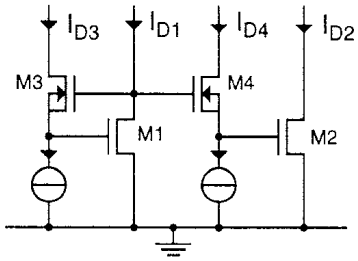
Assuming all the transistors are in saturation, the gate-to-bulk voltages are related to the drain currents I_{Di} according to:

$$V_{GBi} = n_i U_T \ln(I_{Di}/I_{Si}) + V_{T0i} \qquad i = 1 \ldots 4 \tag{106}$$

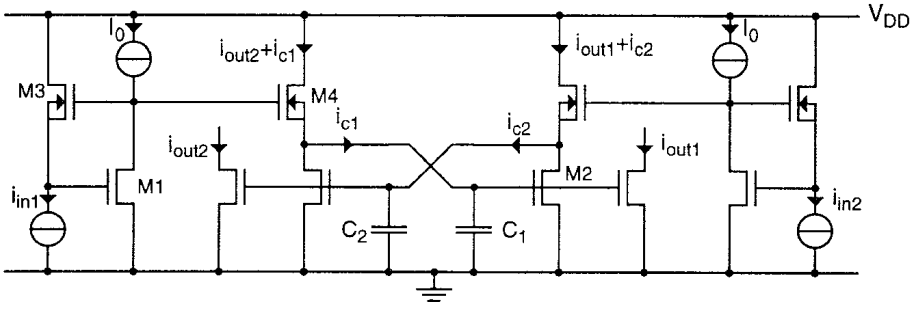
where it has been assumed that $V_{SBi} = 0 \quad i = 1, \ldots, 4$. The product of the drain currents is derived from (105) and (106) assuming a perfect matching of the leakage

current I_{D0i} and identical slope factors n_i :

$$I_{D1} \cdot I_{D3} = I_{D2} \cdot I_{D4} \tag{107}$$



a) MOS multiplier



b) CMOS voltage companding current mode integrator

Figure 2.31 CMOS multiplier and log-domain class AB integrator [55]

The current transfer function of the differential log-domain integrator shown in Fig. 2.31 (b) is obtained by using (107):

$$I_0 \cdot i_{in1} = i_{out1} \cdot (i_{out2} + i_{c1}) \tag{108}$$

$$I_0 \cdot i_{in2} = i_{out2} \cdot (i_{out1} + i_{c2}) \tag{109}$$

Subtracting (109) from (108) results in:

$$(i_{in1} - i_{in2}) \cdot I_0 = i_{out1} \cdot i_{c1} - i_{out2} \cdot i_{c2} \tag{110}$$

Since the capacitors C_1 and C_2 are assumed to be linear, the products of the output and of the capacitive currents are given by:

$$i_{outi} \cdot i_{ci} = nU_T \frac{di_{outi}}{dt} \qquad i = 1, 2 \tag{111}$$

Substituting (111) in (110) and integrating yields the equation of a linear integrator:

$$i_{out} = \frac{1}{\tau} \cdot \int i_{in} dt \tag{112}$$

where $i_{in} \equiv i_{in1} - i_{in2}$ and $i_{out} \equiv i_{out1} - i_{out2}$ are respectively the differential input

and output currents and τ is the integrator time constant given by:

$$\tau = \frac{1}{\omega_u} = \frac{C}{g_m} = \frac{nU_T \cdot C}{I_0} \tag{113}$$

which can be tuned by varying the bias current I_0.

The integrator of Fig. 2.31 (b) can easily be cascaded since the inputs and outputs are compatible. Moreover, it may be driven by several input current sources and can be extended to multiple outputs by adding several output transistors.

Thanks to the companding of the input current, the variation of the voltages across the integrating capacitors C_1 and C_2 stays small (typically smaller than $4nU_T$). Capacitors C_1 and C_2 can therefore be implemented by the non-linear parasitic C_{GB} and C_{GS} capacitances of the n-channel MOS transistors connected to these nodes without significantly degrading the distortion. This makes the integrator suited for integration in a standard digital CMOS process.

The original bipolar integrator suffers from a low DC gain and a high sensitivity to mismatch and base currents. The latter problem is of course solved by using MOSTs instead of BJTs, but the low DC gain and particularly the relative high sensitivity to mismatch becomes a strong handicap for this CMOS implementation. Moreover, the multiplier uses stacked gate-to-source voltages and is therefore not suited to low-voltage operation (it typically requires at least a 1.8 V supply). The circuit of Fig. 2.31 (b) can be improved by using a folded multiplier as suggested in [62] and [65].

It is worth mentioning that due to the class AB operation, the SNR is no longer a linear function of the input current as it would be for a class A circuit. For input currents larger than the nominal bias current, the noise current can no more be considered as constant but it increases with the square root of the signal current and so does the SNR. As shown in Fig. 2.32, the slope of the SNR versus the modulation index in a log-log scale starts at 20 dB/dec and progressively decreases down to 10 dB/dec for a signal amplitude larger than the bias current (or a modulation index m larger than 1). Class AB and class A current mode circuits may be compared by considering that they have initially the same bias current I_0, the same bandwidth B (or small-signal transconductance g_m) and therefore the same idle current noise. Both SNR versus input signal characteristics are thus superimposed for currents smaller than the bias current as shown in Fig. 2.32. The maximum signal or modulation index m_{max} of a class AB circuit is set by the maximum acceptable amount of distortion, whereas it is bounded by the bias current for a class A circuit. The class AB circuit can thus extend the dynamic range by a factor m_{max} and improve the SNR by a factor $\sqrt{m_{max}}$, without any increase of the standby bias current. This makes class AB companding integrators very attractive to extend the dynamic range and the SNR, while preserving the power consumption.

The integrator described previously has been used in the 4th-order low-pass (LP) Tchebycheff filter shown in Fig. 2.33 which has been synthesized from a LC ladder prototype. All integrators have the same transconductance $g_m = I_0/nUt$, which can be tuned by adjusting a common bias voltage V_{G0}. The filter requires an input signal conditioner in order to maintain all currents positive and enable the class AB operation [59]. The difference of the conditioner output currents is equal to the input current, while their product is kept constant and equal to I_0.

The simulated transfer functions are shown in Fig. 2.34 for different bias currents. They are computed from the step responses obtained from a transient analysis in order to

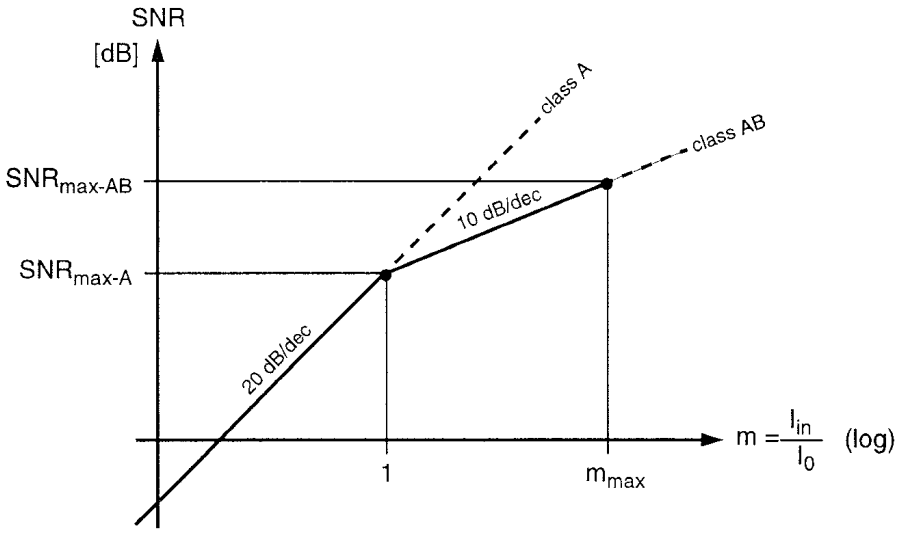


Figure 2.32 SNR versus input signal amplitude for a class A and a class AB circuit

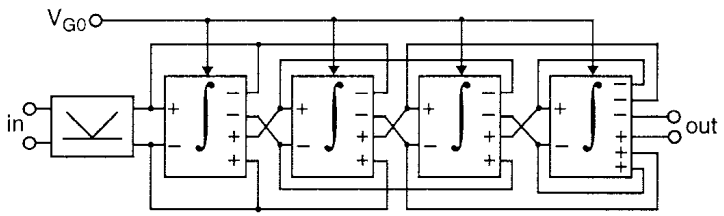


Figure 2.33 4th-order low-pass Tchebycheff filter

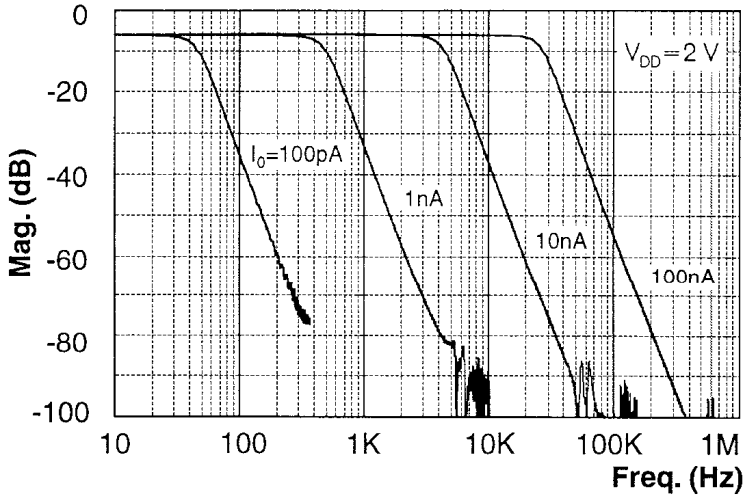


Figure 2.34 Large signal transfer function simulated for $m = 1$

demonstrate the correct operation of the filter even for large signals. The step amplitude is set equal to the bias current, but thanks to the class AB operation, the filter accepts

currents much larger than I_0. The DC gain variation over the 3 decades tuning range stays smaller than 0.2 dB. The effect of the non-linearities of the capacitors are negligible thanks to the small variation of the voltages and to the property of the LC ladder filter which have a small sensitivity to component variations (Fettweiss-Orchard theorem).

The total harmonic distortion (THD) has been evaluated for each cut-off frequency and is plotted in Fig. 2.35 versus the ratio of the input to bias current defined as the modulation index m. The THD for a cut-off frequency fixed at about 500 Hz is less than 1 % even for a modulation index as high as 30. The dynamic range is estimated to about 65 dB and the power consumption is 150 nW for a cut-off frequency of 500 Hz.

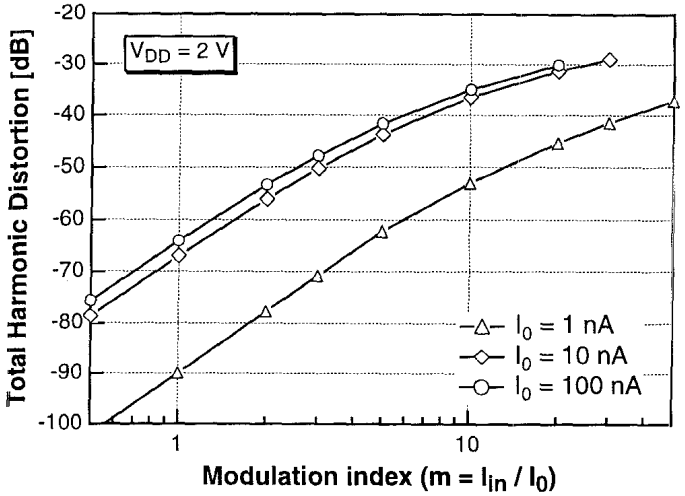


Figure 2.35 Simulation of the THD versus the input current normalized to the bias current (defined as the modulation index m)

Although log-domain filters seem to be very attractive for low-power and low-voltage, a considerable effort is still needed to better understand them and demonstrate their benefits for low-power and low-voltage analog signal processing applications.

1.2.7 Summary and conclusion

Unlike digital circuits where the dynamic power decreases with the square of the supply voltage, a first-order analysis shows that the minimum power consumption required to process analog signals is almost independent of the supply voltage reduction. This is mainly due to the fact that the power consumption of analog circuits at a given temperature is basically set by the required SNR and the frequency of operation (or the required bandwidth). A more detailed analysis indicates that this minimum power consumption of analog circuits is proportional to the ratio between the supply voltage and the signal peak-to-peak amplitude. Power efficient analog circuits should thus be designed to maximize the voltage swing and therefore should handle rail-to-rail signal voltages.

Many of the problems and solutions encountered in CMOS low-power analog circuit design are directly related to the properties of the MOS transistor itself, which must

therefore be properly understood and modelled down to very low currents. The essential features of a transistor can be captured in a symmetrical model where the drain current I_D is the superposition of a forward component I_F and reverse components I_R, which are proportional to the same function F of $V_P - V_S$ and $V_P - V_D$ respectively, where V_P is the pinch-off voltage which is directly related to the gate voltage. This function F is quadratic in strong inversion, while it is exponential in weak inversion. The proportionality factor is the specific current which depends on the aspect ratio of the device and defines a limit between weak and strong inversion. The ratio of the actual drain current to the specific current defines the inversion level or inversion factor of a MOS transistor in saturation. If this inversion factor is lower than one, the device operates in weak inversion. An inversion factor larger than one corresponds to a device operating in strong inversion and a transistor having an inversion factor close to one operates in the moderate inversion region. The transconductance-to-current ratio increases when the inversion factor is decreased and reaches a maximum in weak inversion. An unacceptable large error is made when estimating the effective transconductance of a transistor biased in the middle of the moderate inversion from the asymptotic expressions valid either in weak or in strong inversion. Continuous expression of the drain current as well as the transconductances are thus required for doing a correct sizing of each transistor operating in moderate inversion. Simple analytical expressions can be used and checked by simulation using for example the complete EKV MOST model. The scaling of advanced process is an additional motivation for having such a continuous analytical model, valid from weak to strong inversion. As a matter of fact, the scaling gradually shifts the specific current of a minimum size transistor to higher values of currents which for a given bias current progressively moves the corresponding inversion coefficient to lower values. In other words, for given performance, MOS transistors are more and more biased in the moderate or even in the weak inversion regions of operation.

The pinch-off voltage, the specific current and the inversion coefficient are not only abstract concepts which are only useful for the elaboration and formalism of the transistor model. These definitions show to be also very useful for designing efficient circuits. The pinch-off voltage can indeed be measured and is used for extracting the key parameters of the EKV model. It can also be generated from simple circuits and used for example to bias cascode stages. The specific current of a reference transistor can be generated by means of a dedicated circuit. It can then be used to precisely set the inversion coefficient of a device by simple scaling of this reference current using a series and/or parallel combination of reference transistors. This ratio-based design technique has the advantage to be insensitive to the first-order to temperature and process variations. It is therefore attractive for designing circuits that can be ported from one process to another without any major redesign while preserving the main performance.

The formulation of the drain current as the combination of a forward and a reverse component can be advantageously used to show that currents can be divided in given proportion among the branches of a network composed only of MOS transistors behaving as non-linear resistors. This property is valid independently of the current level and can be used for replacing any resistors of a resistive network by transistors. The same principle can also be used to realize a string of binary weighted current sources.

Voltage gain should be achieved by single-stage operational transconductance amplifier in order to avoid any compensation capacitor other than the load itself and therefore prevent any additional useless power consumption. The gain can be further increased without adding any extra current branch, by using a cascode stage which has to

be properly biased at the minimum voltage in order to preserve sufficient voltage swing.

In many analog signal processing applications, such as hearing aids for example, the input signal dynamic range is much larger than the required SNR. Hence, power can be saved if the SNR can be reduced to the minimum required while maintaining the necessary dynamic range. An ideal analog signal processing systems should even be able to maintain the SNR constant independently of the signal: when the signal is weak, the noise floor has to be low, when the signal is large the noise may be large as long as the required SNR is still achieved. This can be achieved by means of the analog floating point technique, which basically consists in scaling the input signal by an adequate factor adjusted in such a way that the signal fits within a given range. Distortions are avoided by correctly updating the state variables of the analog signal processor. This technique is obviously well adapted to analog sampled-data systems such as switched-capacitor circuits, since the updating can take place between two sampling instants leaving sufficient time for the undesirable but unavoidable transients to vanish. The analog floating point technique can also be applied to continuous-time analog signal processing systems as long as the state-variables are also updated continuously.

A possible way to maintain a sufficient dynamic range when reducing the supply voltage without degrading the power consumption of analog signal processing circuits is to use the instantaneous companding technique. In this approach, the currents are compressed when transformed into voltages and expanded when transformed back to currents. The input current has to be predistorted in order to preserve a linear operation. The expanding function is theoretically not restricted to the exponential function but since the predistortion of the signal requires the derivative of this expanding function, it is much easier to realize it using the exponential function since it is invariant to the differentiation operator and can be implemented either by the current-to-voltage characteristic of a bipolar transistor or a MOS transistor biased in weak inversion. The instantaneous voltage-companding technique additionally allows to extend the dynamic range while preserving the maximum g_m/I available in small-signal operation.

1.2.8 References

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