9 Switched Capacitor Circuits

Part 9.A—Switched capacitor basics

Consider the capacitors in Fig. 9.1. The charge on the capacitor is given by

$$Q = C \cdot (V_1 - V_2)$$

There is no DC current flowing through the capacitor.

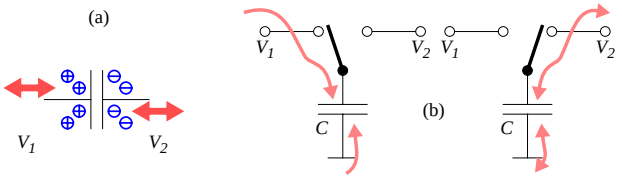

Figure 9.1: Capacitor (a) with its charges and (b) in a switched circuit.

In Fig. 9.1 (b) we show a switched capacitor. During half a time period $T/2$ one capacitor plate is connected to one node, V_1, and during the second time period it is connected to the other node, V_2. Hence, we are first going to charge the capacitance with

$$q_1 = C \cdot V_1$$

and then charge/discharge it with

$$q_2 = C \cdot V_2$$

The net charge transported from V_1 to V_2 is

$$\Delta q = q_1 - q_2 = C \cdot (V_1 - V_2)$$

During one time period, the average current is

$$I = \frac{\Delta q}{\Delta t} = \frac{\Delta q}{T} = \frac{C}{T} \cdot (V_1 - V_2) \text{ or } V_1 - V_2 = \frac{T}{C} \cdot I$$

This can be compared with Ohm's law and we see that the capacitor more or less operates as a resistance. However, it requires that T is very small, hence the frequency must be high.

We now have a way to implement an integrator with capacitors only (and an OP). In Fig. 9.2 we show the active-RC integrator and the "same" integrator but with the resistor replaced with the switched capacitor.Consider the case in Fig. 9.2 (b). One can "see" that during one phase the input capacitor is charged by the input voltage. During the next phase, the capacitor is discharged. One plate is connected to ground and the other is connected to the virtual ground at the input of the OP. The voltage over C_1 is 0 and therefore, the charge must be 0 as well. From one of the plates (bottom in the figure), the charge is transported downto ground and the charge from the other plate is transported to the feedback capacitor, since no current can move into the gates (CMOS OP). Thereby, the charge is accumulated (integrator function) on the feedback capacitor.

However, this configuration has some drawbacks, and we will get back to them in the next sections. The advantages with the switched-capacitor (SC) technique is that we now no longer need to implement resistors on the chip. We only implement capacitors (except for the OP's) and they can also be matched very well.

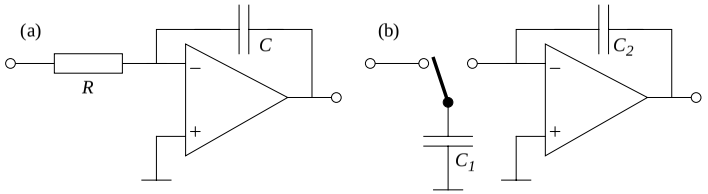

Figure 9.2: Active integrator with (a) RC components and (b) switched capacitor.

To further understand the operation of an SC circuit, we have to understand the concept of charge redistribution.

Part 9.B—Charge redistribution

We consider the different states (phases) of the circuit and investigate how the charge is transported when the switches are changed in the next phase of operation. First, consider these points:

- [A] Charge cannot change on an unconnected capacitor plate. The total sum of charge must be the same in a closed node in both phases.
- [B] It is only the output of a (voltage-controlled) operational amplifier that can add/remove charge.
- [C] A capacitor with equal potential on both plates is discharged.
- [D] If a capacitor is switched to a capacitor network, charge will redistribute and eventually reach equilibrium (if we assume that T is very long).

Examples on charge redistribution

Consider the case of the SC integrator as shown in Fig. 9.2. In Fig. 9.3 we depict both phases of operation. We shall now state the charges on the capacitors in both phases and describe the relations between the charge distribution in the two phases. First, it is convenient to define a reference direction on the capacitors. In our case, we have chosen the positive plate of the capacitors to be as shown with "+" in the figure.

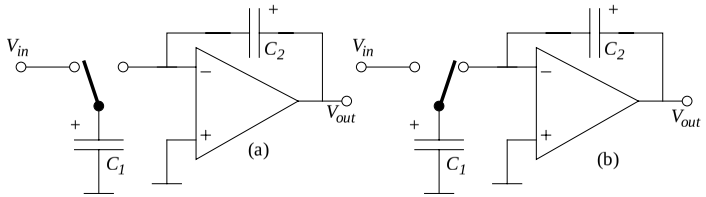

Figure 9.3: SC integrator at both phases.

Phase 1 at t (Fig. 9.3 (a))

$$q_1(t) = C_1 \cdot [V_{in}(t) - 0] = C_1 \cdot V_{in}(t)$$
$$q_2(t) = C_2 \cdot [V_{out}(t) - 0] = C_2 \cdot V_{out}(t)$$

Notice that the charge on the negative plate of C_2 during this phase is maintained according to statement [A]. Change the position of the switches and assume that the system settles within $T/2$.

Phase 2 at $t + T/2$ (Fig. 9.3 (b))

$$q_1(t + \frac{T}{2}) = C_1 \cdot [0 - 0] = 0$$
$$q_2(t + \frac{T}{2}) = C_2 \cdot \left[V_{out}(t + \frac{T}{2}) - 0\right] = C_2 \cdot V_{out}(t + \frac{T}{2})$$

The equations above do not give us any information on the actual transfer function. To achieve this, we must compare the two different phases and what happens in-between. We see that capacitor C_1 was discharged according to [C]. But according to [B] none of this charge can flow into the OP, it must flow to the negative plate of C_2. The charge on the negative plate is increased and the system must reach equilibrium [D] and the OP must add more charge to the positive plate of C_2 [B]. This [A+B+C+D] we can state with

$$q_2(t + \frac{T}{2}) = q_2(t) - q_1(t)$$

Notice the signs, we reduce the "negative" charge on C_2 with the "positive" charge from C_1. The result is

$$C_2 \cdot V_{out}(t + \frac{T}{2}) = C_2 \cdot V_{out}(t) + C_1 \cdot V_{in}(t)$$

However, we must close the loop and also investigate the first phase again, at the time point $t + T$.

Phase 1 at $t + T$

$$q_1(t + T) = C_1 \cdot [V_{in}(t + T) - 0] = C_1 \cdot V_{in}(t + T)$$
$$q_2(t + T) = C_2 \cdot [V_{out}(t + T) - 0] = C_2 \cdot V_{out}(t + T)$$

C_1 is charged with the input voltage and the charge on capacitor C_2 is conserved according to [A] and we have that

$$q_2(t + T) = q_2(t + T/2), \text{ hence } V_{out}(t + T) = V_{out}(t + T/2)$$

Gathering everything, we achieve the transfer function

$$C_2 \cdot V_{out}(t + T) = C_2 \cdot V_{out}(t) - C_1 \cdot V_{in}(t)$$

This can be z-transformed into

$$C_2 \cdot V_{out}(z) \cdot z = C_2 \cdot V_{out}(z) - C_1 \cdot V_{in}(z)$$

giving the transfer function

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1/C_2}{z - 1} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$

which typically is an accumulator function.

Non-overlapping switch signals

In Fig. 9.4 we show the concept of non-overlapping switch signal. This is to guarantee that the

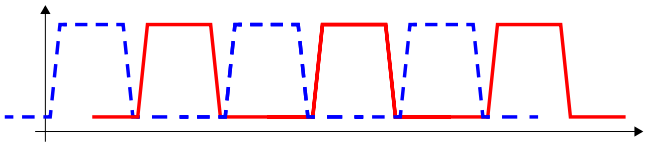

Figure 9.4: Non-overlapping switch signals in an SC circuit.

charge cannot be transferred in-between two phases. We have to guarantee that one switch is completely turned off before we switch on another.

Parasitic-sensitive SC integrator

This circuit in the previous example suffers from a crucial drawback due to the influence of parasitic capacitance. Consider the case again as shown in Fig. 9.5 with the parasitic capacitances added to the circuit. We have added parasitic capacitances to all nodes. Typically, parasitic capac-

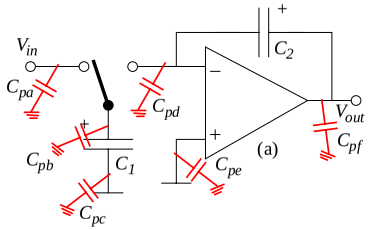

Figure 9.5: SC integrator with parasitic capacitances added.

itance are due to interconnection wires, overlap, gate-drain or gate-source voltages, switches, etc. We therefore want to design a circuit where the transfer function is as unaffected by the parasitic capacitances as possible. We examine all parasitic capacitances and check whether they can destroy the operation. We have

- C_{pa} ... will not affect the transfer function since it is always connected to the input node which is considered to be an ideal voltage source. Independent of the size of C_{pa}, there will still be V_{in} applied over C_1 during phase 1.
- C_{pb} ... is in parallel with C_1 and will influence in exact same way as C_1 throughout the analysis.
- C_{pc} ... is shorted between ground and ground and will not affect the transfer function.
- C_{pd} ... is shorted between ground and virtual ground and will not affect the transfer function.
- C_{pe} ... will not affect the transfer function as for C_{pd}.
- C_{pe} ... will not affect the transfer function with the same motivation as for C_{pa}.

We only have C_{pb} left which is connected in parallel with C_1 and hence will give the transfer function

$$H(z) = -\frac{C_1 + C_p}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$

Parasitic-insensitive SC integrator

Consider the SC circuit shown in Fig. 9.6 shown for both phases. We will first do a charge redis-

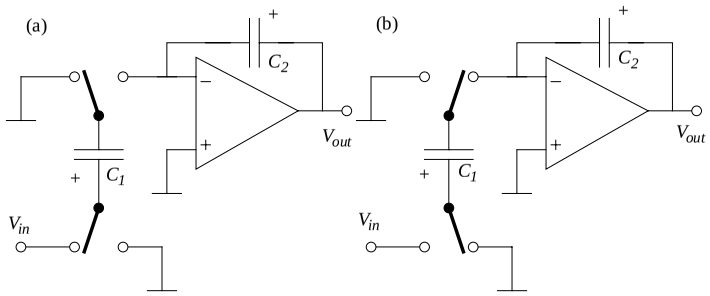

Figure 9.6: SC integrator at both phases.

tribution analysis. State the initial conditions at all phases, then investigate the relations between the phases.

Phase 1 at time t

$$q_1(t) = C_1 \cdot [V_{in}(t) - 0] = C_1 \cdot V_{in}(t)$$
$$q_2(t) = C_2 \cdot [V_{out}(t) - 0] = C_2 \cdot V_{out}(t)$$

Phase 2 at time $t + T/2$

$$q_1(t + \frac{T}{2}) = C_1 \cdot [0 - 0] = 0$$

$$q_2(t + \frac{T}{2}) = C_2 \cdot \left[V_{out}(t + \frac{T}{2}) - 0\right] = C_2 \cdot V_{out}(t + \frac{T}{2})$$

Phase 1 at time $t + T$

$$q_1(t + T) = C_1 \cdot [V_{in}(t + T) - 0] = C_1 \cdot V_{in}(t + T)$$
$$q_2(t + T) = C_2 \cdot [V_{out}(t + T) - 0] = C_2 \cdot V_{out}(t + T)$$

Between phase 1 and 2, we have that C_1 is discharged according to [C]. All its (negative plate) charge flows to the negative plate of C_2 according to [D].

$$q_2(t + \frac{T}{2}) = q_2(t) + q_1(t)$$

Between phase 2 and 1, we have that C_2 must keep its charge according to [A] and [B].

$$q_2(t + T) = q_2(t + \frac{T}{2}) \text{ and } V_{out}(t + T) = V_{out}(t + \frac{T}{2})$$

This gives that

$$C_2 \cdot V_{out}(t+T) = C_2 \cdot V_{out}(t+\frac{T}{2}) = C_2 \cdot V_{out}(t) + C_1 \cdot V_{in}(t)$$

The transfer function becomes

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}$$

Consider the influence of parasitic capacitances as illustrated in Fig. 9.7 where parasitics have

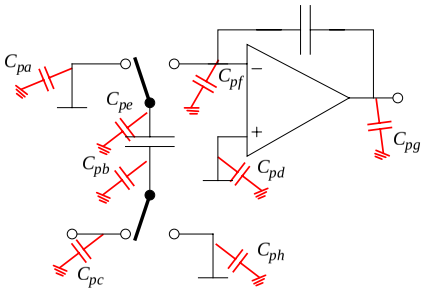

Figure 9.7: SC integrator with parasitic capacitances added.

been added to each node. We have eight capacitors and we have to check them all if they infleunce the transfer function.

- C_{pa} ... will not affect the transfer function since it is always shorted
- C_{pb} ... is in either connected to the input signal or to ground. As soon as it has been charged it is discharged during the next phase - and none of this charge floats into the rest of the net.
- C_{pc} ... will not affect the transfer function since it is always connected to the input node which is considered to be an ideal voltage source. Independent of the size of C_{pc}, there will still be V_{in} applied over C_1 during phase 1.
- C_{pd} ... is shorted between ground and virtual ground and will not affect the transfer function.
- C_{pe} ... will not affect the transfer function since it is always shorted, either to ground (phase 1) or virtual ground (phase 2).
- C_{pf} ... will not affect the transfer function with the same motivation as for C_{pd}.
- C_{pg} ... will not affect the transfer function with the same motivation as for C_{pc}.

Hence, there is no influence on the transfer function in this integrator.

Part 9.C—Speed of Switched-Capacitor Circuits

Notice, that in the previous, we only consider the static influence on performance. We have to be aware of the fact that the parasitic capacitances will affect the bandwidth and speed of the circuit.

Consider the integrator in Fig. 9.7. We know that if the amplifier is considered to be a single-pole system, the closed-loop bandwidth is approximately

$$\omega_{-3dB} = \beta \cdot \omega_u$$

where β is the feedback factor. At phase 1, the feedback factor is

$$\beta_1 = \frac{C_2}{C_2 + C_{pf}}$$

and the load capacitance is

$$C_L^{(1)} = C_L + C_{pg} + \frac{C_2 \cdot C_{pf}}{C_2 + C_{pf}}$$

At phase 2, the feedback factor is

$$\beta_2 = \frac{C_2}{C_2 + C_1 + C_{pf} + C_{pg}}$$

and the load capacitance is

$$C_L^{(2)} = C_L + C_{pg} + \frac{C_2 \cdot (C_1 + C_{pf} + C_{pe})}{C_1 + C_2 + C_{pf} + C_{pe}}$$

Assume that we have implemented a single-stage amplifier, such as folded-cascode or similar. We have that

$$\omega_u^{(i)} = \frac{g_m}{C_L^{(i)}}$$

Thereby, we can derive the -3dB frequencies for both phases:

$$\omega_{-3dB}^{(1)} = \frac{C_2}{C_2 + C_{pf}} \cdot \frac{g_m}{C_L + C_{pg} + \frac{C_2 \cdot C_{pf}}{C_2 + C_{pf}}} \text{ and}$$

$$\omega_{-3dB}^{(2)} = \frac{C_2}{C_2 + C_1 + C_{pf} + C_{pg}} \cdot \frac{g_m}{C_L + C_{pg} + \frac{C_2 \cdot (C_1 + C_{pf} + C_{pe})}{C_1 + C_2 + C_{pf} + C_{pe}}}$$

or

$$\omega_{-3dB}^{(1)} = \frac{C_2}{(C_L + C_{pg})(C_2 + C_{pf}) + C_2 \cdot C_{pf}} \cdot g_m \text{ and}$$

$$\omega_{-3dB}^{(2)} = \frac{C_2}{(C_L + C_{pg})(C_1 + C_2 + C_{pf} + C_{pe}) + C_2 \cdot (C_1 + C_{pf} + C_{pe})} \cdot g_m$$

etc.

Part 9.D—Influence of Non-Ideal OP

In reality, we suffer from a large number of non-idealties and it is not only parasitic capacitance that should be taken into account. We will discuss the influence of offset errors and limited gain of the amplifier. Consider the integrator in Fig. 9.8 where we have added the offset voltage source at the positive amplifier input. On the negative input, we have a voltage V_x originating from the

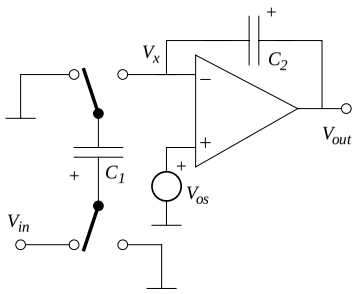

Figure 9.8: SC integrator including voltage offset and effect of limited amlifier gain.

fact that the amplifier gain is limited. Firts notice, that we can write

$$V_{out} = -A \cdot (V_x - V_{os}) \text{ hence } V_x = -\frac{V_{out}}{A} - V_{os}$$

We state the charge redistribution equations:

Phase 1 at time t

$$q_1(t) = C_1 \cdot [V_{in}(t) - 0] = C_1 \cdot V_{in}(t)$$

$$q_2(t) = C_2 \cdot [V_{out}(t) - V_x(t)] = C_2 \cdot \left[V_{out}(t) + \frac{V_{out}(t)}{A} + V_{os} \right] =$$

$$= V_{out}(t) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + V_{os} \cdot C_2$$

Phase 2 at time $t + T/2$

$$q_1(t + \frac{T}{2}) = -C_1 \cdot V_x(t + \frac{T}{2}) = C_1 \cdot \left(\frac{V_{out}(t + \frac{T}{2})}{A} + V_{os} \right) =$$

$$= \frac{C_1}{A} \cdot V_{out}(t + \frac{T}{2}) + C_1 \cdot V_{os}$$

$$q_2(t + \frac{T}{2}) = C_2 \cdot \left[V_{out}(t + \frac{T}{2}) - V_x(t + \frac{T}{2}) \right] =$$

$$= V_{out}(t + \frac{T}{2}) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + V_{os} \cdot C_2$$

Phase 1 at time $t + T$

$$q_1(t + T) = C_1 \cdot [V_{in}(t + T) - 0] = C_1 \cdot V_{in}(t + T)$$

$$q_2(t + T) = V_{out}(t + T) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + V_{os} \cdot C_2$$

We also know from the previous that

$$q_2(t + \frac{T}{2}) + q_1(t + \frac{T}{2}) = q_2(t) + q_1(t) \text{ and } q_2(t + T) = q_2(t + \frac{T}{2})$$

Yielding

$$V_2(t + T) = V_2(t + \frac{T}{2})$$

Which gives that

$$q_2(t + T) = q_2(t) + q_1(t) - q_1(t + \frac{T}{2})$$

Inserting the equations from above, we get

$$V_{out}(t + T) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + V_{os} \cdot C_2 =$$

$$= V_{out}(t) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + V_{os} \cdot C_2 + C_1 \cdot V_{in}(t) - \frac{C_1}{A} \cdot V_{out}(t + T) - C_1 \cdot V_{os}$$

We have that

$$V_{out}(t + T) = \frac{V_{out}(t) \cdot \left(1 + \frac{1}{A}\right) \cdot C_2 + C_1 \cdot V_{in}(t) - C_1 \cdot V_{os} - \frac{C_1}{A} \cdot V_{out}(t + T)}{\left(1 + \frac{1}{A}\right) \cdot C_2}$$

$$V_{out}(t + T) = V_{out}(t) + \frac{C_1/C_2}{1 + \frac{1}{A}} \cdot V_{in}(t) - \frac{C_1/C_2}{A + 1} \cdot V_{out}(t + T) - \frac{C_1/C_2}{1 + \frac{1}{A}} \cdot V_{os}$$

The DC term will be accumulated as well, and we see that it is very important to use a technique to remove this term. These techniques are referred to as auto-zeroing. However, z-transforming (and ignoring the DC-term from V_{os}), we have that

$$V_{out}(z) \cdot z = V_{out}(z) + \frac{C_1/C_2}{1 + \frac{1}{A}} \cdot V_{in}(z) - \frac{C_1/C_2}{A + 1} \cdot V_{out}(z) \cdot z$$

This gives the transfer function as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1/C_2}{1 + \frac{1}{A}} \cdot \frac{1}{z \cdot \left(1 + \frac{C_1/C_2}{A + 1}\right) - 1}$$

This is equal to

$$H(z) = \frac{C_1/C_2}{\left(1 + \frac{1}{A}\right) \cdot \left(1 + \frac{C_1/C_2}{A + 1}\right)} \cdot \frac{1}{z - \frac{1}{1 + \frac{C_1/C_2}{A + 1}}}$$

$$H(z) = \frac{C_1/C_2}{1 + \frac{1}{A}\cdot\left(1 + \frac{C_1}{C_2}\right)} \cdot \frac{1}{z - \frac{1}{1 + \frac{C_1/C_2}{A+1}}}$$

Hence, we have a gain error, the coefficient will not get the desired (designed-for) C_1/C_2 value. We will also shift the pole towards origo of the z-plane. Therefore, the integrator will become lossy. The relative error throughout the frequency plane is given by

$$\varepsilon(z) = \frac{1}{1 + A\cdot\frac{C_2}{C_1 + C_2}} \cdot \frac{z - \frac{C_2}{C_1 + C_2}}{z - \frac{1}{1 + \frac{C_1}{C_2\cdot(1+A)}}}$$