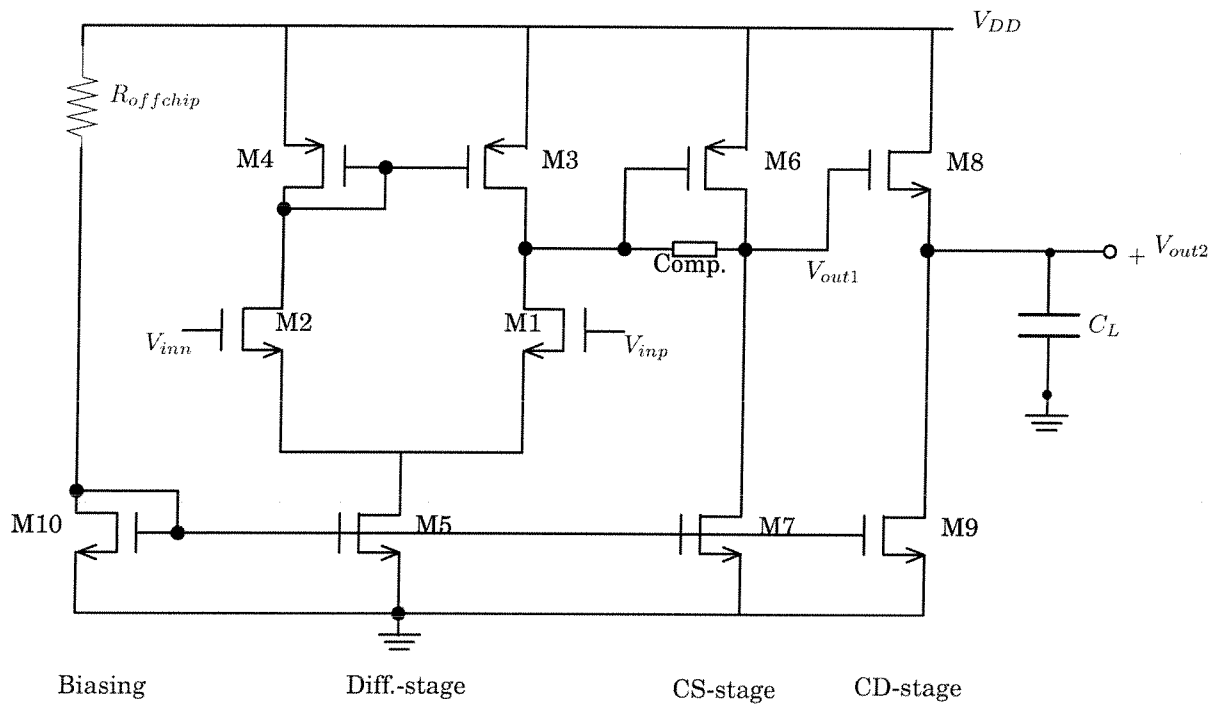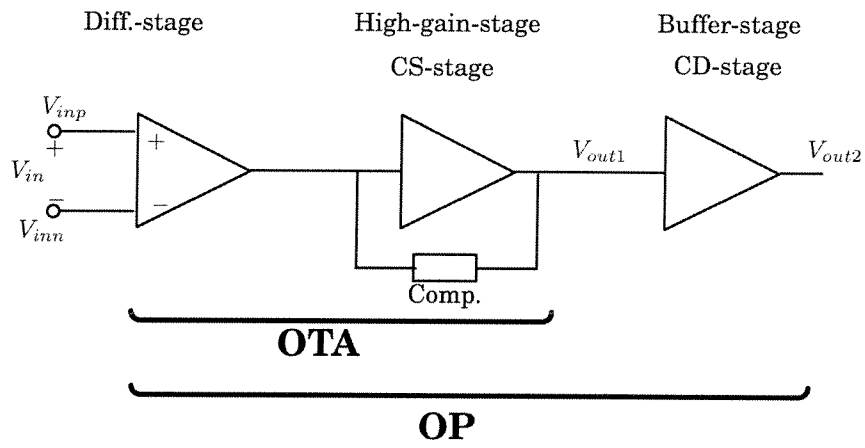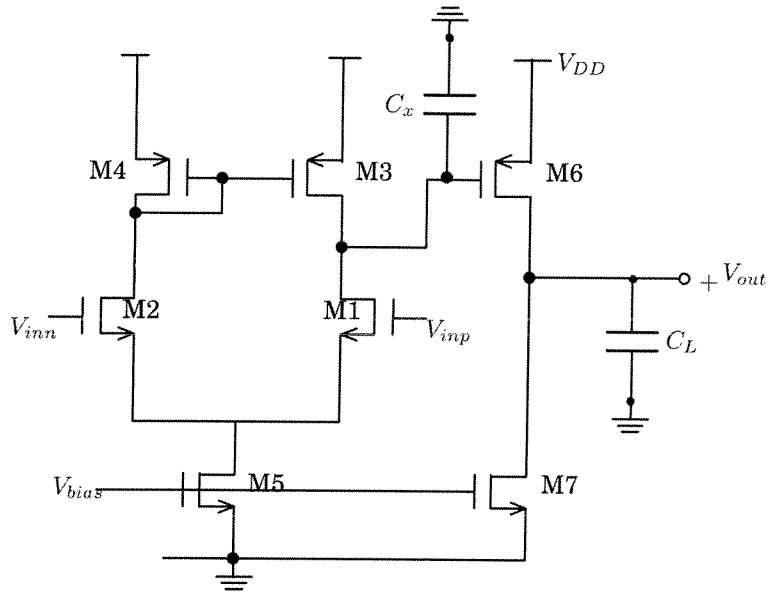**CONSTRUCTION TWO-STAGE OTA/OP**

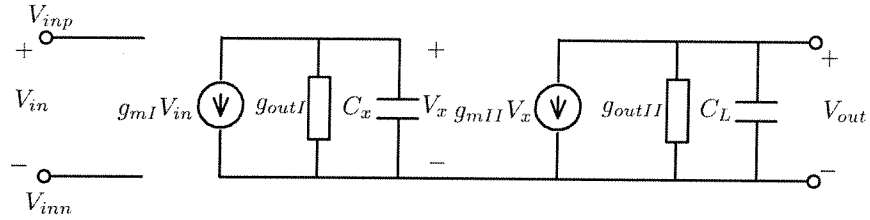Open-loop voltage gain $A_0 \approx A_{diff} \cdot A_{CS} \cdot A_{CD}$

$$A_{diff} \approx -\frac{g_{m1}}{g_{ds1} + g_{ds3}} \qquad A_{CS} \approx -\frac{g_{m6}}{g_{ds6} + g_{ds7}} \qquad A_{CD} \approx -\frac{g_{m8}}{g_{m8} + g_{ds8} + g_{ds9}}$$
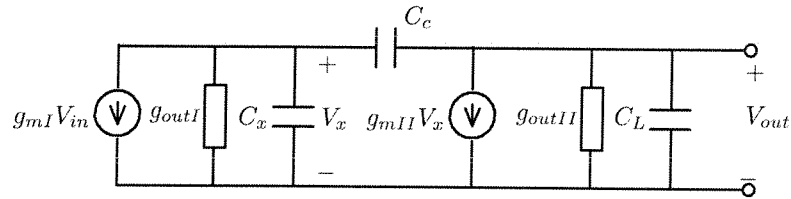
FREQUENCEY ANALYSIS OF TWO-STAGE OTA

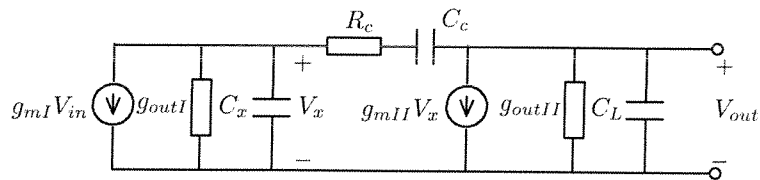Parasitic capacitance: $C_x = C_{gs6} + C_{db3} + C_{db1} + C_{dg6}(1 + A_{CS})$
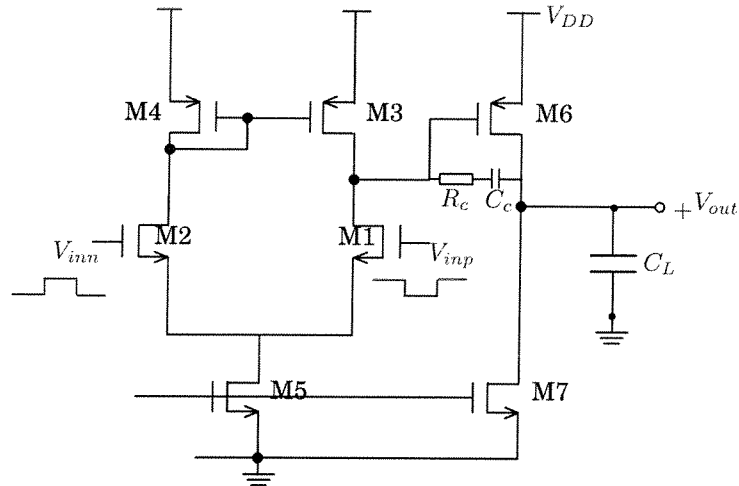
Small signal model:


Compensation with capacitor:

Compensation with RC-link (lead-compensation):

Slew Rate:

DESIGN OF TWO-STAGE OTA (with feed-back)

1. Max. power dissipation $P_{diss} \Rightarrow I_{max} \Rightarrow I_{D5}, I_{D6}$. ($P_{diss} = V_{DD}(I_{D5} + I_{D6})$)

2. Desired SR $\Rightarrow$ demands on I_5, I_6, C_c

3. Desired $\omega_u \Rightarrow$ demands on g_{m1}, $g_{m2} \Rightarrow W_1$, W_2

4. Desired A_0 and $p_2 \Rightarrow$ demands on W_7 (low parasitc C_x demands small W_3 and W_4, which gives large p_2.)

5. Counter-act systematical offset: Choose $\frac{W_7}{W_4} \approx 2\frac{W_6}{W_5}$

6. CMR maximum if V_{ds} small: Choose $V_{ds} = V_{ds,sat} \approx \sqrt{\frac{I_D}{\alpha_1}} = \sqrt{\frac{K I_D L_1}{W_1}} \Rightarrow W_1$, W_3 large
   In the same way: OR maximum $\Rightarrow W_6$, W_7 large

7. Choose the same length L for all transistors (1.5-2 times L_{min})

8. Controle poles positions and ω_u

9. Introduce compensation

TELESCOPIC CASCODE OTA
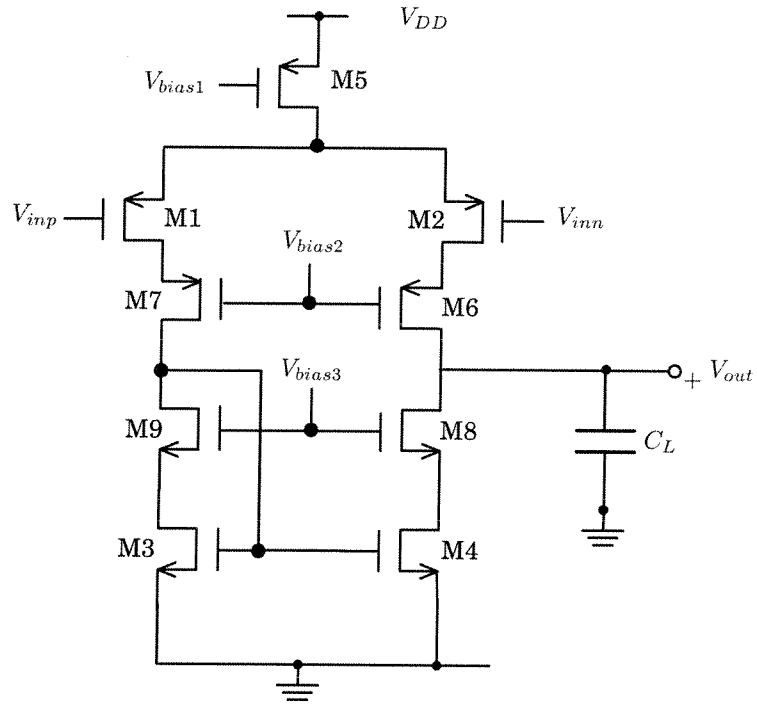
$$A_0 \approx \frac{g_{m2}}{g_{out}} \approx \frac{g_{m2}}{\frac{g_{ds6}g_{ds2}}{g_{m6}} + \frac{g_{ds8}g_{ds4}}{g_{m8}}}$$

$$p_1 \approx -\frac{g_{out}}{C_L}, \quad p_2 \approx -\frac{g_{m6}}{C_x}$$
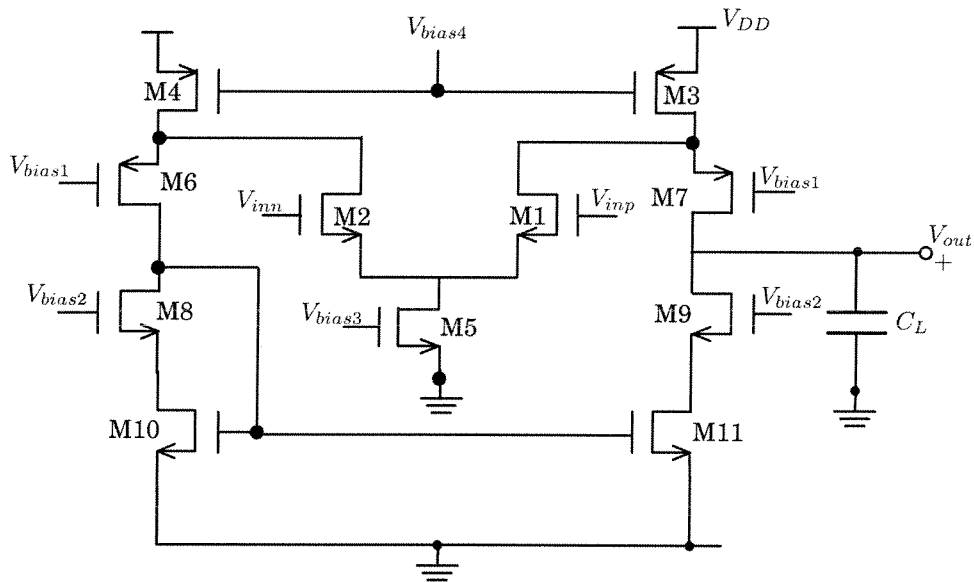
$$C_x = C_{gs6} + C_{sb6} + C_{db2}$$

$$\omega_u \approx A_0 \cdot |p_1| \approx \frac{g_{m2}}{C_L}$$

$$SR = \frac{I_{outmax}}{C_L} = \frac{I_5}{C_L}$$

Properties:

+ Fast

+ Simple construction

+ Low noise

+ Separated poles

− DC-out$\neq$ DC-in (gives problem when feed-back)

− Demands high power supply

− Low input swing and output swing

FOLDED-CASCODE OTA

$$A_0 \approx -\frac{g_{m1}}{g_{out}}$$

$$g_{out} \approx \frac{(g_{ds1} + g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds9}g_{ds11}}{g_{m9}}$$

$$p_1 \approx -\frac{g_{out}}{C_L}, \qquad p_2 \approx -\frac{g_{m7}}{C_x}$$

$$C_x = C_{gs7} + C_{sb7} + C_{db3} + C_{dg3} + C_{db1}$$

$$\omega_u \approx |A_0| \cdot |p_1| \approx \frac{g_{m1}}{C_L}$$

$$SR = \frac{I_{outmax}}{C_L} = \frac{I_{D3}}{C_L}$$

Properties:

+ DC-out = DC-in possible

+ Separated poles

+ Low power supply possible

− Sensitive for load C_L

DESIGN OF FOLDED-CASCODE OTA

1. $I_{tot} = I_{D5} + 2I_{D7} = 2I_{D3} < \frac{P_{dissmax}}{V_{DD}}$

2. $SR_{min} < SR = \frac{I_3}{C_L} = \frac{\frac{I_{D5}}{2} + I_{D7}}{C_L}$ (common to choose $I_{D1} \approx 4I_{D7}$ for high g_{m1})

3. Desired A_0. Increase A_0 by:

   - increasing g_{m1} and (g_{m2}) i.e. increase W_1(and W_2) (gives however decreasing $|p_2|$)
   - increasing g_{m6}, g_{m7} and g_{m8}, g_{m9} (increase W_6, W_7, W_8, W_9). (Gives however decreasing $|p_2|$ because
   $g_{m7} \propto \sqrt{W_7}$ while $C_x \propto W_7$.)
   - using gain-boosting

4. Maximize CMR and OR (see below)

5. To increase ω_u increase W_1 or increase I_{D5}. ($g_m \propto \sqrt{W I_D}$)

6. Too bad phase margin?

   - Add more capacitors to the output
   - Add a resistor in series with this capacitor

Large signal analysis gives:

CMR

$$V_{in,min} = V_{DSsat5} + V_{GS1} = V_{DSsat5} + V_{DSsat1} + V_{T1} \propto \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}/2}{\alpha_1}} + V_{T1}$$

$$V_{in,max} = V_{DD} - V_{DSsat3} - V_{DSsat1} + V_{GS1} = V_{DD} - V_{DSsat3} - V_{DSsat1} + V_{DSsat1} + V_{T1} \propto V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} + V_{T1}$$

OR

$V_{out,min}$ is the maximum value of following two expressions:

$$V_{DSsat11} + V_{DSsat9} \propto \sqrt{\frac{I_{D7}}{\alpha_{11}}} + \sqrt{\frac{I_{D7}}{\alpha_9}}$$

and

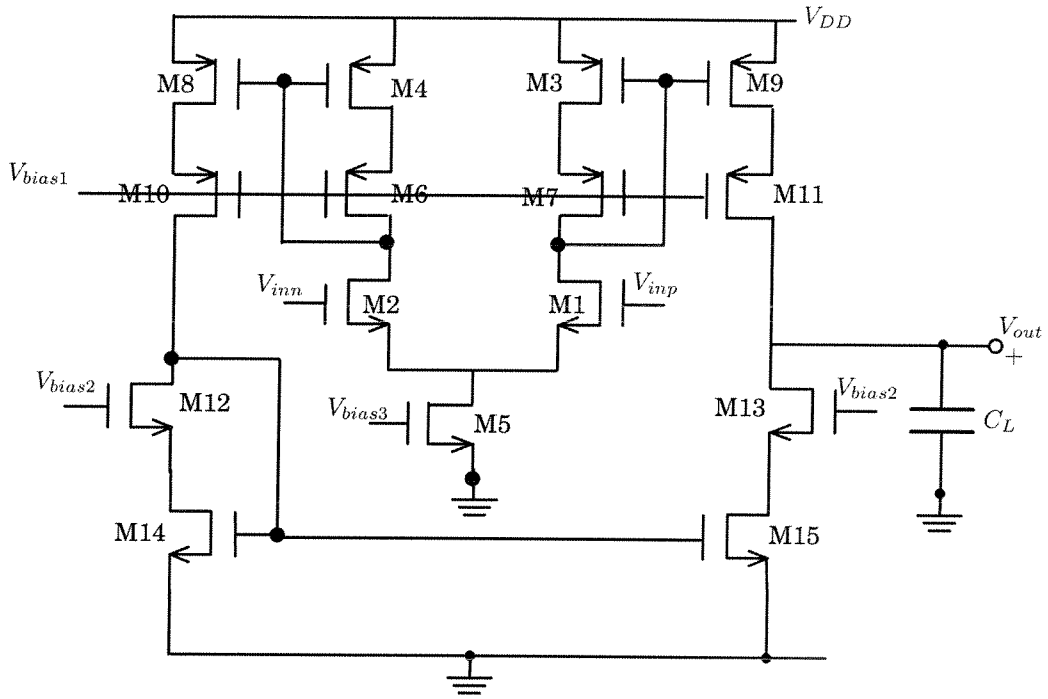$$V_{bias2} - V_{GS9} + V_{DS9} = V_{bias2} - V_{t9}$$

$V_{out,max}$ is the minimum value of following two expressions:

$$V_{DD} - V_{DSsat3} - V_{DSsat7} \propto V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} - \sqrt{\frac{I_{D7}}{\alpha_7}}$$
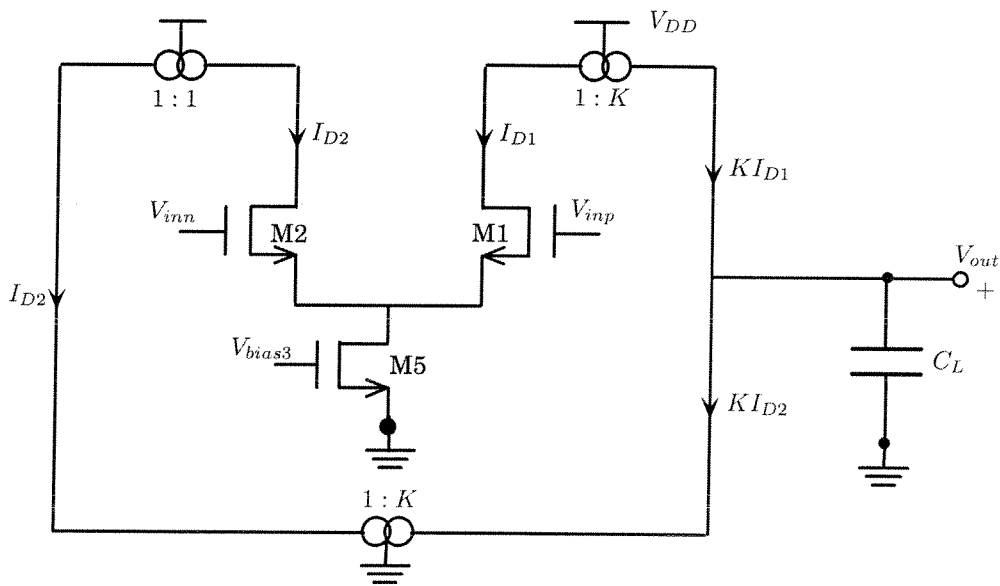
and

$$V_{bias1} + V_{SG7} - V_{SD7} = V_{bias1} + V_{t7}$$

CURRENT MIRROR OTA

Principle scheme:

CURRENT MIRROR OTA:

$$A_0 \approx \frac{K g_{m1}}{g_{out}} \qquad K = \frac{g_{m9}}{g_{m3}}$$

$$g_{out} \approx \frac{g_{ds11} \cdot g_{ds9}}{g_{m11}} + \frac{g_{ds13} g_{ds15}}{g_{m13}}$$

$$p_1 \approx -\frac{g_{out}}{C_L} \,, \quad p_2 \approx -\frac{g_{m3}}{C_x}$$

$$C_x = C_{gs3} + C_{gs9} + C_{db7} + C_{db1}$$

$$\omega_u \approx A_0 \cdot |p_1| \approx \frac{K g_{m1}}{C_L}$$

$$SR = \frac{I_{outmax}}{C_L} = \frac{K I_{D5}}{C_L} \quad \text{(M2 blocks whereby } I_{D1} = I_{D5})$$

Increasing K gives: 1) Increasing A_0. 2) Increasing ω_u. 3) Increasing SR. 4) Decreasing $|p_2|$ as larger K demands larger g_{m9} (i.e. larger W_9) which gives larger C_x.

Properties:

+ Large bandwidth

+ Large SR

− Large thermal noise

− Demands large compensation capacitor C_c

DESIGN OF CURRENT MIRROR OTA

1. $I_{tot} = I_{D5} + K I_{D1} + I_{D1} = \frac{(K+3) I_{D5}}{2} < \frac{P_{dissmax}}{V_{DD}}$

2. $SR_{min} < SR = \frac{K I_5}{C_L}$ (choose $K \leq 5$)

3. Desired A_0. Increase A_0 by:

   − increasing g_{m1} (and g_{m2}) i.e. increasing W_1 (and W_2)
   − increasing g_{m11} and g_{m13}
   − decreasing current on the output

4. Increase CMR and OR by increasing transistor widths (W_i) or decreasing currents

5. To increase ω_u increase W_1 or K

6. Too bad phase margin?

   − Add more capacitors to the output
   − Add a resistor in series with this capacitor