Lecture 5, ATIK

Switched-capacitor circuits 1
Basics, Accumulators

LiU EXPANDING REALITY

What did we do last time?

Differential circuits

- Why differential?
- CMRR, CMR

Operational amplifiers

- More on how we design them
- Cookbook recipes
- PSRR

Circuit noise

- Thermal and flicker noise
- Noise bandwidth

What will we do today?

Switched capacitor operation

- Charge redistribution
- Parasitics

Typical building blocks

- Accumulators

Switched capacitor - Background

Resistors are **evil**... bulky and noisy and nonlinear

Inductors are **evil** ... bulky and have low Q value

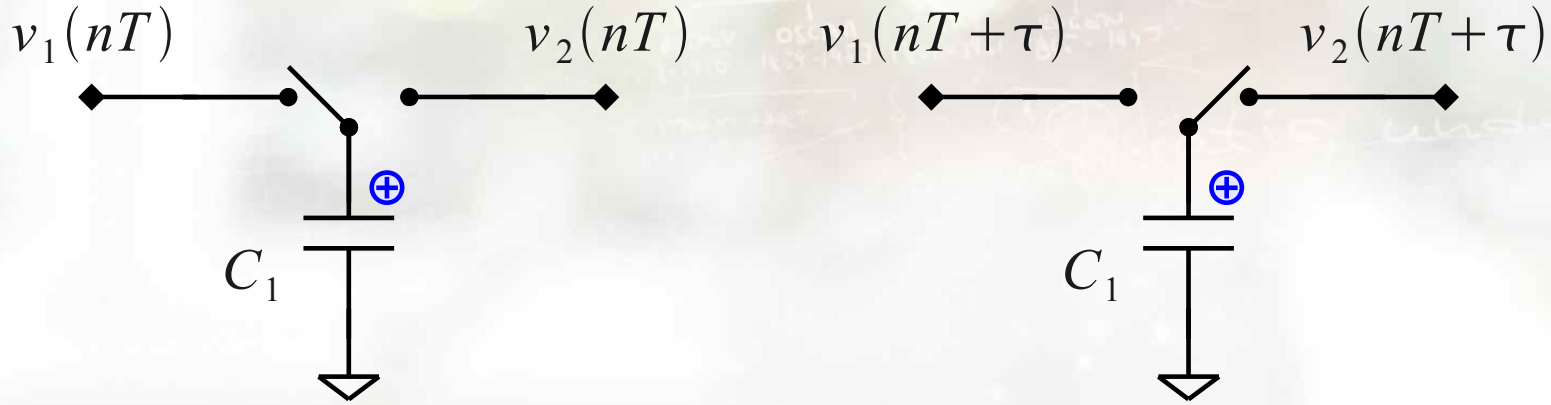
In CMOS design, we want to stick to transistors and capacitors

(preferrably only the transistors)

How can we mimick a resistor using transistors and capacitors

Switched capacitor

The first trial



First phase:

$$q_1(nT) = C_1 \cdot v_1(nT)$$

$$v_2(nT) = v_2(nT-\tau)$$

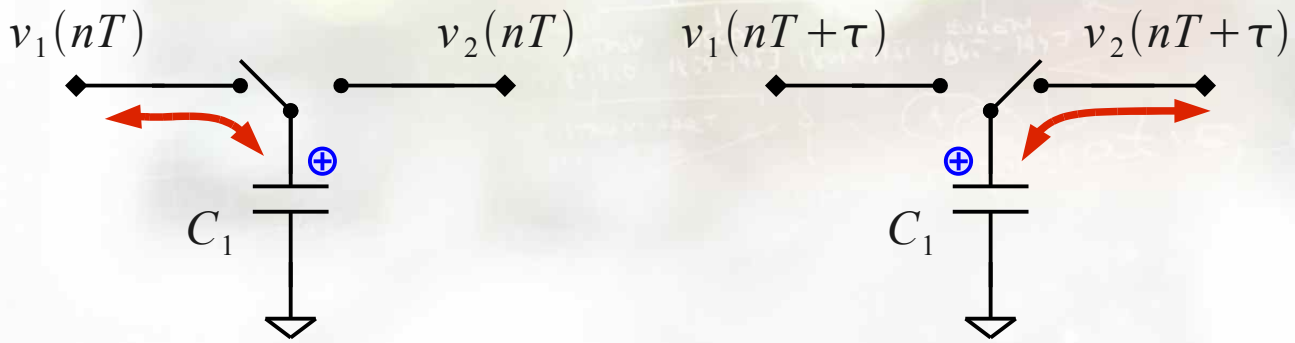
Second phase:

$$q_1(nT+\tau) = C_1 \cdot v_2(nT+\tau)$$

$$v_1(nT+\tau) = ?$$

Switched capacitor, cont'd

The transferred charge



The net charge

$$\Delta Q(nT+\tau)=q_1(nT+\tau)-q_1(nT)=C_1\cdot\left(v_2(nT+\tau)-v_1(nT)\right)$$

The average current during one period

$$I_{avg}=\frac{\Delta Q(nT+\tau)}{T}=\frac{C_1}{T}\cdot\left(v_2(nT+\tau)-v_1(nT)\right)$$

Switched capacitor, cont'd

Compiled

$$I_{avg}(nT+\tau)=\frac{C_1}{T}\cdot\left|v_2(nT+T)-v_1(nT)\right|=\frac{C_1}{T}\cdot\Delta V(nT+\tau)$$

Simulates a resistance

$$R_{eq}=\frac{T}{C_1}$$

With shorter sampling periods, the resistance decreases

- Less charge is transported in average

The larger capacitor, the resistance decreases

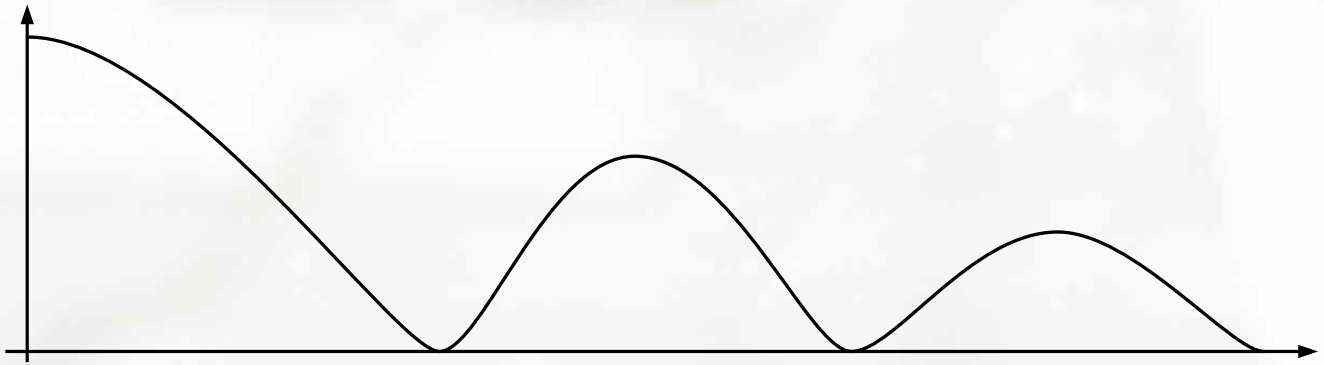
- More current can be handled

Characteristics

When is this assumption valid?

> We're taking an average of something, indicating signal frequency has to be small compared to sample frequency

Pulse-amplitude modulated signal (PAM)



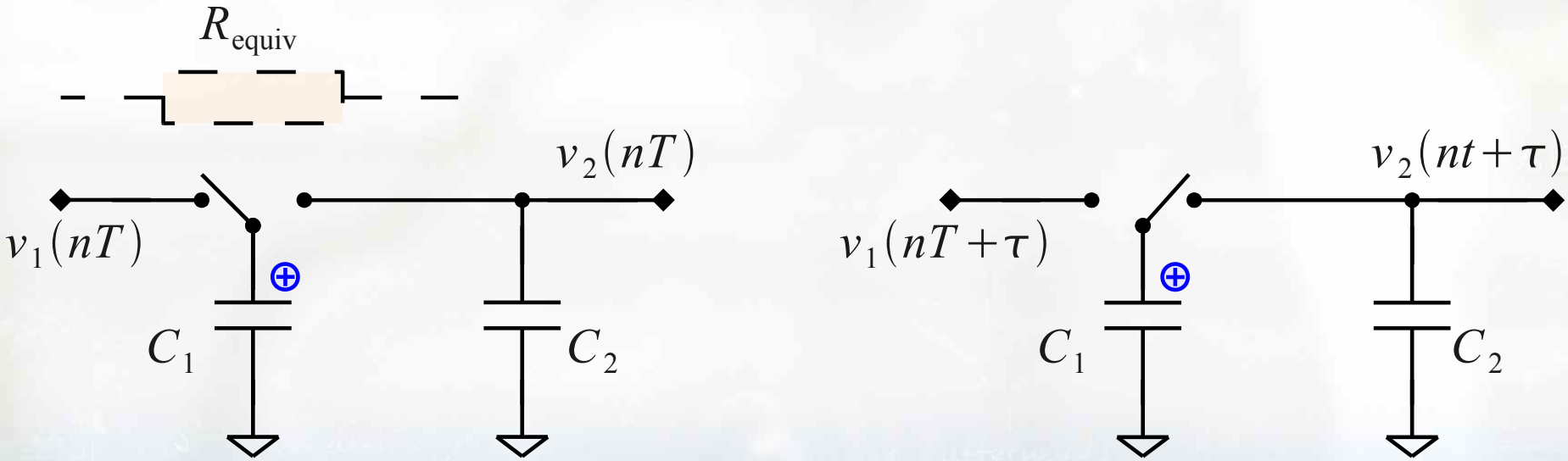
We should look at the flat areas where attenuation is low.

$$f_{signal} \ll f_{sample}$$

Using the switched capacitor: An RC link

A first-order (incorrect!) analysis

$$\frac{V_2(s)}{V_1(s)} = \frac{1}{1+\frac{s}{1/R_{eq}C_2}} \approx \frac{1}{1+\frac{sT}{C_1/C_2}}$$



We get a capacitor ratio instead!

Why are ratios better? And why should we use pears with pears?

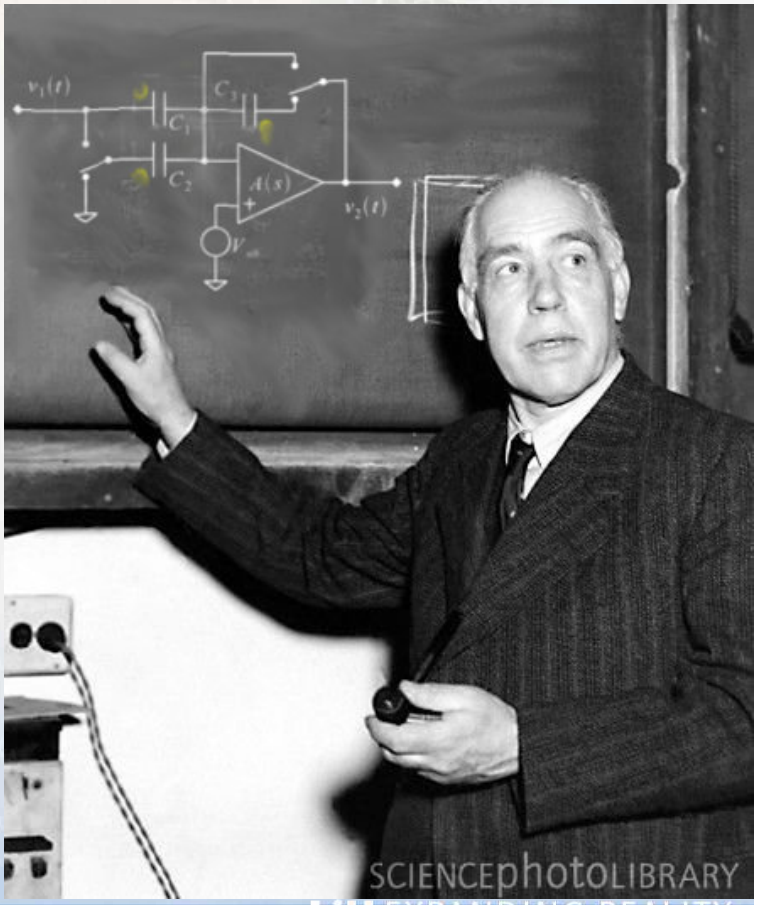
A ratio gives

$$\frac{C_1+\Delta C_1}{C_2+\Delta C_2}=\frac{C_1}{C_2}\cdot\frac{1+\frac{\Delta C_1}{C_1}}{1+\frac{\Delta C_2}{C_2}}=\frac{C_1}{C_2}\cdot\frac{1+\rho_1}{1+\rho_2}\approx$$

$$\frac{C_1}{C_2}\cdot(1+\rho_1)\cdot(1-\rho_2)\approx\frac{C_1}{C_2}\cdot(1-\rho^2)$$

Whereas a product gives

$$(C+\Delta C)\cdot(R+\Delta R)=RC\cdot(1+\rho_C)\cdot(1+\rho_R)\approx$$
$$RC\cdot(1+2\rho+\rho^2)$$



Using the switched capacitor: An RC link

A first-order (correct!) analysis.

(Notice that C2 "steals" charge during one phase.)

Phase 1:

$$V_2(nT)=V_2(nT-\tau) \text{ and } q_1(nT)=C_1\cdot V_1(nT)$$

Phase 2:

$$q_2(nT+\tau)=C_2\cdot V_2(nT+\tau) \text{ and } q_1(nT+\tau)=C_1\cdot V_2(nT+\tau)$$

Charge must be preserved on the two caps:

$$q_1(nT+\tau)+q_2(nT+\tau)=q_1(nT)+q_2(nT)$$
$$(C_1+C_2)\cdot V_2(nT+\tau)=C_1\cdot V_1(nT)+C_2\cdot V_2(nT)$$
$$(C_1+C_2)\cdot V_2(nT+T)=C_1\cdot V_1(nT)+C_2\cdot V_2(nT)$$

Use the frequency domain!

$$(C_1+C_2)\cdot z\cdot V_2(z)-C_2\cdot V_2(z)=C_1\cdot V_1(z)\Rightarrow\frac{V_2(z)}{V_1(z)}=\frac{C_1}{(C_1+C_2)z-C_2}$$

Using the switched capacitor: An RC link

Do a mathematically "incorrect" substitution

When is this assumption valid?

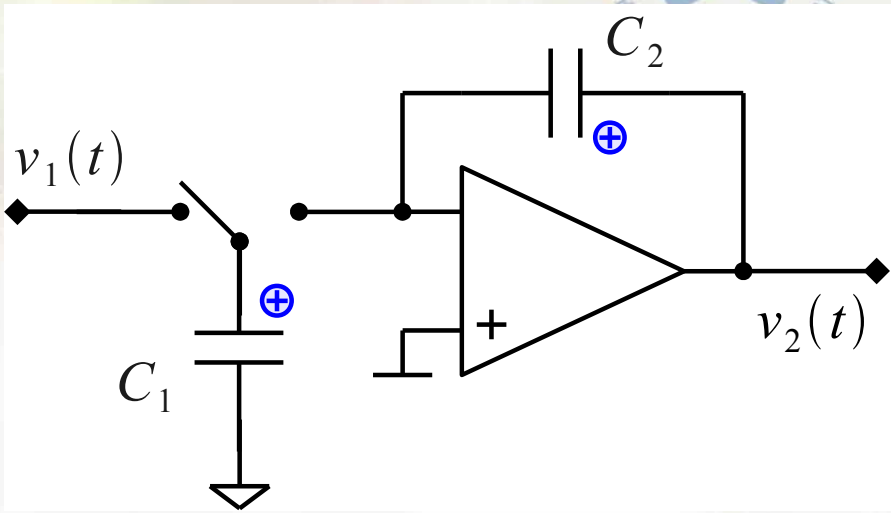
$$\frac{V_2(s)}{V_1(s)} = \frac{C_1}{(C_1+C_2)e^{sT}-C_2} \approx \frac{C_1}{(C_1+C_2)(1+sT)-C_2} = \frac{C_1}{C_1+(C_1+C_2)sT} = \frac{1}{1+\frac{sT}{\frac{C_1}{C_1+C_2}}}$$

The capacitors are not isolated from each other

- Loss in bandwidth
- the factor can never be larger than 1 (!)

Using the SC: Active integrator

The input capacitor will see virtual ground and thus not C2



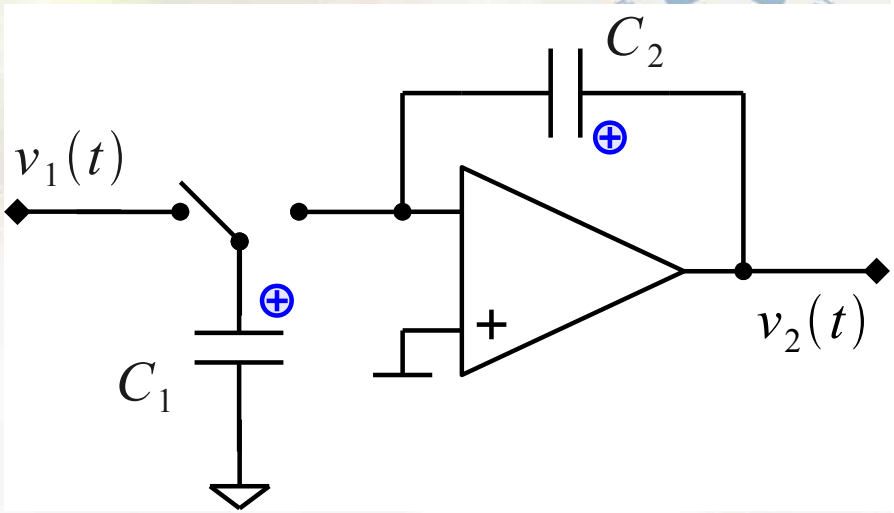
Use the standard continuous-time approach

$$\frac{V_2(t)}{V_1(t)} \approx \frac{-1}{s R_{eq} C_2} = \frac{-C_1/C_2}{s T}$$

The virtual ground will effectively drain C_1 in every second phase, i.e., the charge drop is independent on C_2.

Charge redistribution analysis, phase 1

However, just replacement is not accurate enough!



Input capacitor

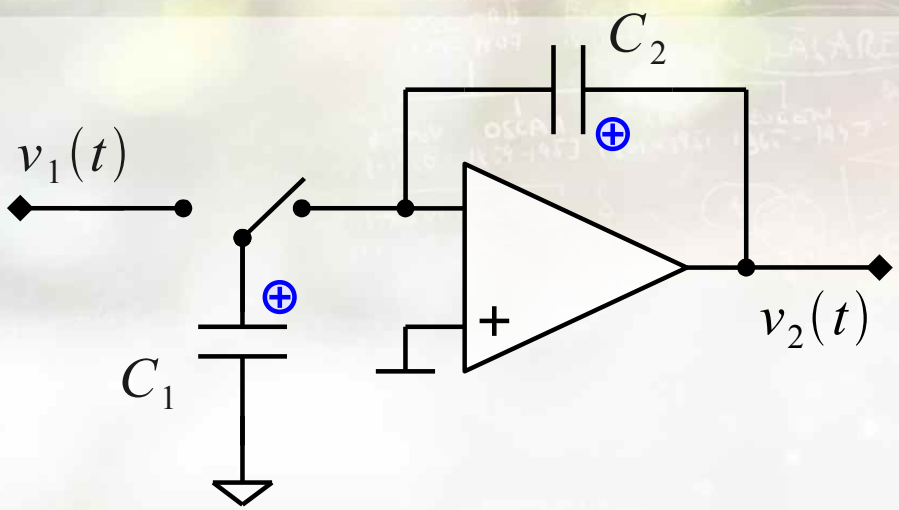
$$q_1(nT) = C_1 \cdot V_1(nT)$$

Storage capacitor

$$q_2(nT) = C_2 \cdot \left(V_2(nT) - 0\right) = C_2 \cdot V_2(nT)$$

Notice the "sign" of the capacitors. These are aid markers only.

Charge redistribution analysis, phase 2



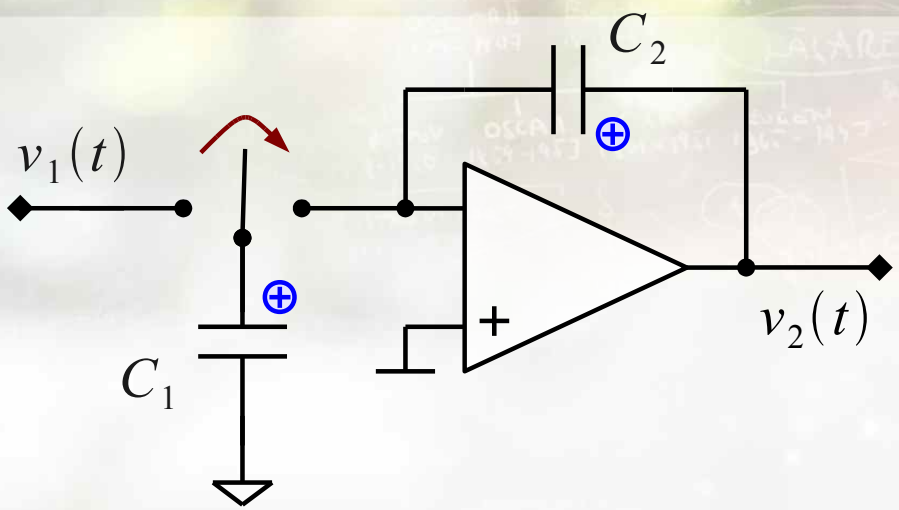
Input capacitor

$$q_1(nT+\tau)=C_1\cdot(0-0)=0$$ (Emptied !)

Storage capacitor

$$q_2(nT+\tau)=C_2\cdot\left(V_2(nT+\tau)-0\right)=C_2\cdot V_2(nT+\tau)$$

Charge redistribution analysis, 1 to 2

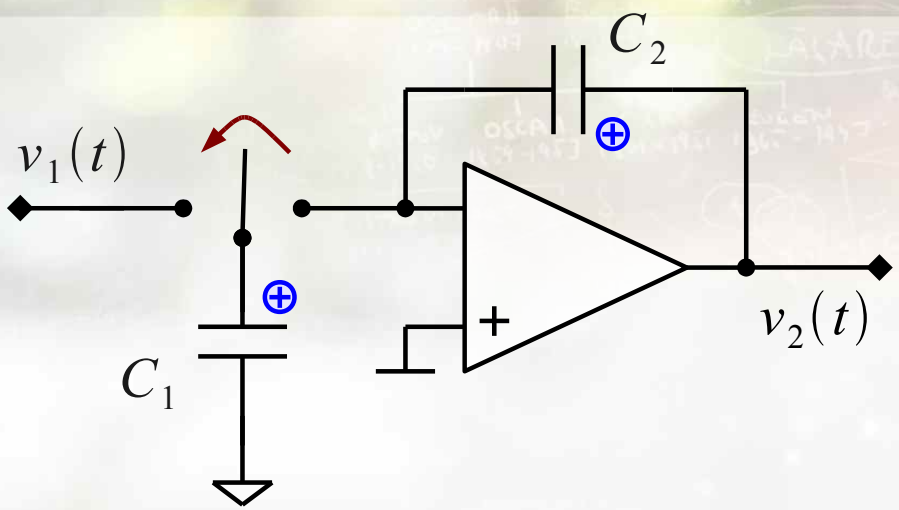


The charge in the system must be preserved!

"Positive" charge on C_1 will float to "negative" plate of C_2.

$$q_2(nT+\tau)=-q_2(nT)-q_1(nT)$$

Charge redistribution analysis, 2 to 1



The "negative" charge on C_2 cannot disappear, the voltage across capacitor is preserved:

$$q_2(nT+T)=q_2(nT+\tau)$$

Input capacitor is recharged

Charge redistribution analysis, compiled

Instanteneous charging

$$q_1(nT)=C_1\cdot V_1(nT)$$

$$q_2(nT)=C_2\cdot V_2(nT)$$

Charge preservation

$$-q_2(nT+\tau)=-q_2(nT)+q_1(nT)$$

$$q_2(nT+T)=q_2(nT+\tau)$$

Combined

$$C_2\cdot V_2(nT+T)-C_2\cdot V_2(nT)=-C_1\cdot V_1(nT)$$

Go to frequency domain

$$C_2\cdot V_2(z)\cdot(z-1)=-C_1\cdot V_1(z)\Rightarrow\frac{V_2(z)}{V_1(z)}=\frac{-C_1/C_2}{z-1}$$

Charge redistribution analysis, checked

Once again, the sloppy frequency transform

$$z = e^{sT} \approx 1 + sT$$

Insert

$$\frac{V_2(z)}{V_1(z)} = \frac{-C_1/C_2}{1 + sT - 1} = \frac{-C_1/C_2}{sT}$$

Now, the two formulas correlate!

Caveats

"High" sample frequency

"High" unity-gain frequency

Low on-resistance

Linear capacitors

Buffers required

- Passive SC implies losses

If we go to a sampled system, e.g. ADC, we can utilize whole frequency band! (Revisited in discrete-time filter design).

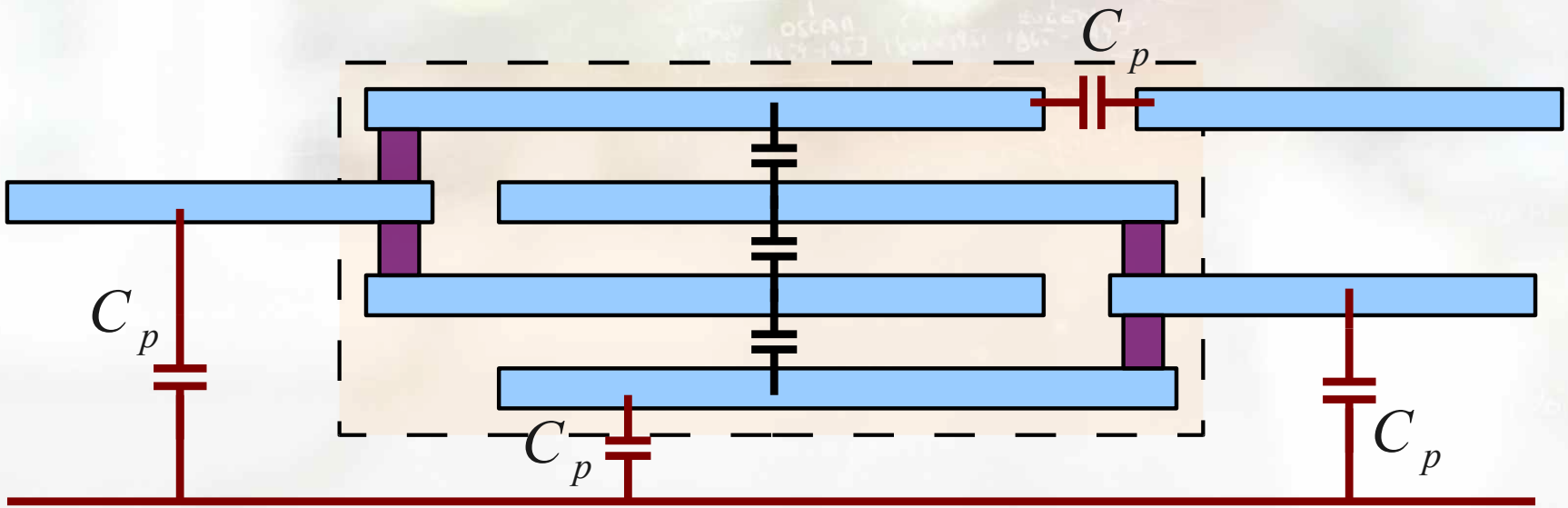
Switched-capacitor in a context

- Filters
- Sigma-delta modulators
- Sample-and-hold
- Gain circuits
- Common-mode feedback circuits
- Comparators
- Auto-zeroing
- Reset circuits

Accumulators/integrators are vital building blocks in many applications

Parasitics, or a capacitor is not ideal

Sandwhiched capacitor in four metal layers



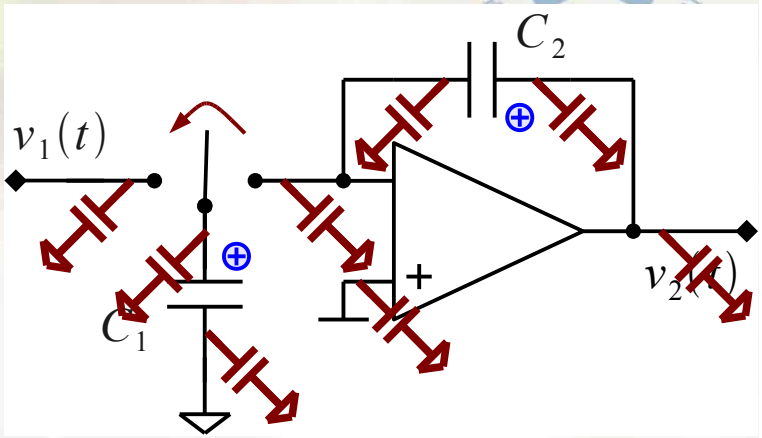
Examples on parasitics

- Bottom-plate parasitics
- Fringing capacitance to near-by objects
- Overlap capacitance (if accuracy is required)

Parasitics, sensitive example

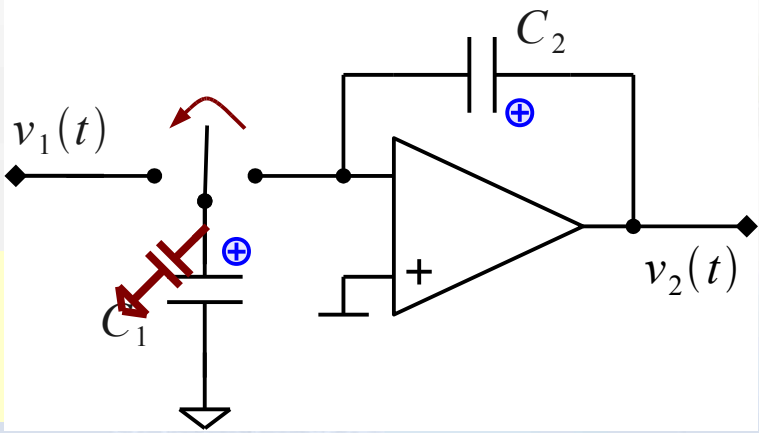
Add parasitics "everywhere"

- Each switch
- Each capacitor plate
- Each OP node



Cancel those that do not influence the results

- Voltage sources
- Virtual grounds
- Grounded

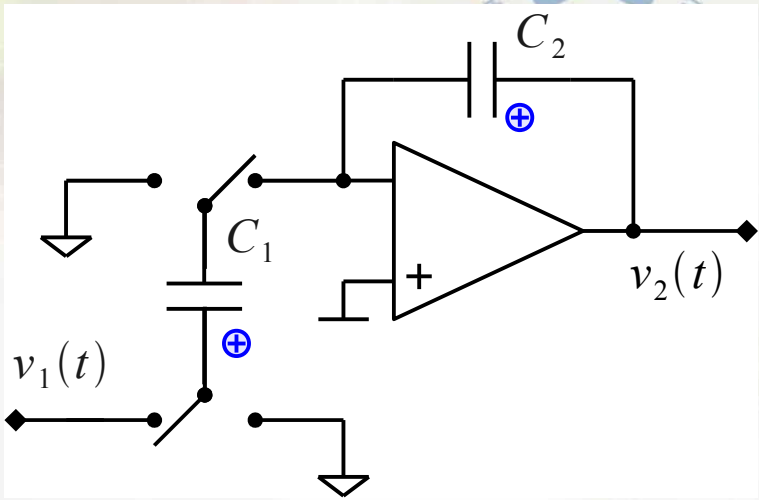


One left!

Effectively changing the value of C1.

Parasitics, insensitive example

This is also an accumulator



Phase 1:

$$q_1(nT)=C_1\cdot V_1(nT),\ q_2(nT)=C_2\cdot V_2(nT)$$

Phase 2:

$$q_1(nT+\tau)=0,\ q_2(nT+\tau)=C_2\cdot V_2(nT+\tau)$$

Charge preservation:

$$q_2(nT+\tau)=q_2(nT)\Rightarrow V_2(nT+\tau)=V_2(nT)$$

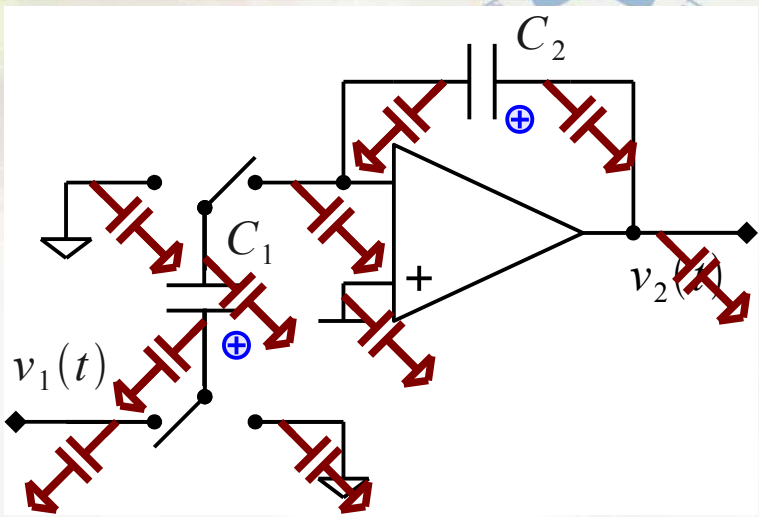
$$-q_1(nT)-q_2(nT)=-q_1(nT-\tau)-q_2(nT-\tau)=-q_2(nT-T)$$

$$C_1\cdot V_1(z)=-C_2\cdot\left(1-z^{-1}\right)\cdot V_2(z)\Rightarrow V_1(z)V_2(z)=\frac{-C_1/C_2}{1-z^{-1}}$$

Parasitics, insensitive example

Add parasitics "everywhere"

- Each switch
- Each capacitor plate
- Each OP node



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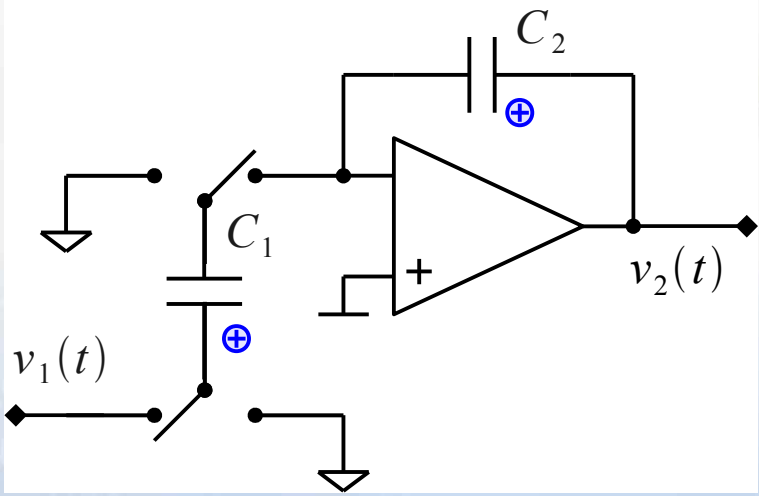

Parasitics, the check list

These can be ignored:

- continuously connected to input voltage source (ideal) or to OP (ideal) outputs (Ideal sources can give/take as much charge as needed)
- connected between ground-ground or between "ground-virtual ground" in both phases (the effective charge is zero all the time)
- charged from a voltage source or OP during one phase and is discharged to ground during next phase
- capacitor plates that are charged during one phase and not connected during next phase

These have to be considered

- charged from a voltage source or OP during one phase and discharged to a sensitive (another capacitor plate or virtual ground) during next phase

What did we do today?

Switched capacitor circuits

- The basics
- Charge-redistribution analysis

Nonidealties

- SC parasitics

What will we do next time?

Switched capacitor circuits with nonideal effects in mind

- What should we look out for?
- What is the impact on system performance, like filters.

Continuous-time filters

Switched capacitor revisited during

- Discrete-time filter lectures
- Data converter lectures