Lecture 3, Amplifiers 2

Improved gain towards OP, OTA, Stability
Tuesday, January 29, 2013

LiU EXPANDING REALITY

What did we do last time?

Went through the most common CMOS building blocks

Common-Gate, Common-Drain, Common-Source

Quickly discussed voltage swing

With lower v_{eff} the swing increases (and so does the gain).

Mismatch

Impact on the minimum, v_{eff}, i.e., don't make v_{eff} too low!

Still wrapping-up the smallest bits and pieces!

What did we do last time?

Gain (g_m/g_{out}) and pole (g_{out}/C_L) and trade-offs between them

$$A(s)=\frac{A_0}{1+\frac{s}{p_1}}=\frac{\frac{g_m}{g_{out}}}{1+\frac{s}{\frac{g_{out}}{C_L}}}$$

Increase gain by

increasing transconductance or output impedance

What will we do today?

Current mirrors

- Swing

Improved gain through cascodes

Stability

- Phase margin
- Compensation (first glance)

Amplifiers and differential pairs

- Why differential?

Current mirrors revisited

Use the current mirrors for biasing

Set the current through the gain stage with a reference current to decouples design parameters!

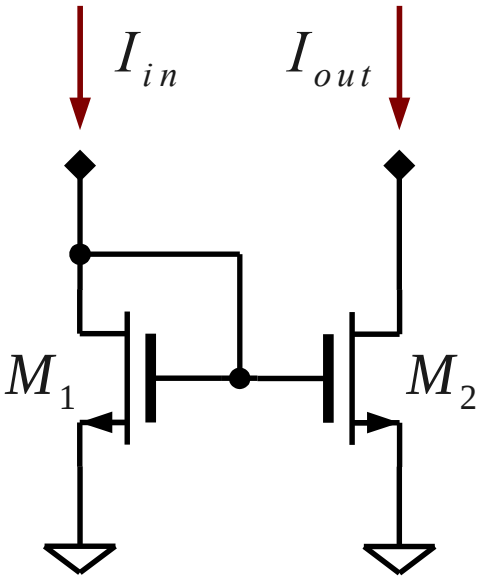
$$I_{out} = \frac{\alpha_2}{\alpha_1} \cdot I_{in}$$

We can "ignore" the size and v_{eff} of the bias transistor (active load) and focus on current instead.

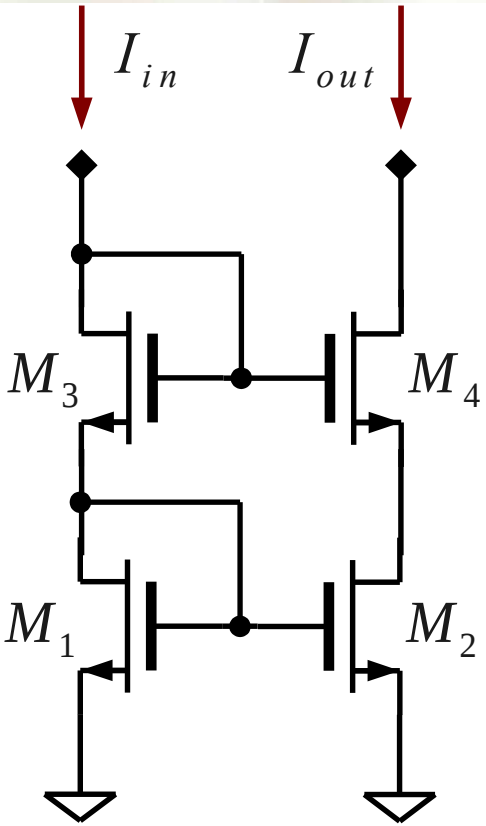
For reference termination

At the "receiver", a simple resistor will do to generate a ground-independent voltage level

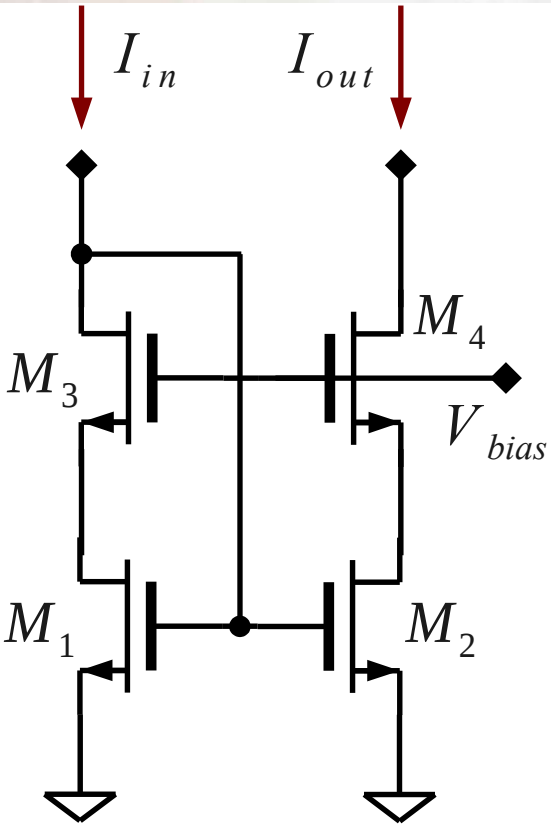
Current mirrors, cont'd



(a) Simple



(b) Cascode



(c) Wideswing

Current mirrors, some maths

Swing

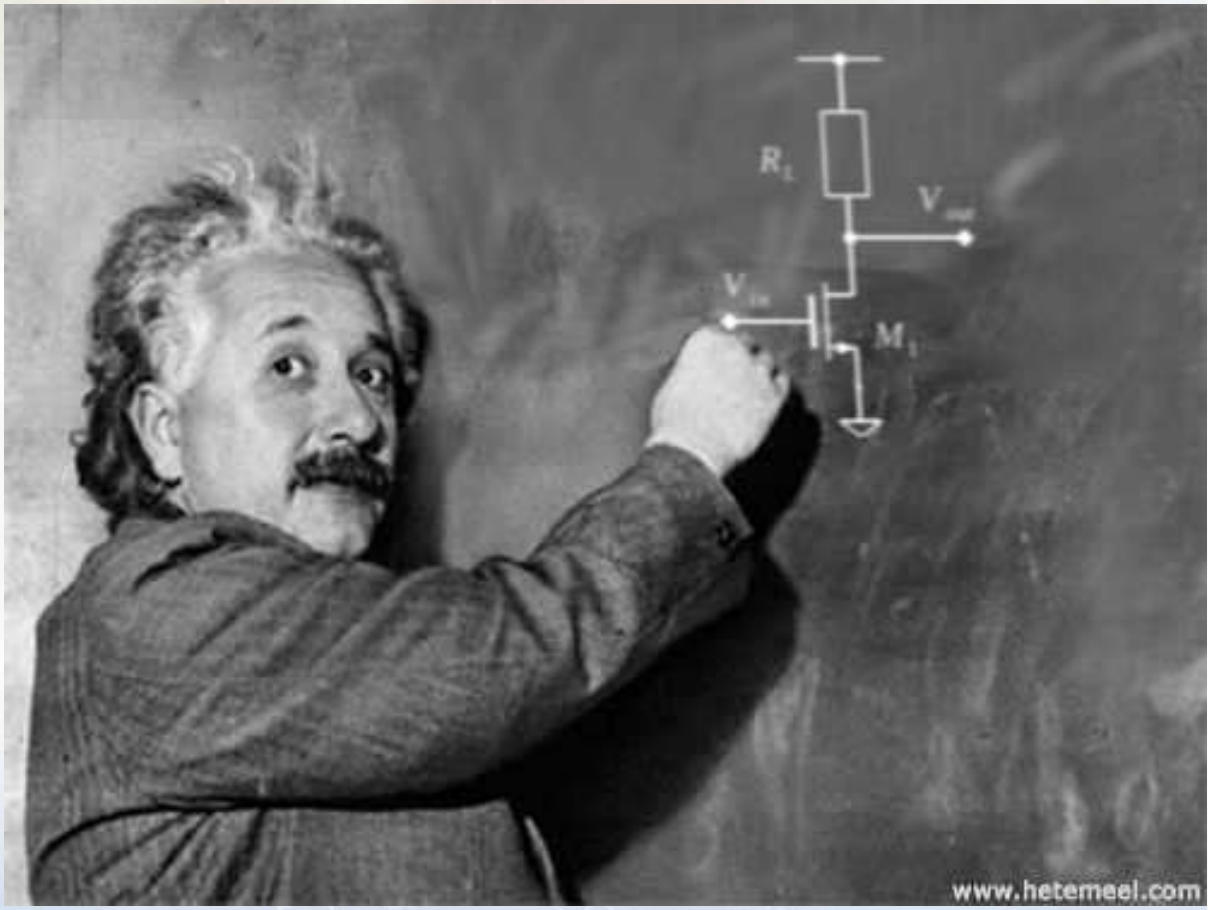
How many can we stack?

Current source

Input impedance

Output impedance

"High-impedance" load



Ok, so there were some extra transistors there... Cascodes

Eats up the voltage headroom

For every diode-connected transistor, we loose one V_T of swing

The wideswing current mirror approach should be used

Concludingly, cascodes increase the gain

(How? - a small-signal exercise)

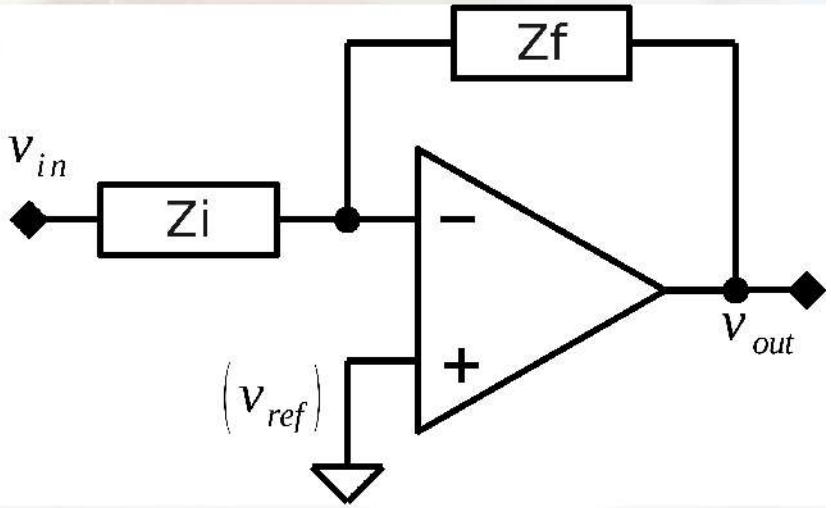
Why do I increase my gain?

Why do we need high gain?

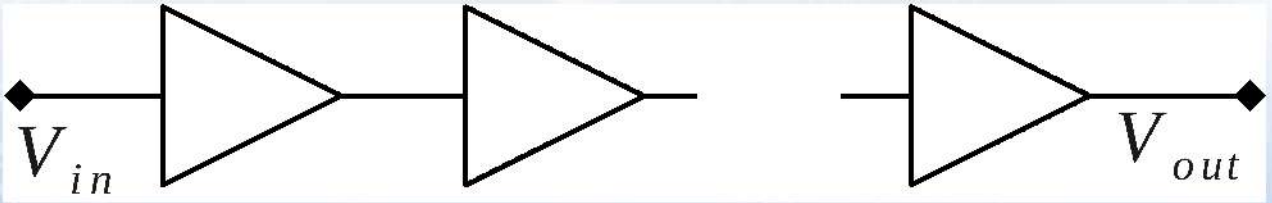
Supresses nonlinearity and offset errors (c.f. control theory)

Closed-loop gain control:

$$\frac{V_{out}}{V_{in}} = \frac{Z_f}{Z_i}$$



One solution is multiple gain stages



How do I increase my gain?

Assuming a simple common-source stage:

$$A = \frac{g_m}{g_{ds}} = \frac{1}{\lambda \cdot v_{eff}} = \frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$$

Answer depends on the biasing conditions

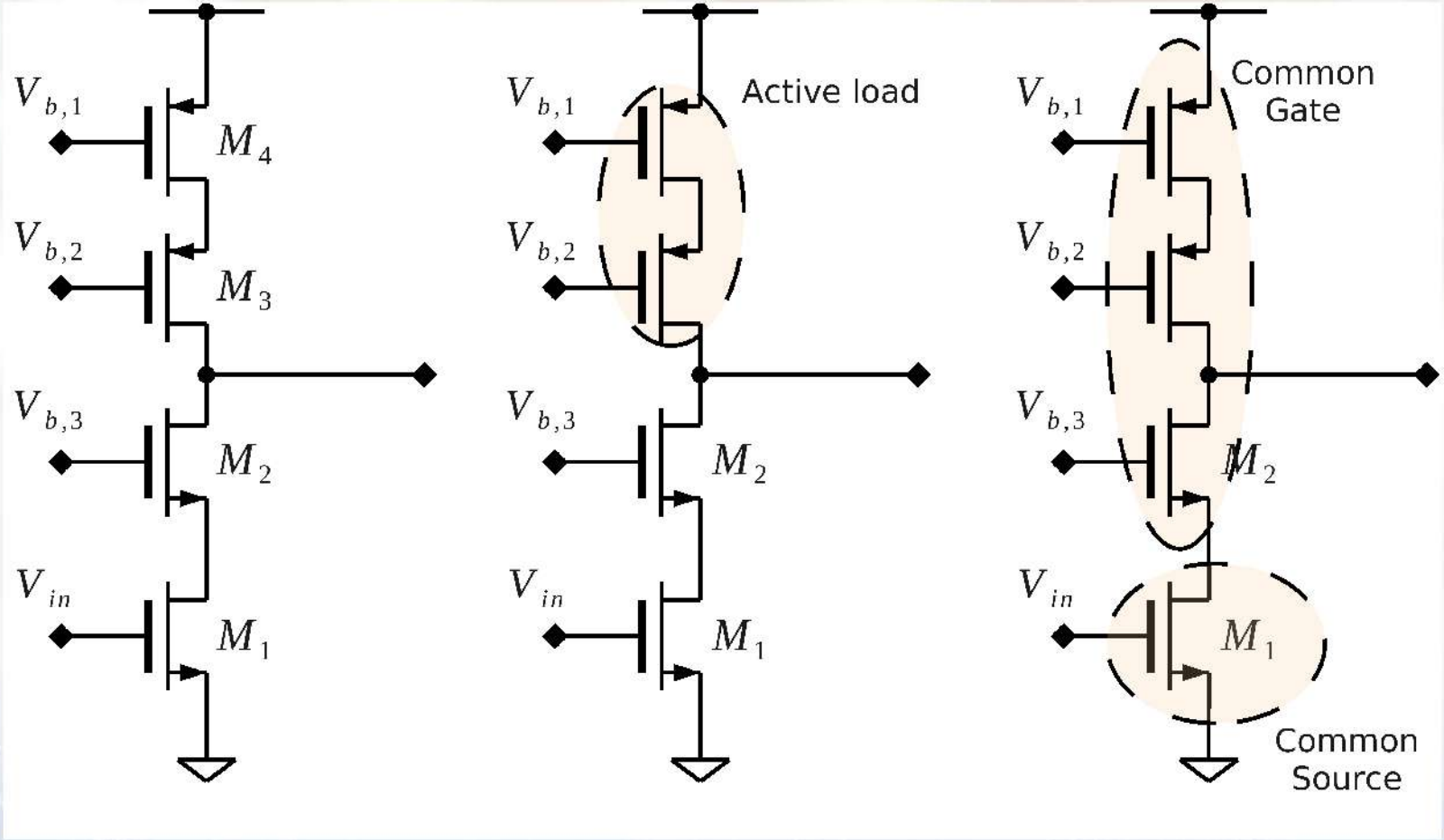
Decrease v_{eff}

Decrease $\lambda \sim 1/L$, i.e., increase the channel length.

Decrease (!) the current I_D

Increase the transistor aspect ratio, $\alpha \sim S \sim W$

How do I increase my gain?



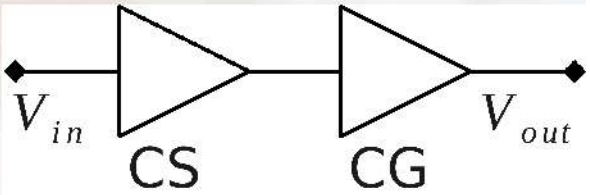
Multi-stage or cascodes?

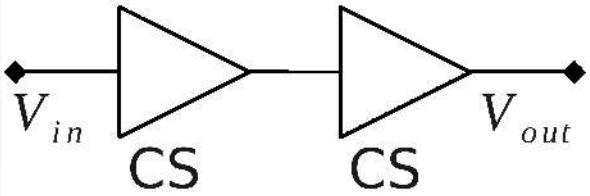
Single-stage (cascodes) vs two-stage?

They will have the same DC gain

They will not have the same output impedance

Multiple poles ("one per stage")





The transfer function (in both cases) is

$$A(s) \approx \frac{A_1 \cdot A_2}{\left(1+\frac{s}{p_{11}}\right)\cdot\left(1+\frac{s}{p_{12}}\right)}$$

Multiple poles

Case 1 (CS+CG)

First amplifier sees low-impedance load: $(g_1+g_{m1})\|C_1 \approx g_{m1}\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Case 2 (CS+CS)

First amplifier sees high-impedance load $(g_1+0)\|C_1 \approx g_1\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Notice the Case-2 g_2 is higher than the Case-1 g_2

Multiple poles, cont'd

Bode plot

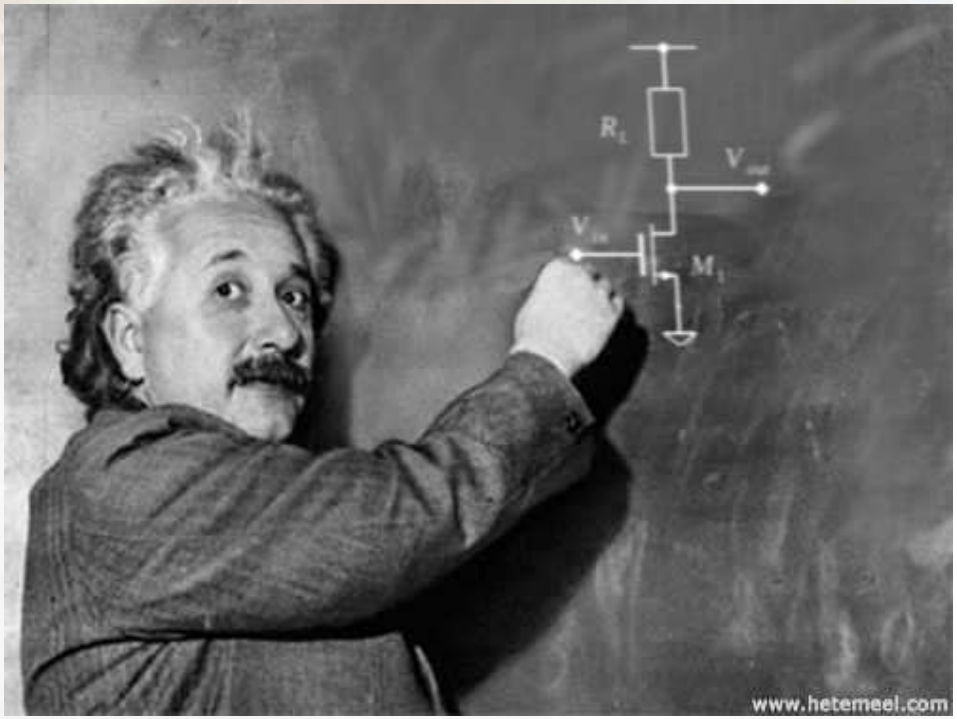
-90 degrees per pole

-20 dB/dec per pole

Phase margin

Compared to x-axis

ϕ_m is the distance at the crossing point, i.e., the phase margin



Regardless what you do ... Feedback

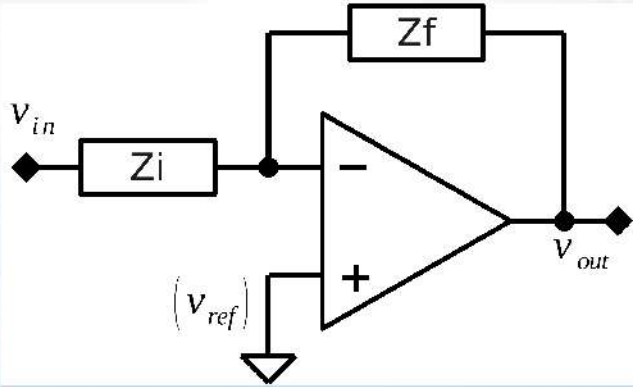
Preferrably, a controlled system, with a closed-loop gain of:

$$Y(s)=\left(X(s)-\beta(s)\cdot Y(s)\right)\cdot A(s)\Rightarrow$$

$$\frac{Y(s)}{X(s)}=\frac{A(s)}{1+\beta(s)\cdot A(s)}=\frac{1/\beta(s)}{1+\frac{1}{\beta(s)\cdot A(s)}}$$

A feedback factor of: $\beta(s)$

An open-loop gain of: $\beta(s)\cdot A(s)$



Stability

In short: the transfer function must be designed such that

$$\beta(s)\cdot A(s)\neq -1$$

If this is the case, we have an infinitely high transfer function

(In reality, the proof is quite complex.)

Phase margin (how far are we off from this to happen)

Poor phase margin gives ringing in the output when applying step

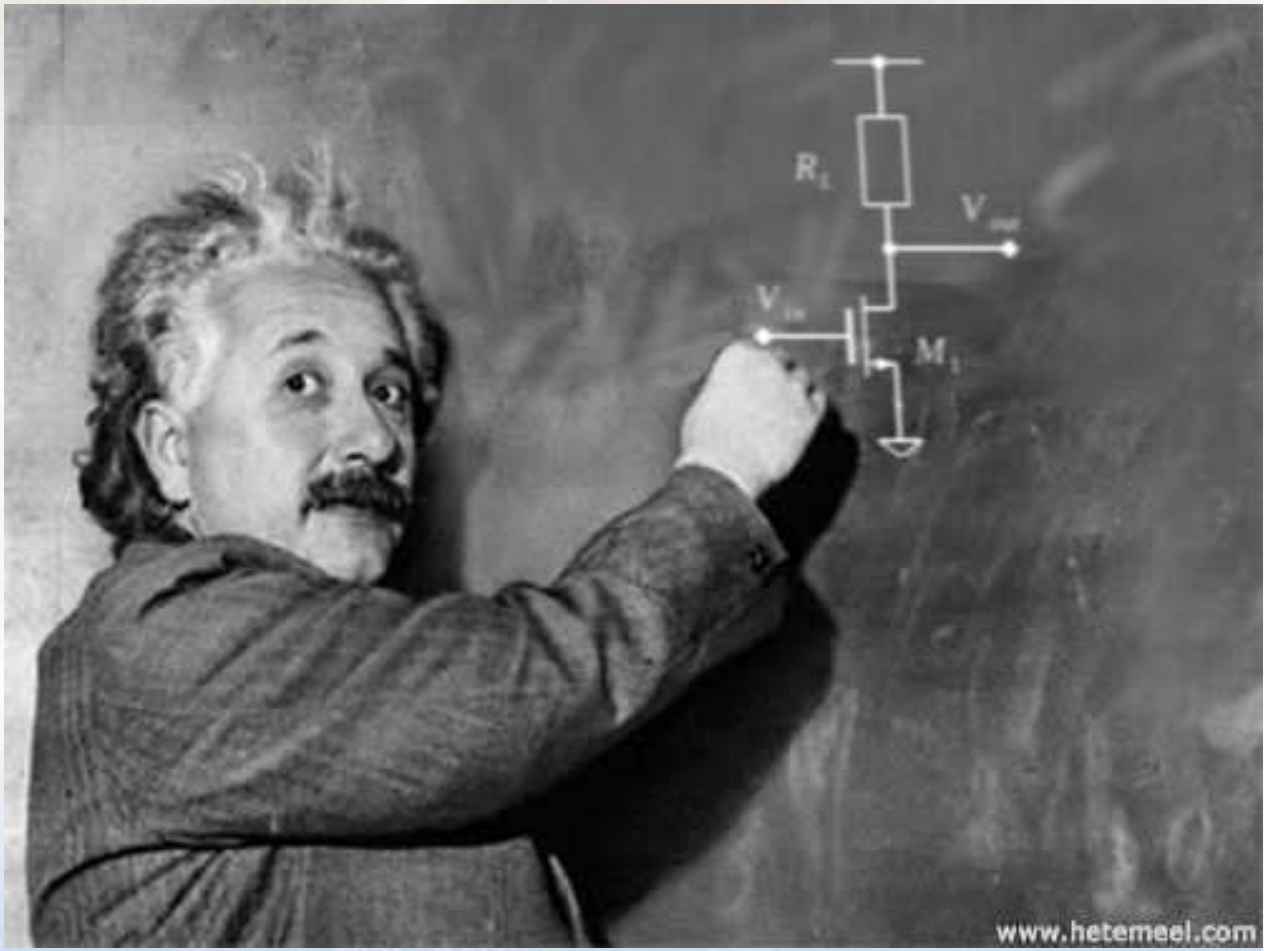
Critically damped signal at approximately 70 dB (poles become real rather than complex pair, i.e., they are well splitted)

Stability, cont'd

Bode plot

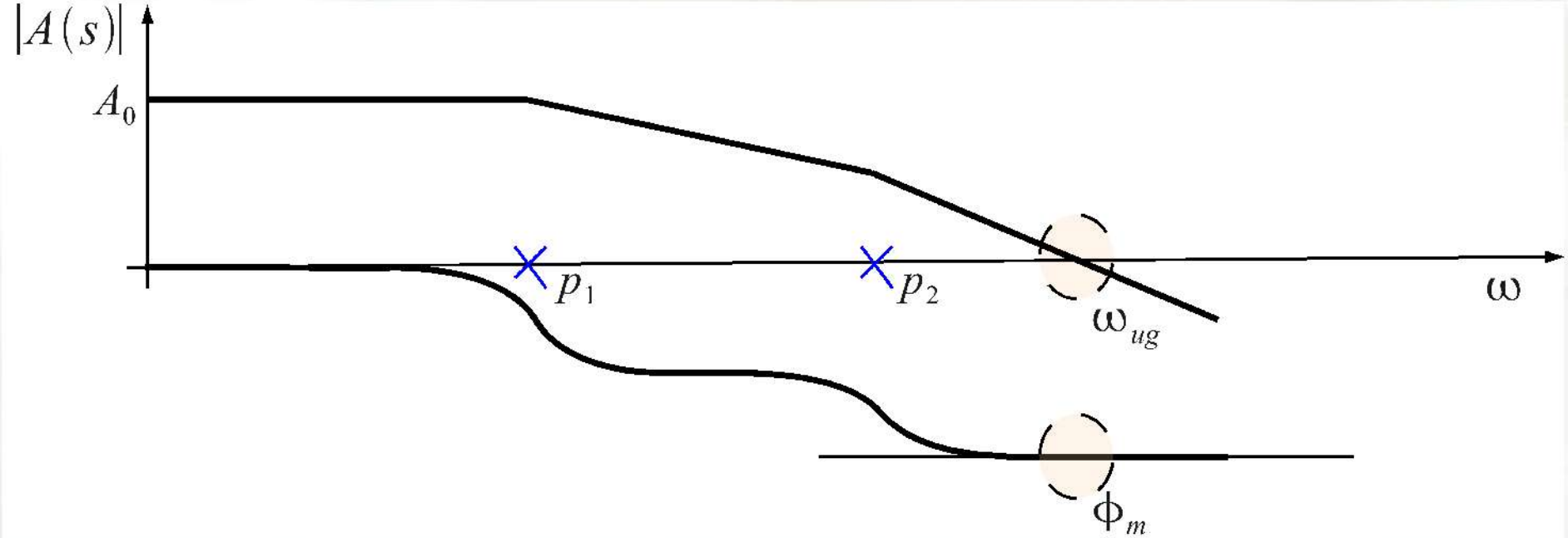
What happens to the transfer characteristics in feedback?

Phase margin



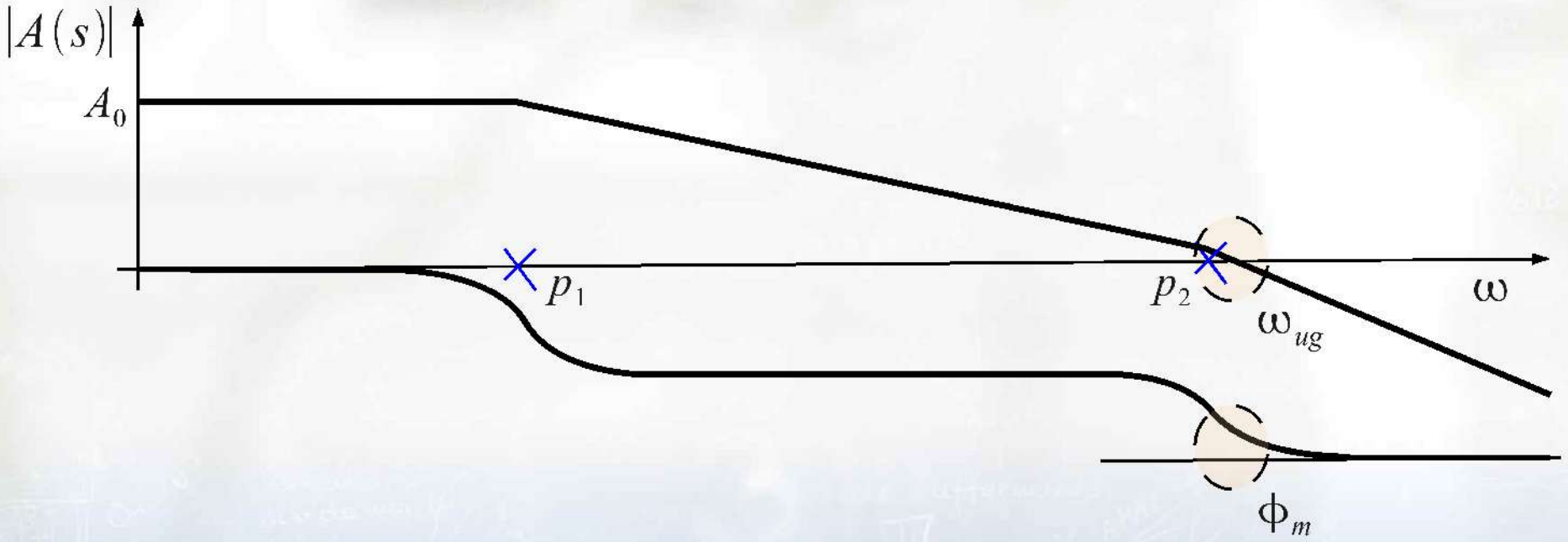
Poles and zeros revisited

Stable?

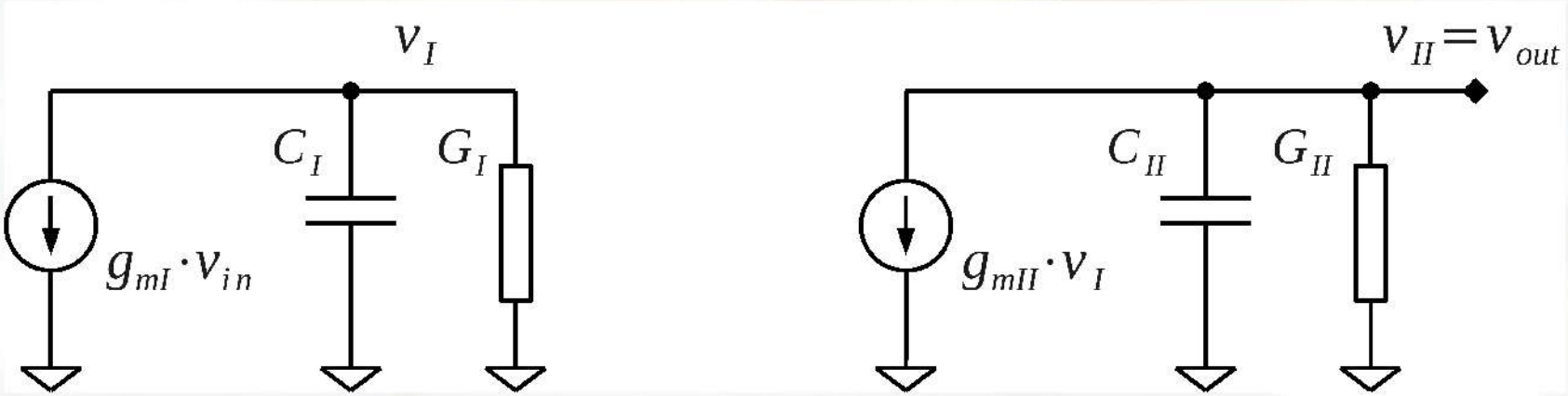


Poles and zeros revisited

Stable?



The models of a two-pole system



$$p_1 = \frac{G_I}{C_I}, \quad p_2 = \frac{G_{II}}{C_{II}}$$

$$A_1 = \frac{g_{mI}}{G_I}, \quad A_2 = \frac{g_{mII}}{G_{II}}$$

Dominant pole assumption (output)

Assuming "pole splitting", i.e., $p_2 \gg p_1$, gives us

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)} \approx \frac{A_1 \cdot A_2}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 \cdot p_2}}$$

This implies: $\omega_{ug} \approx A_1 \cdot A_2 \cdot p_1$ and

$$\phi_m = 180 - arg\, A(j\omega_{ug}) = 180 - atan\frac{\omega_{ug}}{p_1} - atan\frac{\omega_{ug}}{p_2} \approx 90 - atan\frac{\omega_{ug}}{p_2}$$

The formulas (dominant load!)

Unity-gain frequency

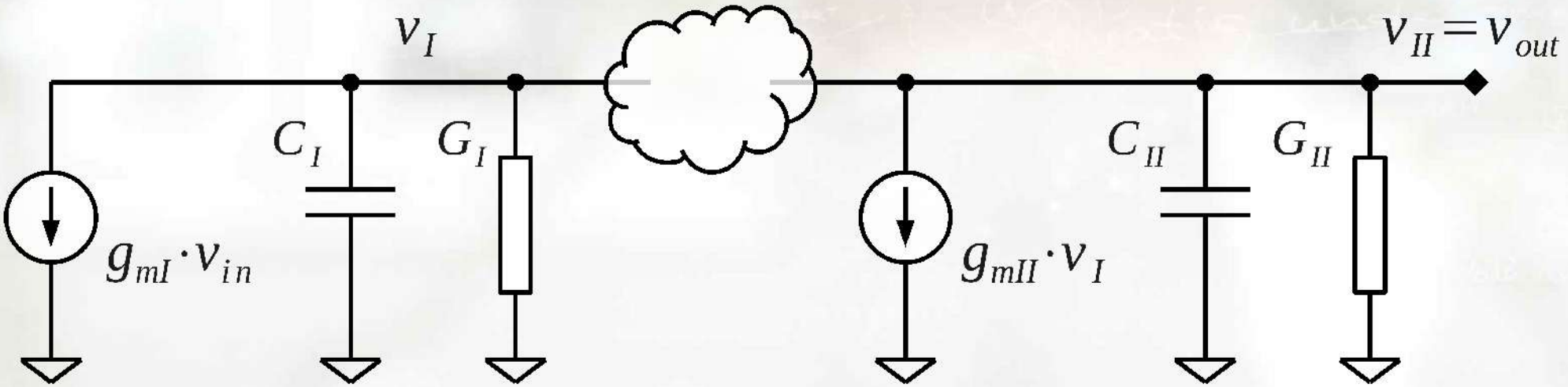
$$\omega_{ug} \approx \frac{g_{mI} \cdot g_{mII}}{G_I \cdot G_{II}} \cdot \frac{G_{II}}{C_{II}} = \frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}$$

Phase margin

$$\phi_m \approx 90 - atan\frac{\omega_{ug}}{p_2} = 90 - atan\frac{\frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}}{\frac{G_I}{C_I}} = 90 - atan\frac{g_{mI} \cdot g_{mII} \cdot C_I}{G_I^2 \cdot C_{II}}$$

etc., etc., etc. We need to be a bit more organized...

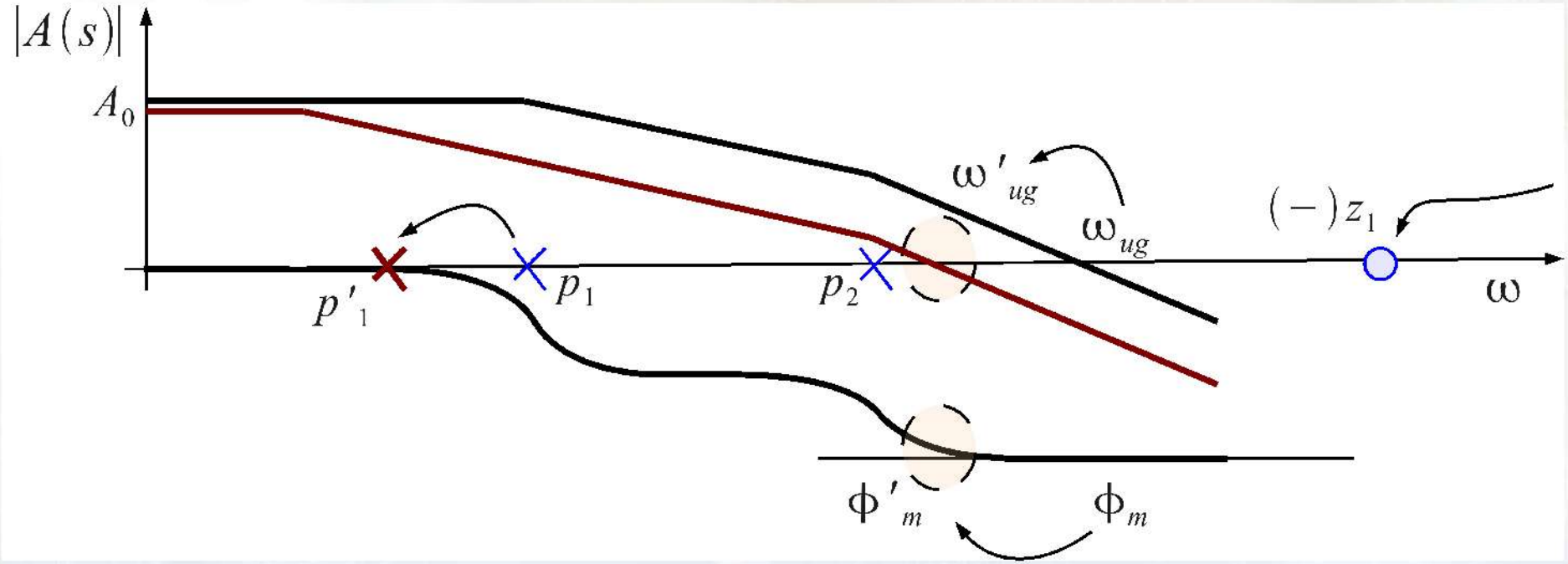
Compensation, poles are too close



The "cloud" is typically a capacitor or a series resistor-capacitor

Compensation

What is the cost associated with compensation?



Compensation, two cases:

1) "Internal" node sees a low-impedance node

Output load dominates and we drive a capacitive load (typically)

Load-compensation, i.e., increase cap externally

2) "Internal" node sees a high-impedance node

Internal load dominates, and we drive a resistive load (typically)

Miller-compensation, i.e., utilize the second-stage gain to multiply C_C

As always, some exceptions to the rule:

We could add common-drain at output

Nested compensation, active compensation, ... and more ...

Compensation, Miller capacitance

Introduced zero	Parasitic pole	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C}$	$p_2 = \frac{-g_{mII}}{C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

Introduced zero	Parasitic pole	Phase margin
$z_1 \approx 10 \cdot \omega_{ug}$	$p_2 \approx 2.2 \cdot \omega_{ug}$	≈ 60

Dominant pole moves "down", parasitic pole moves "up"

Parasitic zero added (harmful for phase margin)

Compensation, Nulling resistor 1

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}} \cdot \left(1 + \frac{C_{II}}{C_C}\right)$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow p_2$	$p_3 \approx 1.73 \cdot \omega_{ug}$	≈ 60

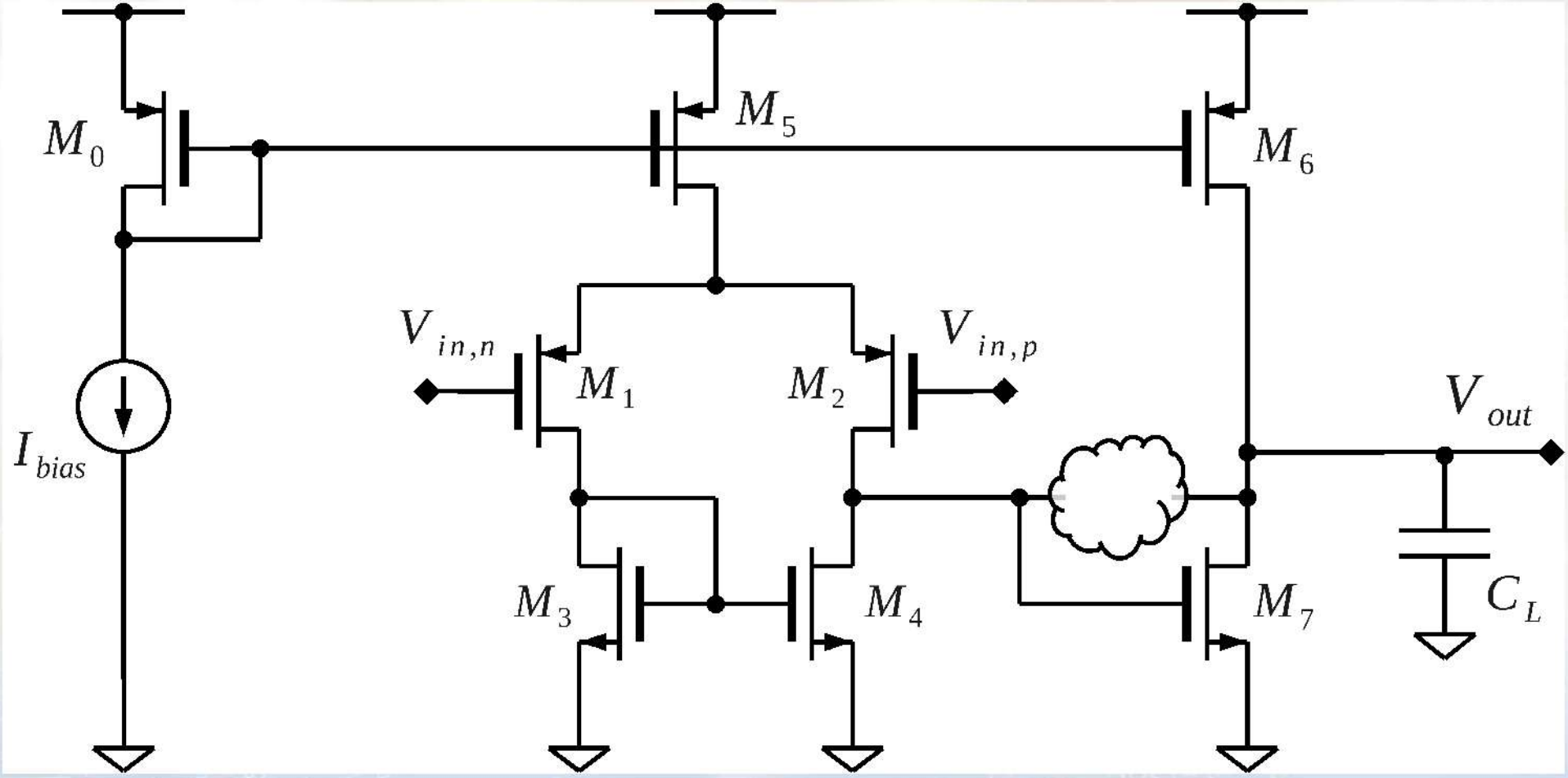
Compensation, Nulling resistor 2

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

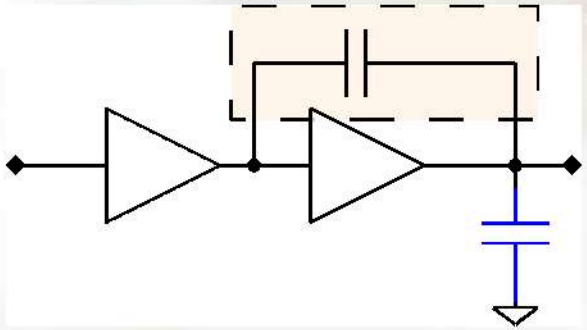
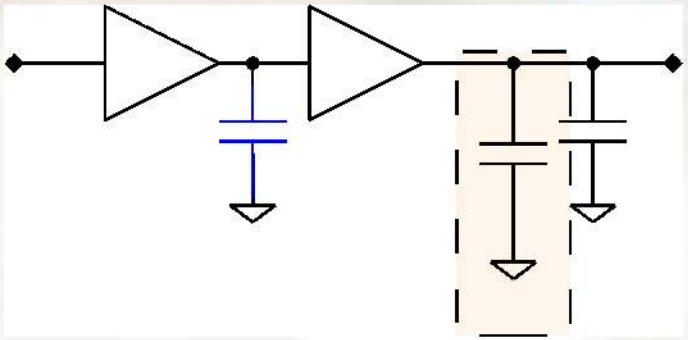
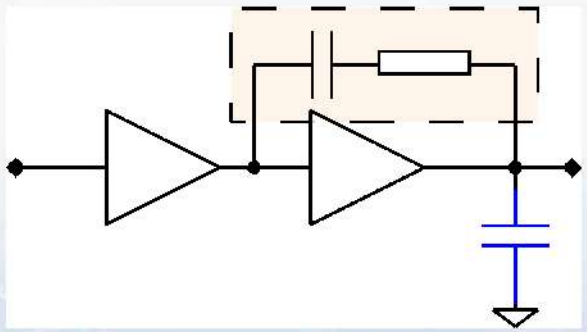
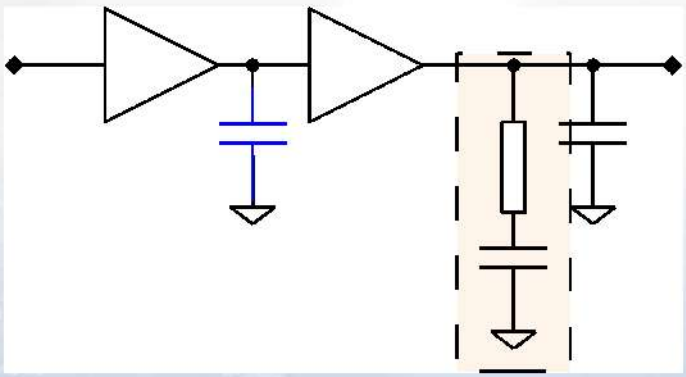
$$R_Z = \frac{1}{g_{mII}}$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \to \infty$	$p_2 \approx 1.73 \cdot \omega_{ug}$, $p_3 > 10 \cdot \omega_{ug}$	≈ 60

Operational amplifer



Compensation compiled:

	Miller	Load compensation
Cap		
Cap + Res		

Rule-of-thumbs for hand-calculation

Use e.g. MATLAB to support calculations for better understanding

See for example

```
/site/edu/es/TSTE08/antikLab/m/antikPoleZero.m
/site/edu/es/TSTE08/antikLab/m/antikSettling.m
```

In the end, use the simulator.

Must be robust over circuit variations, e.g., temperature

Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

See example exercises

What did we do today?

Wrapping up the simple amplifier stages and current mirrors

Suggesting cascodes to increase gain

Multiple poles

Stability and stability analysis

Compensation

What will we do next time?

Differential circuits

Why differential?

Operational amplifiers

More on how we design them

Circuit noise

Handles