1 Switched-capacitor circuits

1.1 Background

Since around mid 70's, it has been possible to implement complete, single-chip integrated switched-capacitor (SC) filters. This has increased the interest for such a discrete-time filter and in most discrete-time implementations today you will find some kind of switched-capacitor filter or at least some SC building blocks, such as sample-and-hold and/or accumulators (integrators).

In SC circuits, we require three components; switches, capacitors, and operational amplifiers. Normally these three components can all be implemented in a fairly standard CMOS[1] process. In fact, due to the CMOS process, we are able to create operational amplifiers (opamps) without input leakage currents. This is very important in an SC circuit. The accuracy and quality of the SC circuits will mostly depend on the quality of the capacitors in the given process. Therefore, we might sometimes require special layers, e.g., additional poly-silicon layers, to create linear[2] capacitors. There are switched techniques, such as the switched-current (SI) or switched-voltage (SV) techniques, where we do not have to rely on linear capacitors. These technique suffer from other limitations though.

The main advantage with SC circuits are that the operation of the circuits is normally determined by capacitor *ratios*, unlike for example active-RC filters where the operation is determined by the relation between a resistance and a capacitance. Hence, we can implement our circuit to be less sensitive to mismatch errors. Thereby the SC circuit is mostly very linear and that is why it has become so "popular".

The main disadvantages with SC circuits are that you normally need linear capacitors and good matching between them and you need operational amplifiers. Good matching between the capacitors implies a large chip area. The use of operational amplifiers normally implies a lower limit on the supply voltage required.

1.2 Basics of a sampled circuit

Using SC circuits implies sampling of voltages or charges. Due to the switching operation, the voltages throughout the circuit are sampled *and held*. This implies that the voltages (in the ideal case) are piecewise constant – in the real case they are normally dependent on a settling behavior, etc. Anyway, the voltages in the circuit will be given by expressions similar to

$$v(t) = \sum_{n=0}^{\infty} v(n) \cdot p(t - nT), \tag{1.1}$$

where $v(n)$ is the voltage level, T is the update or sample period, and $p(t)$ is the pulse function as

1. CMOS: Complementerary Metal Oxide Semiconductor.
2. Linear capacitors imply that the capacitance does not change with the voltage applied across the capacitor.

$$p(t) = \begin{cases} 1 & 0 \le t < T \\ 0 & t \ge T \end{cases}, \tag{1.2}$$

which states the piecewise constant voltage. From (1.1) and (1.2) we deduce that $v(n)$ is the information – the signal – and $p(t)$ is the signal carrier.

If we consider the frequency domain, we see that the spectrum becomes

$$\begin{aligned} V(\omega) &= \int_{-\infty}^{\infty} v(t) \cdot e^{-j\omega t} dt = \int_{-\infty}^{\infty} \sum_{n=0}^{\infty} v(n) \cdot p(t - nT) \cdot e^{-j\omega t} dt = \\ &= \sum_{n=0}^{\infty} v(n) \cdot \int_{-\infty}^{\infty} p(t - nT) \cdot e^{-j\omega t} dt = \\ &= \sum_{n=0}^{\infty} v(n) \cdot e^{-j\omega nT} \cdot \int_{-\infty}^{\infty} p(t - nT) \cdot e^{-j\omega(t-nT)} dt = V(e^{j\omega T}) \cdot \mathrm{sinc}(\omega), \end{aligned} \tag{1.3}$$

where $\omega = 2\pi f$. We see that the output spectrum $V(e^{j\omega T})$ is weighted by the sinc function, $\sin(\pi f)/\pi f$. We also know that the spectra of a discrete-time signal repeats it self at multiples of the sample frequency throughout the frequency domain. In Fig. 1 we find an example of how the spectrum of a piecewise constant signal is weighted in an SC circuit.

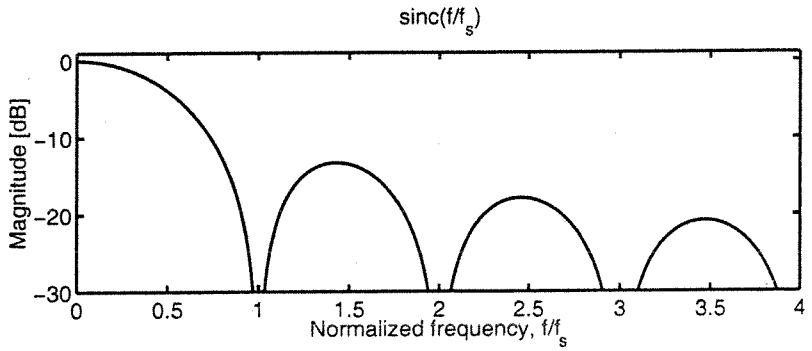


Figure 1: Principle of the weighting of the spectra in a switched-capacitor circuit.

From the discussion above, we understand two *important properties* of SC circuits:

- The output spectrum is weighted and therefore, we cannot use an update period that is in the same order of magnitude as the signal bandwidth without getting a distorted waveform.

- The output spectrum repeats it self and therefore we need to design an analog, continuous-time low pass filter that removes the higher frequency components. Together with the sample theorem, this implies that we require a sample frequency that is higher than the signal bandwidth in order to increase the passband width of the filter.

Actually, a single filter can be designed to tackle both properties above, but then we suffer from the fact that as soon as we introduce an analog filter, we introduce the same complexity we wanted to avoid by using the linear SC technique. However, if we use a sample frequency much higher than the signal bandwidth we will reduce the sinc distortion and

we will separate the repetivive signal bands to eventually be able to implement the low pass filter by passive components. It should also be noted that some of the anti-sinc weighting can be done in the SC circuit itself, by carefully tuning the transfer function to amplify at higher frequencies.

1.3 Our first switched capacitor

To better understand the operation of SC circuits we normally consider the charge on the capacitors and how it is transferred through the circuit when opening and closing the switches.

For a capacitor of capacitance C we have that the charge can be written as the product of the voltage across the plates and the capacitance, i.e.,

$$q(t) = C \cdot v(t). \tag{1.4}$$

The larger capacitance, C, the more charge, q, can be stored for a fixed voltage, v. An ideal capacitance does (obviously) not have any resistive components and hence the charge (holes or electrons) will instantaneously be transported to the plates of the capacitor as soon as the voltage is applied across the plates. In the time domain, this can be described by a Dirac impulse. In reality we will have some resistance in wires, cables, contacts, etc., smoothening the impulse.

An unconnected capacitor will conserve the charge on its plates, since there is no DC path to ground (or common voltage source) from both plates through which the charge can be transported. Again, this is of course only true to a certain extent, since we always have secondary paths between the plates. Anyway, the key point with this statement is that by using this property in an SC circuit we can create small "memory" cells, i.e., delay elements or z^{-1} in the z-domain. These are used to create discrete-time systems with different transfer functions.

Now, consider the single capacitor shown in Fig. 2 (a) for two different settings of the switch. We have indicated the positive and negative plates on the capacitor. This notation will help us throughout the work later when we analyze more complex circuits. The negative plate is grounded and the positive plate can be connected to either one of two nodes V_1 and V_2 through the switch S_1. We let S_1 connect the positive plate and V_1 during the time period from kT to $kT + T/2$. This will be referred to as the *first phase* (ϕ_1) of operation. During the time period $kT + T/2$ to $kT + T$ the plate is connected to V_2 instead. Logically, we refer to this as the *second phase* (ϕ_2) of operation. It is however common to use even more phases in an SC circuit. To simplify notation, we will throughout the text use $\tau = T/2$ as well.

We analyze the circuit by investigating the charge during the two phases. We have illustrated how the redistribution of charge in Fig. 2 (b). So, during ϕ_1 the charge on the capacitor will be

$$q(\phi_1) = C \cdot V_1 \tag{1.5}$$

and during ϕ_2 the charge will be

$$q(\phi_2) = C \cdot V_2. \tag{1.6}$$

Thereby we see that if $V_1 \neq V_2$ we will have a change in the charge on the plates – a certain amount of charge must have been transported from V_1 to V_2. This charge difference can be written as

$$\Delta q = q(\phi_2) - q(\phi_1) = C \cdot [V_2 - V_1]. \tag{1.7}$$

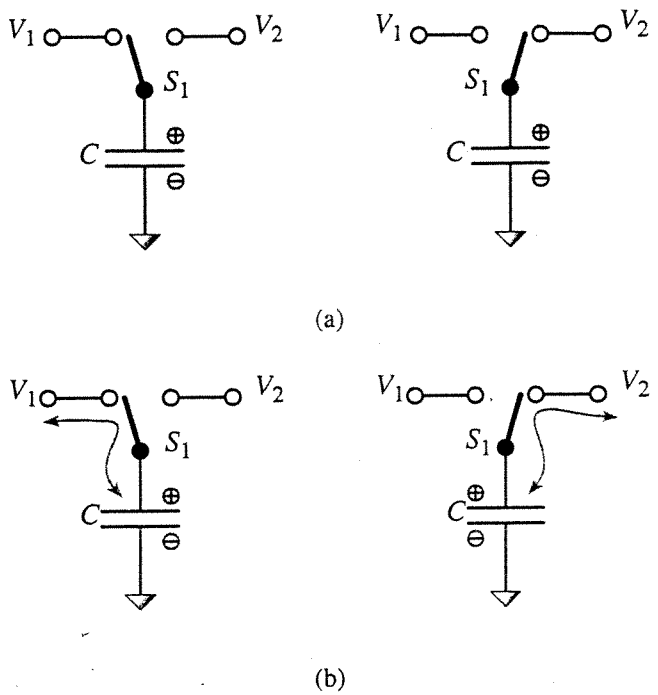


Figure 2: A switched capacitor with switch connecting the positive plate to either V1 or V2.

This charge "package" is transported during one sample period and hence the average current, $\bar{I}$, can be written as

$$\bar{I} = \frac{\Delta q}{\Delta t} = \frac{q(\phi_2) - q(\phi_1)}{T} = \frac{C}{T} \cdot (V_2 - V_1). \tag{1.8}$$

Here we see that the average current can be written as a factor C/T times a voltage, $V_2 - V_1$. This is virtually Ohm's law for a resistor, where the conductance corresponds to $G = C/T$, i.e., $R = T/C$. We conclude that a switched capacitor *behaves as a resistance*. This is the essential part of the swiched-capacitor technique and we have sketched the principle in Fig. 3.

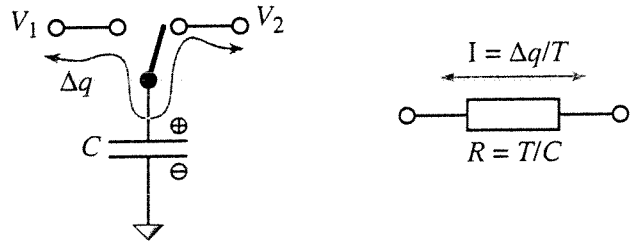


Figure 3: A switched capacitor simulates the behavior of a resistance.

We require however the sample period T to be rather small to guarantee a good analogy between the two cases. The choice of T is related to the bandwidth of the system and the "accuracy" of the integration. This is covered more closely in Sec. 1.8, where we discuss different ways to map the transfer function from the continuous-time to the discrete-time domain. So, if we want to be "sloppy" we can say that we can realize the operation of an active-RC filter by replacing all the resistors by switched capacitors. This will however require a too high oversampling ratio and there are better, alternative SC circuits that perform a similar operation. It is a good tool for understanding the operation of the circuit

though. As another tool we develop a strategy for determining the operation of SC circuits by investigating how the charge is transported throughout the circuit. First, we must understand how an opamp can help us improve the circuits.

1.4 Using operational amplifiers in SC circuits

Previously, we have considered the passive components (well, apart from the switch which is kind of active). Now we include the operational amplifier (opamp) which is used to increase the driving capability and for some other purposes.

One of the most important features is that we can reproduce a voltage and distribute it to several different sources without affecting the voltage source. Here the source can be the voltage across a capacitor, which obviously is sensitive towards loss of charge on its plates. Another feature is that we can provide the circuit with virtual grounds. With a virtual ground, we understand a node that has no AC content, hence it is perfectly constant, but it is at the same time not connected to the common ground. This is useful for the charge conservation as well.

Consider the circuit in Fig. 4. This is an operational amplifier in a buffer configuration. The output voltage is equal to the voltage applied to the positive input. In this case this is given by the voltage across the capacitor. (We assume that the capacitor has been charged during another phase of operation). Using this configuration yields an output voltage with great driving capability, hence its output can be distributed to several different sinks. At the same time the input voltage is separated from all those sinks. Hence, we can have a weak, sensitive source that is isolated through the amplifier. Now, this is exactly what we are looking for in our case — we have the voltage across a capacitor which is very sensitive to any loss in charge which we at the same time want to use to distribute to other capacitors.

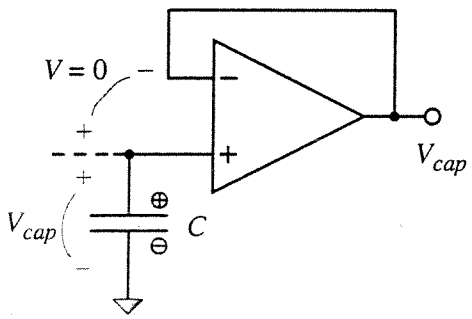


Figure 4: Opamp in a buffer configuration reproducing the voltage across a capacitor.

Consider the circuit in Fig. 5 where we have an ideal opamp with its positive input is connected to a constant (DC) voltage source, V_{DC}. Since the gain of the amplifier is infinitely high, the voltage difference between the negative and positive inputs must be zero. Hence, the voltage at the negative input is V_{DC} as well (virtual ground). The negative input of the opamp is connected to a capacitor in series with a resistor down to ground. (The resistor is simply a model of a switch and its resistance may very well be set to 0 Ohms in this example.) Although the resistor connects one of the plates to ground it will not drain the charge stored in the capacitor, since no charge can disappear from the opamp's negative input[1]. Thereby, we have V_{DC} over the capacitor and 0 V over the resistor. (Once again, we assume that the charge on the capacitor has been transported there during another phase of operation.

1. Assuming that the input stage to the opamp consists of MOS transistors.

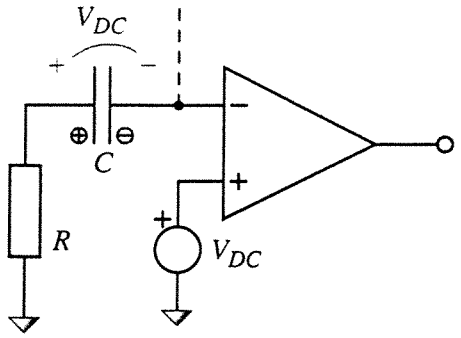


Figure 5: Opamp in a buffer configuration creating a virtual ground.

In Fig. 6 we find our first simple switched-capacitor accumulator (SCA) or sometimes also crudely referred to as an integrator. Normally, though, we associate an integrator with a continuous-time operation and accumulator with discrete-time behavior. The principle is the same as the active-RC integrator, but we have now replaced the series resistor with the switched shunt capacitor as described in Sec. 1.3. The switches indicate the phase of operation.

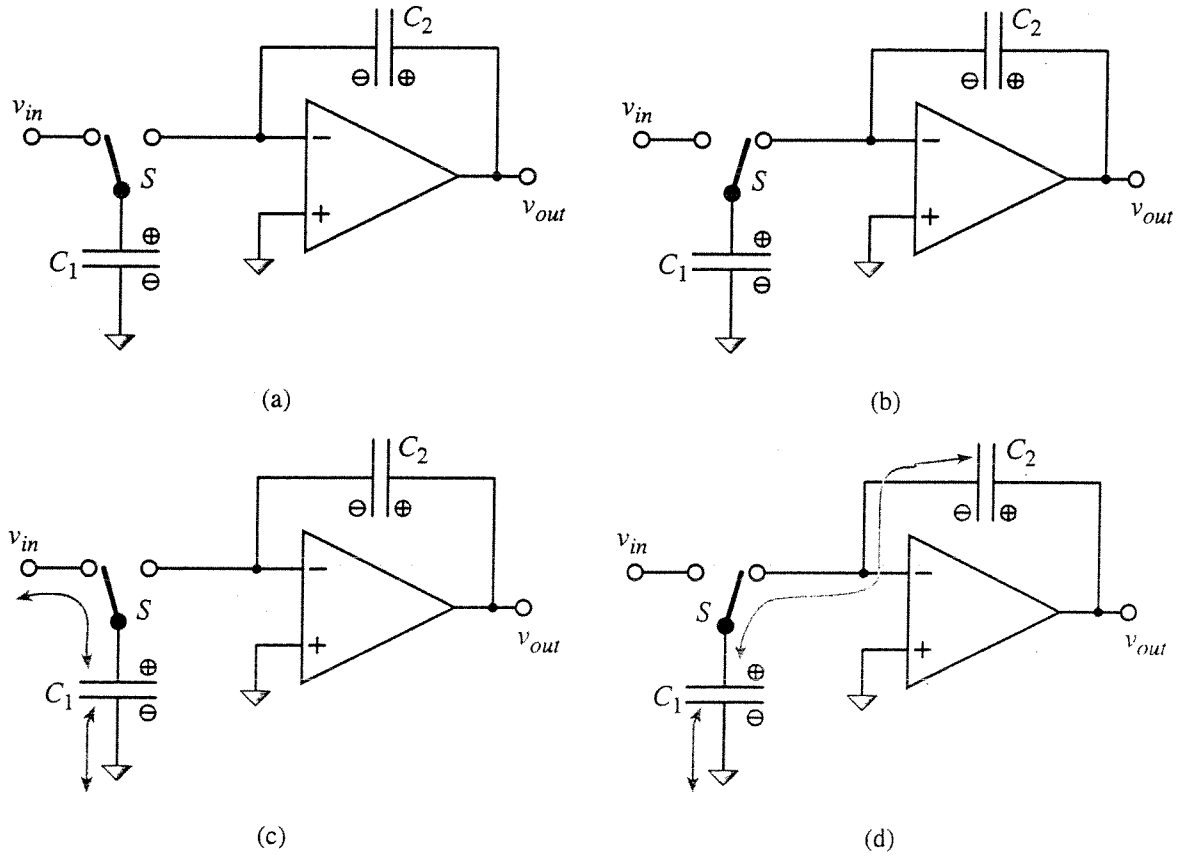


Figure 6: Example of a switched capacitor accumulator during (a) first and (b) second phase. In (c) and (d) the charge transportation is illustrated.

During the first phase (ϕ_1) – Fig. 6 (c) – we see that C_1 is charged by the input voltage and hence the charge on the positive plate of this capacitor will be given by

$$q_1(kT) = C_1 \cdot [v_{in}(kT) - 0] = C_1 \cdot v_{in}(kT). \tag{1.9}$$

The negative plate will get its charge from the ground, providing with equal amount of negative charge for equilibrium. Here we will also use the assumption that the input voltage is the output from another SC circuit (or similar) and thereby it will be piecewise constant over a whole sample period. This implies that

$$v_{in}(kT) = v_{in}(kT - \tau) \tag{1.10}$$

as well. The negative opamp input is disconnected from C_1 and since we have CMOS opamps, no charge can disappear from this node. There is no DC path to ground, since the feedback capacitor blocks any DC current. Thereby the charge on this capacitor will be determined by the charge on the plate during the previous period:

$$q_2(kT) = q_2(kT - \tau). \tag{1.11}$$

Since the positive input is connected to ground and the gain of the amplifier is infinite the voltage on the negative input will be 0 as well. Thereby, we have that

$$q_2(kT) = C_2 \cdot [v_{out}(kT) - 0] = C_2 \cdot v_{out}(kT). \tag{1.12}$$

Combining (1.11) and (1.12) gives us the memory function on the output:

$$C_2 \cdot [v_{out}(kT) - 0] = C_2 \cdot [v_{out}(kT - \tau) - 0] \Rightarrow v_{out}(kT) = v_{out}(kT - \tau). \tag{1.13}$$

During the second phase (ϕ_2) – see Fig. 6 (d) – we disconnect the input voltage and we connect C_1 to the negative opamp input. Now something must happen; we have increased the amount of capacitance (and charge) to the negative opamp input but the voltage in this node must be kept constant at 0 V due to the infinite gain of the opamp. We see that the voltage across C_1 must be 0 V as well since it is connected between ground and virtual ground. Capacitor C_1 must loose all of its charge. Since its positive plate is connected to virtual ground and the charge will not just "disappear" – it will flow to the negative plate of C_2, since no charge can go into the opamp. The opamp output can be considered as an ideal voltage source and it will provide the postive plate of C_2 with enough charge to compensate for the change of charge.

We have that the charge on C_1 has disappeared

$$q_1(kT + \tau) = C_1 \cdot [0 - 0] = 0 \tag{1.14}$$

and the charge on C_2 must be given by its "old" charge plus the "new" charge from C_1 as

$$-q_2(kT + \tau) = -q_2(kT) + q_1(kT). \tag{1.15}$$

Notice now how we have used the references on the capacitor plates. The charge q_1 was stored on the postitive plate of C_1 and was transported to the negative plate of C_2. The charge on C_2 can also be written as

$$q_2(kT + \tau) = C_2 \cdot [v_{out}(kT + \tau) - 0] = C_2 \cdot v_{out}(kT + \tau). \tag{1.16}$$

Using the expressions from (1.9) through (1.14), and (1.16) in (1.15) gives us the transfer function as

$$\begin{aligned} C_2 \cdot v_{out}(kT + \tau) &= C_2 \cdot v_{out}(kT) - C_1 \cdot v_{in}(kT) = \\ &= C_2 \cdot v_{out}(kT - \tau) - C_1 \cdot v_{in}(kT) = C_2 \cdot v_{out}(kT - \tau) - C_1 \cdot v_{in}(kT - \tau). \end{aligned} \tag{1.17}$$

This can be written as

$$v_{out}(kT+\tau) = v_{out}(kT-\tau) - \frac{C_1}{C_2} \cdot v_{in}(kT-\tau), \tag{1.18}$$

where we clearly can identify the accumulation of the output voltage. Using the z transform gives us

$$z^{1/2} \cdot V_{out}(z) = z^{-1/2} \cdot V_{out}(z) - \frac{C_1}{C_2} \cdot z^{-1/2} \cdot V_{in}(z) \tag{1.19}$$

and the transfer function

$$A(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}, \tag{1.20}$$

which is the well-known expression for a discrete-time accumulator (integrator). The gain of the accumulator is given by the capacitor ratio C_1/C_2. If we would have the continuous-time case, the transfer function would be

$$A(s) = \frac{-1}{sC_2R_1} = \frac{-1}{sC_2} \cdot \frac{C_1}{T} = -\frac{C_1}{C_2} \cdot \frac{1}{sT}. \tag{1.21}$$

1.5 Some tips and tricks for charge distribution analysis

Here we have compiled some of the properties from the SC circuit with opamp in order to create a useful tool or strategy for analysing the operation of SC circuits:

- No charge can disappear from unconnected/disconnected capacitor plates
- The absolute charge on the positive plate is equal to the absolute charge on the negative plate
- A capacitor with same potential on both plates will have an effective zero voltage across its plates and thereby looses all of its charge
- We use opamps with MOS transistor inputs and thereby, no current can flow into the opamp inputs
- The output of the ideal opamp operates as an ideal voltage source and can provide infinite amount of charge
- The circuit will strive for equilibrium and the charge will redistribute to reach that state within the sample period
- Due to the charge conservation at for example the opamp input node (virtual ground) the total amount of charge on the plates connected to that node must be constant held constant

During the analyses of the SC circuits, we investigate three consecutive phases[1]. This enables us to derive a transfer function over a whole sample period.

1. Here we assume an SC circuit with only two phases. In general, we mostly need to investigate $3n/2$ phases, where n is the number of phases.

In SC circuit the clock phases are normally nonoverlapping which means that we have a short period of time where all switches are open. If the clock phases are overlapping, we will destroy the transfer function due to unwanted charge sharing.

1.6 More SC building blocks

Above, we considered the basics of SC circuits and how they operate in general. As an example we illustrated an SC accumulator which mimiced the active-RC integrator by replacing the resistor with a switched capacitor. We will now take a closer look on some other building blocks, such as the sample-and-hold (S/H) and the gain circuit. We will also outline why the accumulator described in Sec. 1.4 is not very good to use in a real implementation. Its limitation is due to the influence of parasitic components in the capacitors and switches.

1.6.1 Influence of parasitics in SC accumulators

Capacitors implemented on-chip, i.e., plate-capacitors laid out on the silicon surface (the substrate), suffer from the drawback that there will also be a large capacitance between the bottom plate and the actual substrate. Normally, the substrate is grounded and therefore there will be a parasitic capacitance between the bottom plate and ground. Unfortunately, there will also be a parasitic component associated with the top plate due to the edge of the plate and connection wires increasing the capacitance to the substrate. This parastic is usually not as large as the bottom-plate parasitic, but it is not neglegible. We have illustrated the effect in Fig. 7, where the bottom plate has been indicated separately. Notice that the parasitics couple to *ground* (or whatever the substrate is connected to) and not to any of the voltages connected to the plates.

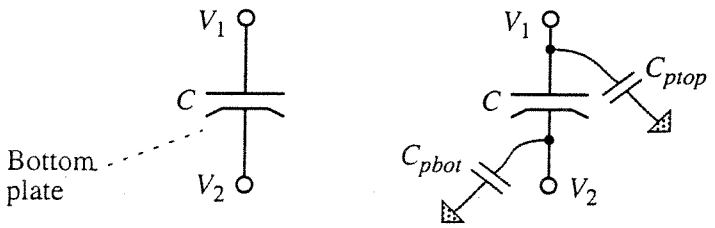


Figure 7: Parasitic capacitance associated with the top and bottom plate.

Normally, the parasitic components may be large compared to the nominal capacitance, well in the order of tens of per cent of the actual capacitance. This ratio is very approximate and it may vary a lot for different capacitors over the chip. Therefore, we must be very careful when designing our circuit. We must use or implement SC blocks that are designed so that these parasitic components do not influence the actual transfer function. They will inevitably influence the speed of the circuit, but we can mostly design our switches and opamps to compensate for this additional capacitance. We also conclude that we should be very careful to which nodes we connect the ground plates. They should *never be connected to the sensitive nodes*, such as the input node of the opamp.

We will highlight the concept of parasitic capacitance with two examples of SC accumulators circuits as shown in Fig. 8 (a) and (b). We recognize the left SCA from Fig. 6, but we have modified it slightly by adding a second input, V_2. The acumulator in Fig. 8 (b) does only have one input. The two circuits are rather similar, but we shall later see what differs the two from each other.

The accumulator is one of the most important building blocks in discrete-time filters. As we also found in (1.20) the accumulator output should be given by the sum of the previous output value and the input value as

$$V_{out}(kT+T) = V_{out}(kT) - V_{in}(kT). \tag{1.22}$$

In the z-domain this can be expressed as

$$z \cdot V_{out}(z) = V_{out}(z) - V_{in}(z), \tag{1.23}$$

and we get the transfer function

$$A(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-1}{z-1} = -\frac{z^{-1}}{1-z^{-1}}. \tag{1.24}$$

Consider (1.23) – as mentioned previously, we achieve the transfer function by summing the stored output value and the stored input value. Hence, we need two capacitors to store the values separately.

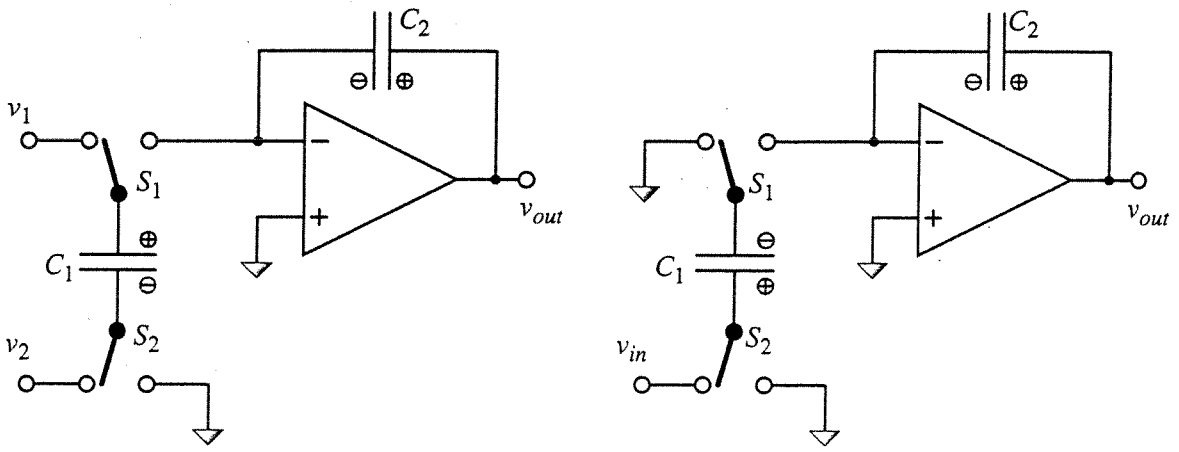


Figure 8: Two SC accumulators circuits.

We investigate the parasitics by adding the additional capacitance down to ground from each plate of all capacitors and both ends of switches down to ground. Consider the modified accumulators from Fig. 8 shown in Fig. 9, where we have added most of the parasitics.

First we start with the gain circuit shown in Fig. 9 (a). We identify the two main capacitors C_1 and C_2. We also find the C_{p1}, C_{p2}, C_{p3} and C_{p4} to be connected in parallel with the input or output voltage. These are nodes fed by an operational amplifier and hence will not influence the result, since the voltage applied to that node is independent of the capacitance. C_{p5}, C_{p6}, C_{p7} and C_{p8} are shorted between ground (or virtual ground) and ground, hence they will never influence the result, since they are always empty of charge. The parasitics remaining are C_{p9} and C_{p10}.

During phase ϕ_1 we charge capacitor C_1 with the two input voltages v_1 and v_2. The negative input of the opamp is disconnected. Hence, we get

$$q_1(kT) = C_1 \cdot [v_1(kT) - v_2(kT)], \tag{1.25}$$

but we also see that we charge C_{p9} by the input voltage v_1 and C_{p10} by the input voltage v_2, hence

$$q_{p9}(kT) = C_{p9} \cdot v_1(kT) \text{ and } q_{p10}(kT) = C_{p10} \cdot v_2(kT). \tag{1.26}$$

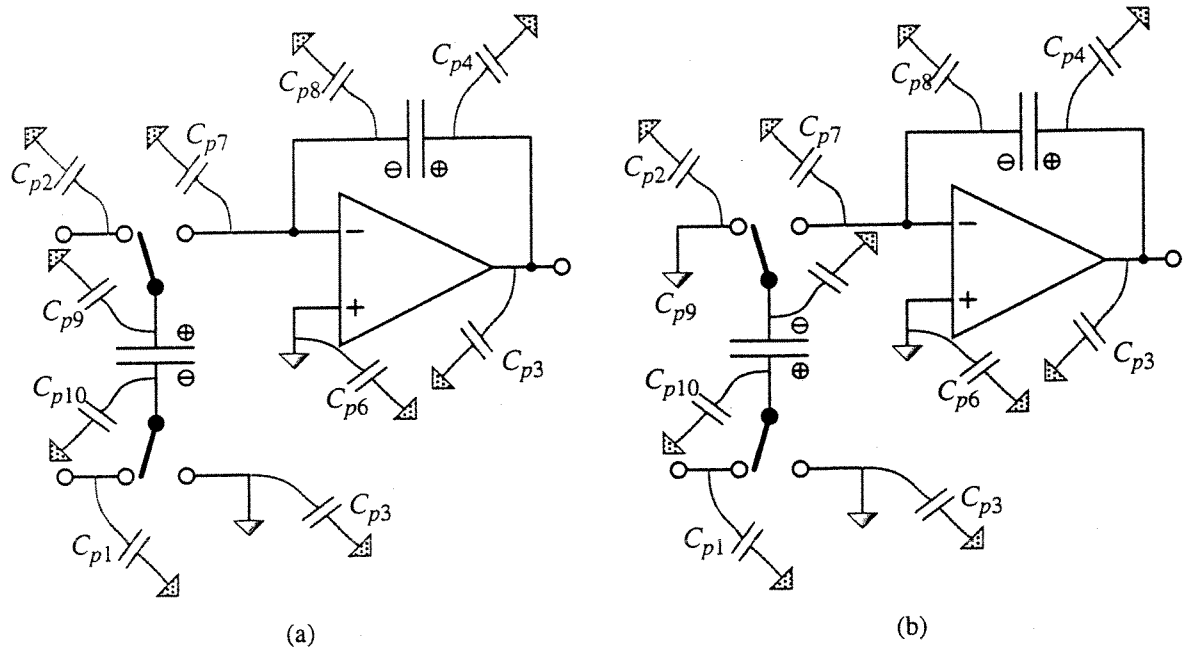


Figure 9: Two SC accumulators circuits with indicated parasitic components.

The charge on the feedback capacitance is

$$q_2(kT) = C_2 \cdot [v_{out}(kT) - 0] = C_2 \cdot v_{out}(kT). \tag{1.27}$$

Since the charge cannot disappear from the plates of C_2, we see that the charge must equal that from the previous clock phase. We have

$$q_2(kT) = q_2(kT - \tau) = C_2 \cdot v_{out}(kT - \tau), \tag{1.28}$$

hence

$$v_{out}(kT) = v_{out}(kT - \tau). \tag{1.29}$$

During the next phase (ϕ_2), we have the switches changed to their other position. Now, we see that C_{p10} is shorted and hence all the charge will cancel and not influence the transfer function. C_{p9} will also be shorted and loose all of its charge. Here however, the charge will not "disappear" – it will flow towards the negative plate of C_2. (Once again – no charge can flow into the opamp inputs). We have that the charge on C_2 can be written as

$$q_2(kT + \tau) = C_2 \cdot [v_{out}(kT + \tau) - 0] = C_2 \cdot v_{out}(kT + \tau). \tag{1.30}$$

This charge must equal the "old" charge plus the "new" charge. Hence we get

$$q_2(kT + \tau) = q_2(kT) + q_1(kT) + q_{p9}(kT). \tag{1.31}$$

Using (1.25), (1.26), (1.28), and (1.30) in (1.31) gives us

$$C_2 \cdot v_{out}(kT + \tau) = C_2 \cdot v_{out}(kT - \tau) + (C_1 + C_{p9}) \cdot v_1(kT) - C_1 \cdot v_2(kT). \tag{1.32}$$

Assuming that the inputs are piecewise constant, hence $v_i(kT) = v_i(kT - \tau)$ gives us the z-transform as

$$\begin{aligned} &C_2 \cdot V_{out}(z) \cdot z^{1/2} = \\ &\quad = C_2 \cdot V_{out}(z) \cdot z^{-1/2} + (C_1 + C_{p9}) \cdot V_1(z) \cdot z^{-1/2} - C_1 \cdot V_2(z). \end{aligned} \tag{1.33}$$

To simplify the discussion, we will also assume that $V_2(z)$ is grounded, i.e., $V_2(z) = 0$. Notice that with this assumption we have actually recreated our SCA from Fig. 6. Therefore we get

$$C_2 \cdot V_{out}(z) = C_2 \cdot V_{out}(z) \cdot z^{-1} + (C_1 + C_{p9}) \cdot V_1(z) \cdot z^{-1}, \tag{1.34}$$

or given as a transfer function

$$A(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1 + C_{p9}}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}. \tag{1.35}$$

Here we see that the parasitic component affects the gain of the circuit – in general, it affects the transfer function of the circuit. Therefore, we call this a *parasitic sensitive* SC circuit. Luckily it does not affect the pole, which normally is an even worse problem, since we mostly can compensate for gain errors rather easily.

Now, consider the accumulator in Fig. 9 (b). We can neglect the parasitics C_{p1}, C_{p2}, C_{p3} and C_{p4}, since they are connected in parallel with the input or output voltages. C_{p5}, C_{p6}, C_{p7}, and C_{p8} are always shorted between grounds. The parasitics remaining are once again C_{p9} and C_{p10}. Actually we can directly see that C_{p9} is switched between ground and virtual ground, hence, it will never store any charge and will not influence the transfer function. The only remaining parasitic component is C_{p10}.

During the first phase (ϕ_1) we have the charge on the first capacitor as

$$q_1(kT) = C_1 \cdot [v_{in}(kT) - 0] = C_1 \cdot v_{in}(kT) \tag{1.36}$$

and the charge on the second capacitor is

$$q_2(kT) = C_2 \cdot [v_{out}(kT) - 0] = C_2 \cdot v_{out}(kT). \tag{1.37}$$

Since the charge cannot disappear from the feedback capacitor C_2 we understand that the charge must be conserved from the last phase:

$$q_2(kT) = q_2(kT - \tau) = C_2 \cdot v_{out}(kT - \tau), \tag{1.38}$$

hence

$$v_{out}(kT - \tau) = v_{out}(kT). \tag{1.39}$$

The parasitic is charged as well:

$$q_{p10}(kT) = C_{p10} \cdot [v_{in}(kT) - 0] = C_{p10} \cdot v_{in}(kT) \tag{1.40}$$

During the next phase (ϕ_2) we see that C_1 is switched and the plates will become connected between ground and virtual ground. Both plates have the same potential and hence it must loose all of its charge. The circuit strives for equilibrium and the charge will be transported from the negative plate to the negative plate of C_2. The opamp will compensate with charge to the positive plate of C_2. The charge on the positive plate of C_1 is drained in the ground. At the same time C_2 will keep its charge from the previous phase. Hence, we get

$$q_2(kT + \tau) = C_2 \cdot [v_{out}(kT + \tau) - 0] = q_2(kT) + q_1(kT). \tag{1.41}$$

Using the voltage notations, we get

$$C_2 \cdot v_{out}(kT + \tau) = C_2 \cdot v_{out}(kT) + C_1 \cdot v_{in}(kT). \tag{1.42}$$

The parasitic is switched from the input to ground. It will loose all of its charge since both plates are connected to ground. However all of that charge will get lost to the ground and will not be transported anywhere else within the circuit, hence

$$q_{p10}(kT+\tau) = C_{p10}\cdot[0-0]. \tag{1.43}$$

Using the result in (1.38) and that the input voltage is piecewise constant during the entire sample period, $v_{in}(kT) = v_{in}(kT-\tau)$ gives us

$$C_2\cdot v_{out}(kT+\tau) = C_2\cdot v_{out}(kT-\tau) + C_1\cdot v_{in}(kT-\tau). \tag{1.44}$$

Or expressed with the z-transform we get

$$C_2\cdot V_{out}(z)\cdot z^{1/2} = C_2\cdot V_{out}(z)\cdot z^{-1/2} + C_1\cdot V_{in}(z)\cdot z^{-1/2} \tag{1.45}$$

and the transfer function becomes

$$A(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2}\cdot\frac{z^{-1}}{1-z^{-1}}, \tag{1.46}$$

which is our desired transfer function. The parasitics do not affect the transfer function and therefore we call this type a *parasitic insensitive* SC circuit.

1.6.2 Sample-and-hold

Besides the accumulator the sample-and-hold (S/H) or track-and-hold (T/H) circuits are important. Technically, any SC circuit performs a sampling function, but we will discuss the S/H as a separat building blocks, since we normally add some special features to them. Here we want to sample the input signal and use the opamp to reproduce it and drive a number of different stages. Typical applications are for the ADC and also at the input to e.g. SC filters. The S/H can also be implemented to have a gain given by a capacitor ratio, similar to the cases in (1.35) and (1.46).

Consider the S/H circuit shown in Fig. 10. This circuit is also referred to as an SC gain circuit. Unlike the other SC circuits we have investigated, this does not accumulate the voltage at its output.

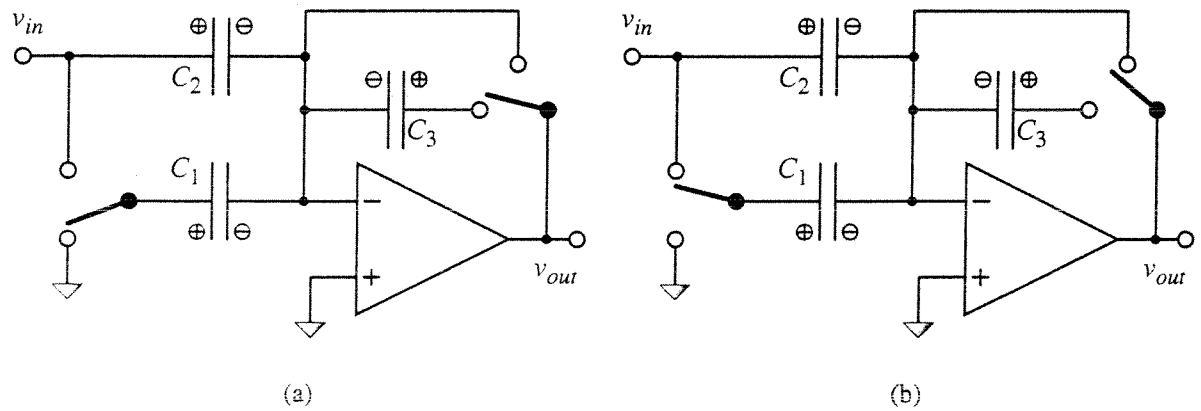


Figure 10: SC sample-and-hold during its two phases.

The drawback with this sample-and-hold circuit is that the gain of the circuit is dependent on the matching of the capacitors C_1 and C_2. This error source can be quite dominating in any high-resolution application.

We will now do a charge redistribution analysis of the circuit. During the first phase (ϕ_1) we have no charge on C_1, since it is shorted between ground and virtual ground:

$$q_1(kT) = C_1 \cdot [0-0] = 0. \tag{1.47}$$

Capacitor C_2 is charged by the input voltage and hence

$$q_2(kT) = C_2 \cdot [v_{in}(kT)-0] = C_2 \cdot v_{in}(kT). \tag{1.48}$$

The charge on C_3 is given by the output voltage:

$$q_3(kT) = C_3 \cdot [v_{out}(kT)-0] = C_3 \cdot v_{out}(kT). \tag{1.49}$$

During the next phase (ϕ_2), we add the C_1 to the input and the output is fed back to the negative input of the opamp. Hence, the output voltage is forced to 0 V. The charge on C_1 becomes

$$q_1(kT+\tau) = C_1 \cdot [v_{in}(kT+\tau)-0] = C_1 \cdot v_{in}(kT+\tau). \tag{1.50}$$

The charge on C_2 is given by

$$q_2(kT+\tau) = C_2 \cdot [v_{in}(kT+\tau)-0] = C_2 \cdot v_{in}(kT+\tau). \tag{1.51}$$

We see that the positive plate of C_3 is left disconnected. This implies that the charge on C_3 is maintained from the previous phase, since no charge can disappear from an unconnected plate:

$$q_3(kT+\tau) = q_3(kT) = C_3 \cdot v_{out}(kT). \tag{1.52}$$

Notice that this equation does not say anything about the output voltage during this phase. We now consider the charge conservation. From phase 1 to phase 2 the only charge that is conserved is the charge on C_3 (!). The charges on C_1 and C_2 are completely determined by the voltage applied at the input for this time period. Therefore, we have to investigate what happens when we switch from phase 2 to phase 1. Again we have – see equations (1.47) through (1.49):

$$q_1(kT+T) = C_1 \cdot [0-0] = 0, \tag{1.53}$$

$$q_2(kT+T) = C_2 \cdot [v_{in}(kT+T)-0] = C_2 \cdot v_{in}(kT+T) \tag{1.54}$$

and

$$q_3(kT+T) = C_3 \cdot [v_{out}(kT+T)-0] = C_3 \cdot v_{out}(kT+T). \tag{1.55}$$

Here the charge conservation is a key issue. The total amount of charge associated with the negative opamp input must be conserved from the previous phase. Hence we have

$$q_1(kT+T)+q_2(kT+T)+q_3(kT+T) = q_1(kT+\tau)+q_2(kT+\tau)+q_3(kT+\tau). \tag{1.56}$$

Combining (1.50) through (1.52) with (1.53) through (1.55) in (1.56) gives us

$$\begin{aligned} &0 + C_2 \cdot v_{in}(kT+T) + C_3 \cdot v_{out}(kT+T) = \\ &\quad = C_1 \cdot v_{in}(kT+\tau) + C_2 \cdot v_{in}(kT+\tau) + C_3 \cdot v_{out}(kT). \end{aligned} \tag{1.57}$$

Assuming that the input voltage is piecewise constant over the entire sample period as determined by $v_{in}(kT) = v_{in}(kT+\tau)$. We get

$$C_2 \cdot v_{in}(kT+T) - (C_1+C_2) \cdot v_{in}(kT) = C_3 \cdot v_{out}(kT) - C_3 \cdot v_{out}(kT+T). \tag{1.58}$$

Using the z transform gives us the following expression

$$C_2 \cdot V_{in}(z) \cdot z - (C_1 + C_2) \cdot V_{in}(z) = C_3 \cdot V_{out}(z) - C_3 \cdot V_{out}(z) \cdot z . \tag{1.59}$$

The transfer function becomes

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_2 - (C_1 + C_2) \cdot z^{-1}}{C_3 \cdot (1 - z^{-1})} = -\frac{C_2}{C_3} \cdot \frac{1 - (1 + C_1/C_2) \cdot z^{-1}}{1 - z^{-1}} . \tag{1.60}$$

We see that this is a filtering function. We have one pole at DC and one zero that can be moved by the C_1/C_2 ratio. If we now make the somewhat strange assumption that $C_1 = 0$ we get a transfer function that is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_2}{C_3} \cdot \frac{1 - z^{-1}}{1 - z^{-1}} = -\frac{C_2}{C_3} . \tag{1.61}$$

Hence we have a gain function, where the ratio between C_2 and C_3 determines the gain. The switching of C_3 is necessary to induce charge at the negative opamp input – otherwise this would be undefined.

As an alternative to the S/H above, we consider the S/H circuit shown in Fig. 11. As well as the previous circuit, this also uses a feature called *autozeroing* which allows us to cancel out much of the offset error. However, the gain of the circuit is unity – it is not possible to achieve any amplification, since there is only one capacitor. We will get back to this example after we have discussed the influence of nonideal components in SC circuits, see Sec. 1.7.5.

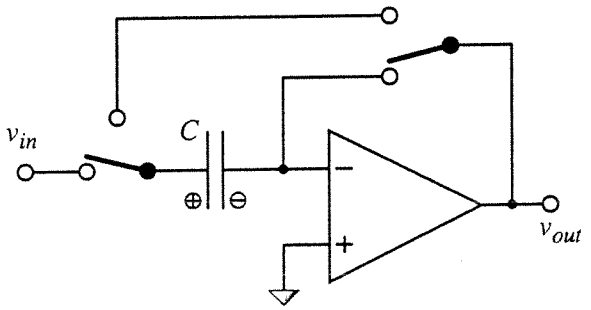


Figure 11: SC sample-and-hold with autozeroing.

1.7 Nonideal components

In reality we obviously do not have ideal components. We have already touched upon the influence of parasitics in the capacitors. In addition to this, we typically have the influence of the resistance in the switches as well as the finite gain and bandwidth of the operational amplifiers. There are more error sources, such as the limited driving capability of the opamps (slew rate), signal-dependent capacitance, noise, etc. They will however be left for the student to investigate.

1.7.1 Opamps with input offset voltage

One important issue is the influence of offset voltage at the input of the opamp. This can typically occur if there is mismatch between the transistors in the input differential pair. Consider the example of the accumulator from Fig. 9 (b) but shown in Fig. 12 with an off-

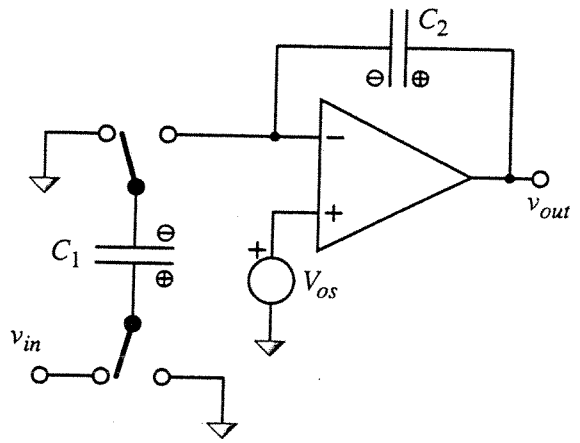


Figure 12: Illustration of offset voltage at the input of the amplifier.

set voltage, V_{os}, on the positive input of the opamp. We still assume an infinite gain and hence the voltage on the negative input will become V_{os} as well.

We will run through the charge redistribution analysis for the different phases. This time we will do it slightly differently to be able to cope with the offset error. We see that during the first phase (ϕ_1) we get

$$q_1(kT) = C_1 \cdot [v_{in}(kT) - 0] = C_1 \cdot v_{in}(kT). \tag{1.62}$$

The charge on the feedback capacitor will however become

$$q_2(kT) = C_2 \cdot [v_{out}(kT) - V_{os}]. \tag{1.63}$$

Since the charge must be conserved at the opamp's negative input node, we get that

$$q_2(kT) = q_2(kT - \tau) = C_2 \cdot [v_{out}(kT - \tau) - V_{os}]. \tag{1.64}$$

This gives us the (well-known) relation

$$v_{out}(kT) = v_{out}(kT - \tau). \tag{1.65}$$

During the next phase (ϕ_2), we have that C_1 will not loose all of its charge due to the non-zero voltage level at the negative input. The charge must be given by

$$q_1(kT + \tau) = C_1 \cdot [0 - V_{os}] = -C_1 \cdot V_{os}. \tag{1.66}$$

The charge on the feedback capacitor must be given by

$$q_2(kT + \tau) = C_2 \cdot [v_{out}(kT + \tau) - V_{os}]. \tag{1.67}$$

Due to the charge conservation between phase ϕ_1 and ϕ_2 at the negative input node we get the following relation

$$-q_1(kT) - q_2(kT) = -q_1(kT + \tau) - q_2(kT + \tau), \tag{1.68}$$

hence the "new" charge must equal the "old" charge. We get

$$C_1 \cdot v_{in}(kT) + C_2 \cdot [v_{out}(kT) - V_{os}] = -C_1 \cdot V_{os} + C_2 \cdot [v_{out}(kT + \tau) - V_{os}] \quad (1.69)$$

which becomes

$$C_1 \cdot v_{in}(kT) + C_2 \cdot v_{out}(kT) = -C_1 \cdot V_{os} + C_2 \cdot v_{out}(kT + \tau). \quad (1.70)$$

Once again assuming that the input voltage is maintained constant during one sample period and using (1.65). Now we get that

$$C_1 \cdot v_{in}(kT - \tau) + C_2 \cdot v_{out}(kT - \tau) = -C_1 \cdot V_{os} + C_2 \cdot v_{out}(kT + \tau). \quad (1.71)$$

Using the z-transform gives us the output as

$$V_{out}(z) = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_{in}(z) + \frac{C_1}{C_2} \cdot \frac{1}{1 - z^{-1}} \cdot V_{os}. \quad (1.72)$$

We do not have to care about the delay term for the offset voltage $z^{-1/2}$. From (1.72) we see that the offset voltage will be accumulated on the output as well. Therefore, we must be sure that we have a small enough offset voltage which does not saturate the accumulator output or use an autozeroed SCA (see Sec. 1.7.5).

1.7.2 Opamps with finite gain

Another limitation is the influence of the finite gain in the amplifier. When we have a finite gain, the voltage difference between the opamp inputs is not zero. If the positive input is left grounded, the negative input will become $v_x = -v_{out}(t)/A_0$, where A_0 is the gain of the amplifier and v_{out} is its output voltage.

As an example, we will once again use the accumulator from Fig. 9 (b) but we have now added the (signal-dependent) voltage source at the negative input node.

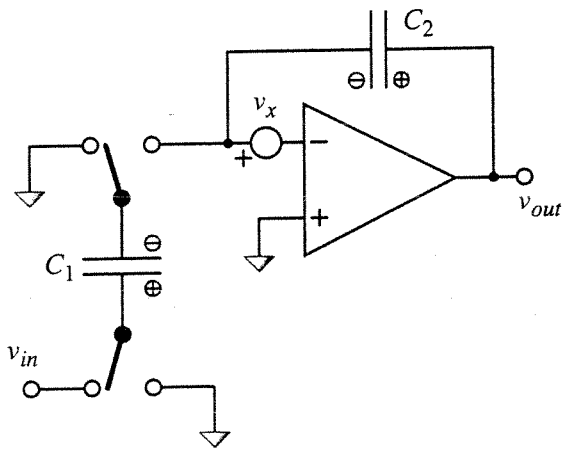


Figure 13: SC accumulator with non-zero input voltage difference due to finite gain.

We run through the charge redistribution analysis: We see that during the first phase (ϕ_1) we get for capacitor C_1:

$$q_1(kT) = C_1 \cdot [v_{in}(kT) - 0] = C_1 \cdot v_{in}(kT). \quad (1.73)$$

The charge on the feedback capacitor will however become

$$q_2(kT) = C_2 \cdot \left[v_{out}(kT) - \frac{-v_{out}(kT)}{A_0} \right] = C_2 \cdot v_{out}(kT) \cdot \left(1 + \frac{1}{A_0} \right). \quad (1.74)$$

Since the charge must be conserved at the opamp's negative input node, we get that

$$q_2(kT) = q_2(kT-\tau) = C_2 \cdot v_{out}(kT-\tau) \cdot \left(1 + \frac{1}{A_0}\right). \tag{1.75}$$

This gives us the relation between the output voltage at different time instants:

$$v_{out}(kT) = v_{out}(kT-\tau). \tag{1.76}$$

During phase ϕ_2, C_1 will once again not loose all of its charge due to the non-zero voltage difference at the opamp input. The charge must now be given by

$$q_1(kT+\tau) = C_1 \cdot \left[0 - \frac{-v_{out}(kT+\tau)}{A_0}\right] = C_1 \cdot \frac{v_{out}(kT+\tau)}{A_0}. \tag{1.77}$$

The charge on the feedback capacitor must be given by

$$q_2(kT+\tau) = C_2 \cdot \left[v_{out}(kT+\tau) - \frac{-v_{out}(kT+\tau)}{A_0}\right] = C_2 \cdot v_{out}(kT+\tau) \cdot \frac{1+A_0}{A_0}. \tag{1.78}$$

Due to the charge conservation between phase ϕ_1 and ϕ_2 at the negative input node we get the following relation

$$-q_1(kT) - q_2(kT) = -q_1(kT+\tau) - q_2(kT+\tau), \tag{1.79}$$

hence the "new" charge must equal the "old" charge. We get

$$\begin{aligned} &C_1 \cdot v_{in}(kT) + C_2 \cdot v_{out}(kT-\tau) \cdot \frac{1+A_0}{A_0} = \\ &= C_1 \cdot \frac{v_{out}(kT+\tau)}{A_0} + C_2 \cdot v_{out}(kT+\tau) \cdot \frac{1+A_0}{A_0}, \end{aligned} \tag{1.80}$$

As usual, we assume that the input voltage is constant during the whole sample period and using (1.76), we we get

$$C_1 \cdot v_{in}(kT-\tau) + C_2 \cdot v_{out}(kT-\tau) \cdot \frac{1+A_0}{A_0} = v_{out}(kT+\tau) \cdot \left(C_2 + \frac{C_1+C_2}{A_0}\right). \tag{1.81}$$

Using the z-transform gives us the output as

$$C_1 \cdot V_{in}(z) \cdot z^{-1} = V_{out}(z) \cdot \left(C_2 + \frac{C_1+C_2}{A_0}\right) - C_2 \cdot V_{out}(z) \cdot z^{-1} \cdot \frac{1+A_0}{A_0}. \tag{1.82}$$

Now we can find the transfer function as

$$A(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{\left(1 + \frac{1+C_1/C_2}{A_0}\right) - z^{-1} \cdot \frac{1+A_0}{A_0}}. \tag{1.83}$$

We rewrite this slightly and we get

$$A(z) = \frac{z^{-1}}{1 - z^{-1} \cdot \dfrac{1}{1 + \dfrac{C_1/C_2}{1 + A_0}}} \cdot \frac{C_1/C_2}{1 + \dfrac{1 + C_1/C_2}{A_0}}. \tag{1.84}$$

We see that we have two errors – one gain error and that the pole has moved away from $z = 1$. The latter implies that the integration is not ideal, we have a *lossy SCA*.

1.7.3 Switches with non-zero on-resistance

In reality, the switch (and wires, etc.) will have a certain resistance when they are closed. We will here just quickly overview how this influences the result. Call the parasitic resistance of the switch R_{on}. Since the charge current "through"[1] the capacitor, $i(t)$, is given by the time-derivative of the charge, we have the that

$$i(t) = \frac{dq(t)}{dt} = C \cdot \frac{dv(t)}{dt}. \tag{1.85}$$

With the resistance of the switch, we have that the voltage across the capacitor can be written as

$$v_C(t) = v_{in}(t) - R_{on} \cdot i(t) = v_{in}(t) - R_{on}C \cdot \frac{d}{dt}[v_{in}(t) - v_C(t)]. \tag{1.86}$$

This gives us an expression for the capacitor voltage as

$$v_C(t) - R_{on}C \cdot \frac{dv_C(t)}{dt} = v_{in}(t) - R_{on}C \cdot \frac{dv_{in}(t)}{dt}. \tag{1.87}$$

Now we assume that the input voltage is constant (the time-derivative is zero)

$$\frac{dv_{in}(t)}{dt} = 0 \tag{1.88}$$

and we get the well-known result

$$v_C(t) - R_{on}C \cdot \frac{dv_C(t)}{dt} = v_{in}(0) \Rightarrow v_C(t) = v_{in}(0) \cdot [1 - e^{-t/R_{on}C}]. \tag{1.89}$$

Since we are considering a discrete-time system, we are only interested in the voltages at multiples of the sample time $kT/2$. Hence, we have

$$v_C(kT + T/2) = v_{in}(kT) \cdot [1 - e^{-T/2R_{on}C}]. \tag{1.90}$$

Now, we have to design the circuit to be insensitive to the switch resistance. We want the settling error to be small, and hence we have

$$e^{-T/2R_{on}C} < \varepsilon \Rightarrow R_{on}C < \frac{-\ln \varepsilon}{T/2}, \tag{1.91}$$

where ε is a relative tolerance measure and $\tau_T = R_{on}C$ is the time constant of the capacitor.

1. The current does not really flow *through* the capacitor, it is the charge transported to the plates of the capacitors.

We now have two important options to choose from to meet the requirement in (1.91). We can (a) either design the circuit so that the relation above is met by reducing R_{on} or C or (b) we can do it by reducing the sampling time T. Consider the simulation result in Fig. 14, where we have plotted the timing constraints vs. the relative error, ε, for different sampling frequencies. The error has been varied from 0.01 to 10 per cent and the sample period from 1 KHz to 10 MHz. Notice the logarithmic scale on both the x and y axes.

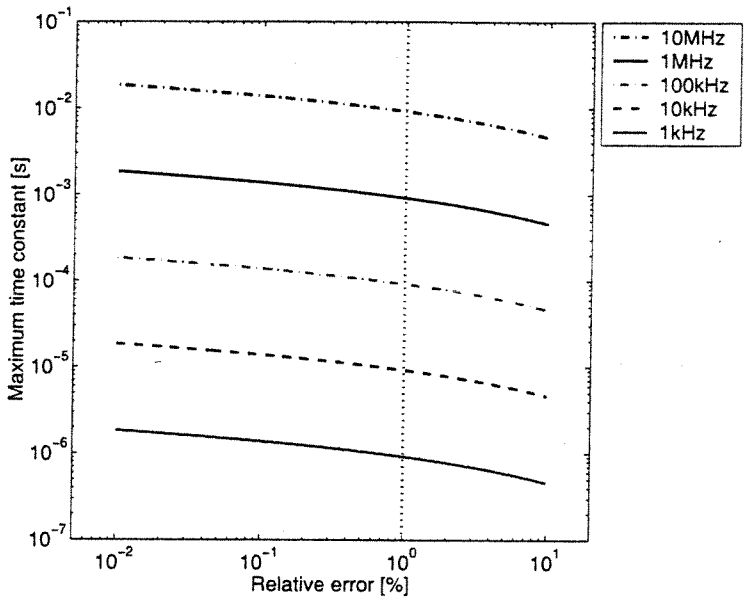


Figure 14: Simulated timing constraints as function of the relative error.

We see from (1.91) that for a 1-% error, the maximum time constant is given by $\tau_T \approx 9.2/T$ which becomes for example 0.9 µs for the 10-MHz sample frequency. With this discussion we want to illustrate the design methodology for choosing the size of your capacitors and the size of your switches. Mostly we implement the switches with MOS transistors or transmission gates[1]. The on-resistance of an NMOS switch is typically given by the inverse size of the transistor:

$$R_{on} = \frac{1}{(W/L)\cdot\beta\cdot V_x}. \tag{1.92}$$

The larger we make the switch the lower resistance, i.e., lower time constant. On the other hand we will then introduce parasitic capacitance from the switch transistors as well contributing to a complex analyses of the SC circuit. We will however consider these as second order effects and are to be considered when we actually implement our circuit.

1.7.4 Opamps with finite bandwidth

Another limitation is the influence of finite bandwidth operational amplifiers. We remember from the continuous-time case that the transfer function of an opamp with feedback and relatively high gain could be written as

$$A(s) = \frac{A_0}{1+\dfrac{s}{\beta\cdot\omega_u}}, \tag{1.93}$$

1. A transmission gate is a combined PMOS and NMOS switch.

if we assume a single, dominating pole. ω_u is the unity-gain frequency. This unity gain frequency is typically given by $\omega_u = g_m/C_L$ where g_m is the transconductance and C_L is the capacitance associated with the output node of the opamp. β is the feedback factor and is dependent on the capacitance (and resistance) in the feedback path. Hence, the amount of the output voltage that is fed back to the input. We can quit easily see that the feedback factor varies with the different phases. Consider the example in Fig. 8 (b). Here we see that during phase ϕ_1, capacitor C_1 is not connected to the opamp input and hence the feedback factor will be larger – closer to 1. During ϕ_2 we have that the feedback factor must be given by

$$\beta = \frac{C_1}{C_1 + C_2}. \tag{1.94}$$

We conclude that it is very important to investigate all phases of operation when you design opamps for SC circuit. The requirements on the phase margin and slew rate vary between the different phases.

Anyway, an amplifier with a limited bandwidth implies an amplifier with a finite output impedance. Therefore, the charging (and discharging) of the capacitors will follow a pattern very similar to that described for the non-ideal switches in Sec. 1.7.3. The opamp cannot change its output voltage infinitely fast. The output settling will be determined by the system described by (1.93) and hence the output voltage will typically be given by the start value at kT plus the ideal voltage step given by the end value at $kT + \tau$:

$$v_{out}(kT + t) = v_{out}(kT) + \Delta v_{out}(kT + \tau) \cdot [1 - e^{-t/\tau_O}], \tag{1.95}$$

where $\tau = T/2$ and $\tau_O = 1/\beta\omega_u$ is the time constant of the opamp. At the sampling instant, $t = \tau$, we get

$$v_{out}(kT + \tau) = v_{out}(kT) + \Delta v_{out}(kT + \tau) \cdot [1 - e^{-\tau/\tau_O}], \tag{1.96}$$

In the same way as for the switch on-resistance we understand from (1.96) that it is obvious that we must have a sample period that is much higher than the time constant to guarantee a small error.

Now we have a quite nice relation between the maximum allowable voltage step (Δv_{out}), the sampling frequency ($f = 1/T$), the current through the opamp ($I \propto g_m^2$), and the capacitance ($C_1, C_2 \propto \beta$).

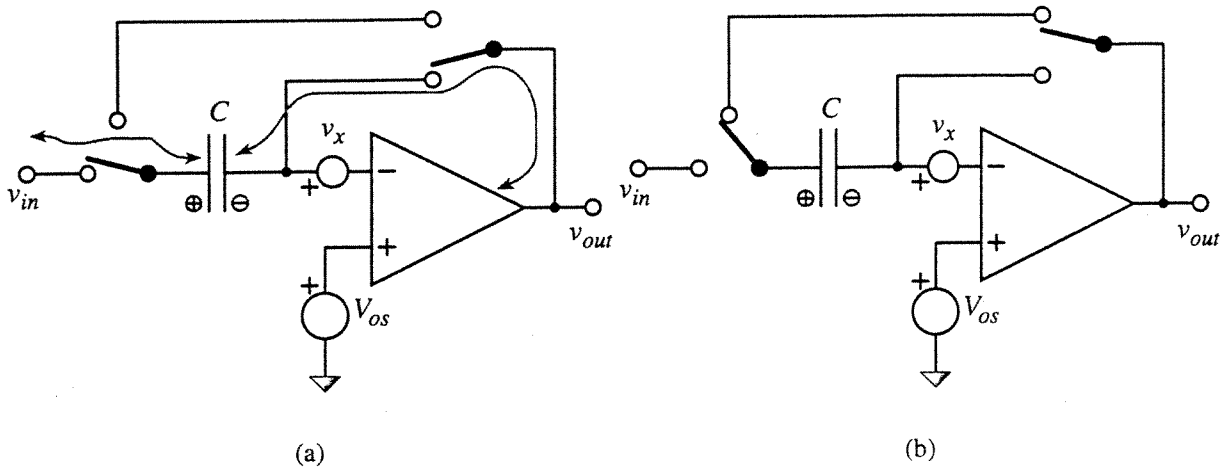
If we include a second pole in the transfer function (1.93) we will get the phase margin (which is a function of the "distance" between the poles) as a design parameter as well. See for example pp. 232-9 in [1]. In SC circuits a rule of thumb is to design our opamp to guarantee a 70-degree phase margin.

1.7.5 Sample-and-hold revisited

In Fig. 11 we illustrated a sample-and-hold circuit with so called autozeroing. This technique is used to minimize the influence of any offset voltage at the input of the opamp. We investigate the circuit by using the examples shown in Fig. 15. First we assume that the opamp is ideal. We have one sample and autozeroing phase (ϕ_1) and one hold phase (ϕ_2).

During the autozeroing phase, the input voltage is connected to the positive plate of the capacitor C and the opamp is connected in a buffer configuration. Since the gain is infinite the output voltage equals the ground voltage. Hence, the charge on the capacitor is

$$q(kT) = C \cdot [v_{in}(kT) - v_{out}(kT)] = C \cdot [v_{in}(kT) - 0] = C \cdot v_{in}(kT). \tag{1.97}$$



(a) (b)

Figure 15: Sample-and-hold circuit during (a) autozeroing (and sampling) phase and (b) hold phase.

During the next phase, we disconnect the input voltage from the capacitor, break the buffer feedback and connect the positive plate of the capacitor to the output node. No charge can disappear from the input of the opamp (to which the negative plate of the capacitor is connected). This implies that the charge on the capacitor is conserved and hence the voltage over the capacitor must equal that from the previous phase. We have that

$$q(kT+\tau) = C \cdot [v_{out}(kT+\tau) - 0] = C \cdot v_{out}(kT+\tau) = C \cdot v_{in}(kT). \tag{1.98}$$

We see that

$$v_{out}(kT+\tau) = v_{in}(kT), \tag{1.99}$$

where the output voltage is held during half the sample period. During the other half, it is reset to 0. We will have an output voltage "moving" fast between 0 and the input voltage level. Notice also that the input signal is continuous-time and that it is the input voltage level at the time instant $t = kT$ that is held at the output.

Now we add some nonidealties: Assume that there is mismatch between the input transistors of the opamp, hence we have an offset voltage. Also assume that we have a finite gain of the opamp, A_0. The voltage at the negative node will then be given by

$$V_{os} - \frac{v_{out}}{A_0}. \tag{1.100}$$

During the buffer configuration we see that the negative input is connected to the output and hence we get

$$v_{out} = V_{os} - \frac{v_{out}}{A_0} \Rightarrow v_{out} = \frac{V_{os}}{1 + 1/A_0}. \tag{1.101}$$

So during the autozeroing phase of the opamp (sample phase) we have that the true stored charge on the capacitor is

$$q(kT) = C \cdot \left[v_{in}(kT) - \frac{V_{os}}{1 + 1/A_0} \right]. \tag{1.102}$$

During the next phase, we fold over the capacitor and we now get that

$$q(kT+\tau) = C\cdot\left[v_{out}(kT+\tau)-\left(V_{os}-\frac{v_{out}(kT+\tau)}{A_0}\right)\right] =$$

$$= C\cdot\left[v_{out}(kT+\tau)\cdot\left(1+\frac{1}{A_0}\right)-V_{os}\right]. \qquad (1.103)$$

This "new" charge must equal the "old" charge due to the charge conservation at the negative input of the opamp and we get

$$v_{out}(kT+\tau) = \frac{v_{in}(kT)+V_{os}-\dfrac{V_{os}}{1+1/A_0}}{1+1/A_0} = \frac{v_{in}(kT)+\dfrac{V_{os}}{1+A_0}}{1+1/A_0}. \qquad (1.104)$$

We now see that the offset voltage is suppressed by the gain of the opamp: $V_{os}/(1+A_0)$. Let for example A_0 be infinite and you see that we reach the ideal case shown in (1.99).

1.8 Switched-capacitor filters

Since we have analyzed and designed our accumulator we are now able to create discrete-time filters according to any of the standard methods. (Actually our simplest SC filter is the accumulator itself which is a high pass filter – not very good though.) We have looked at the sample-and-hold to put at the input, the SCAs internally in the filter and gain circuits if they are required.

With a computer program (or from tables) we find our coefficients a_i and b_i in the transfer function for a certain filter

$$H(z) = \frac{b_0+b_1z^{-1}+\ldots+b_N\cdot z^{-N}}{a_0+a_1z^{-1}+\ldots+a_M\cdot z^{-M}}. \qquad (1.105)$$

We can now choose any way of realizing the filter from this function: we can use the direct forms, cascaded biquad links, or state-variable filters. The design and synthesis becomes very similar to that of digital filters. We have the same type of limiting factors; overflow and underflow due to high voltage across the capacitors, truncation noise due to finite gain and offset on the amplifiers, etc.

One standard solution of a state-variable filter (leapfrog) is shown in Fig. 16. This is a third-order filter, but increasing the order is relatively straight forward. It simulates the behavior of an RLC-reference filter. We see that it has three poles generated by the three SCAs. In the same way as in the continuous-time leapfrog filter, zeros can be created by introducing cross-coupled capacitors between the negative inputs of the upper and lower SCA. These will not become switched in the SC implementation either.

Notice that the SCAs are in principle identical with that of Fig. 8 (b), but they are modified to handle multiple inputs. This is achieved by connecting several capacitors controlled by one switch to the negative opamp input. The upper SCA has three inputs and the two lower only two inputs. Also notice that the sign of the output of the SCA can easily be changed by alter the position of the switch S_2 in Fig. 8 (b). This has been done for the "middle" SCA in Fig. 16. (Compare with the continuous-time case, where you must add an inverting buffer for the corresponding integrator).

A "simple" way to find the component values in a filter such as the one displayed above is to use the continuous-time state representation and perform a bilinear or LDI (lossless discrete integrator) transformation. Hence, we get something like

$$H(s) \rightarrow H(e^{j\omega T}) \rightarrow H(z), \qquad (1.106)$$

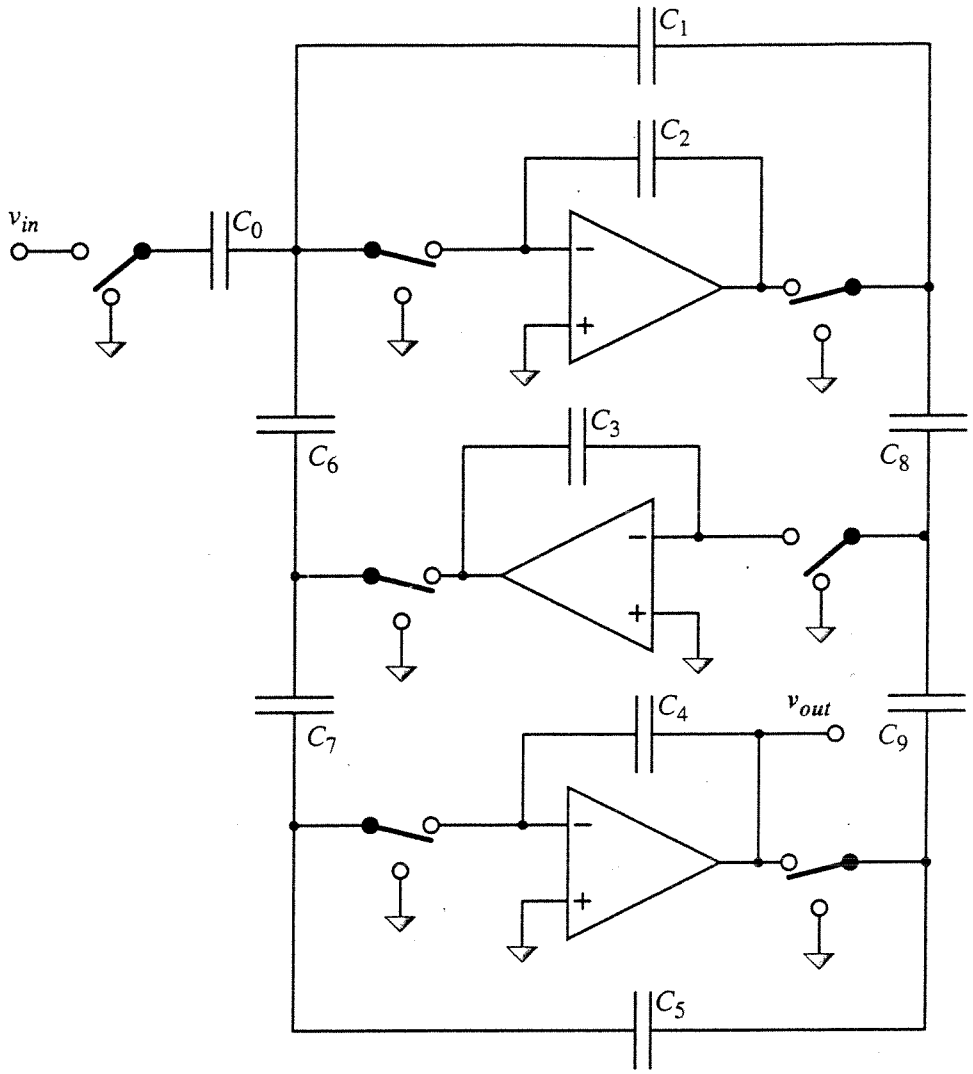


Figure 16: Third-order state-variable filter generated using the LDI transform.

The bilinear transform implies that we replace all the continuous-time integrators as

$$\frac{1}{s} = \frac{1}{s_0} \cdot \frac{1+z^{-1}}{1-z^{-1}}, \tag{1.107}$$

where s_0 is a scaling constant as

$$s_0 = \frac{\omega_a}{\tan(\omega T/2)}, \tag{1.108}$$

where ω_a is the angular frequency in the continuous-time domain and ωT is the angle in the digital domain. We can now choose a reference frequency for the scaling. With the LDI transform we replace all integrators with

$$\frac{1}{s} = \frac{1}{s_0} \cdot \frac{1}{z^{1/2}-z^{-1/2}}, \tag{1.109}$$

where s_0 once again is a scaling constant as

$$s_0 = \frac{\omega_a}{2\sin(\omega T/2)}. \tag{1.110}$$

The bilinear transform is able to cover the entire frequency range, which the LDI transform does not. On the other hand it has some advantages in terms of implementation complexity. This implies that the LDI transform should be used for narrow-band applications and the bilinear for wide-band applications. With narrow- and wide-band applications, we understand the ratio between the signal bandwidth and the sample frequency.

When we implement the discrete-time filter using the continuous-time leapfrog filter we roughly replace all the continuous-time integrators with the expressions found in (1.107) through (1.110). Some modifications have to be done, but they are only minor. Once again though, we should generate our filter and our component values with the help of a computer program.

1.9 References

[1] D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, New York, NY, USA, 1997.