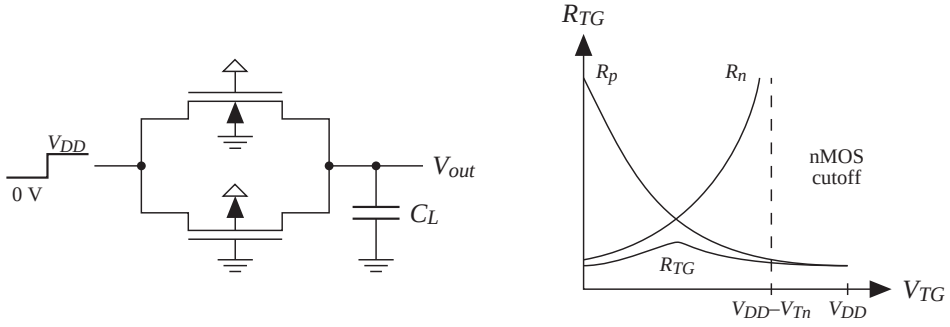
SOLUTIONS TO EXAM IN TSEI03 DIGITAL CIRCUITS 2019-10-21

1 a) $C_{ox}WL$

b) The *voltage transfer characteristic* is a plot that illustrates the input-output voltage behavior of a digital circuit. The output voltage is plotted on the vertical axis as a function of the input voltage on the horizontal axis.

c) The resistance of a transmission gate consists of parallel connected, nonlinear resistances of an NMOSFET and a PMOSFET. The resistance of one MOSFET increases when the resistance of the other decreases with changing voltage over the circuit. This behavior enables optimization of their relative sizes for approximately constant total resistance. See the example in the illustration below.



2 From the data it can be seen that $V_{DS} > V_{DSAT}$ for all sets $\Rightarrow$ no operating mode is resistive. To decide between saturated and velocity saturated operating modes we need to compare V_{GT} and $V_{DSAT} = 0.58$ V. Inspecting the data sets we see the smallest $V_{GT} = 2–V_T$. Hence we obtain that the MOSFET is velocity saturated for all sets if $2–V_T < 0.58 \Rightarrow V_T \leq 1.42$ V, which seems likely, so let us guess that and verify it later.

$$I_D = \left(k'\frac{W}{L}V_{DSAT}\right)\left(V_{GS} - V_{T0} - \frac{V_{DSAT}}{2}\right)\left(1+\lambda V_{DS}\right) = P_1 \cdot P_2 \cdot P_3$$

a) Find V_{T0} e.g. by comparing the relative currents of data set 1 and 2

$$\frac{I_{D1}}{I_{D2}} = \frac{P_1\left(2.5 - V_{T0} - \frac{0.58}{2}\right)P_3}{P_1\left(2.0 - V_{T0} - \frac{0.58}{2}\right)P_3} = \frac{1812}{1297} \Rightarrow V_{T0} \approx 0.45 \text{ V}$$

b) γ is easy to solve if we solve c) first

c) We can find $2|\Phi_F|$ in the V_T-equation for data set 4 and 5, so we start by finding V_T:s
Data set 2 is numerically close to 4 and 5, so we use that in calculations of V_{T4} and V_{T5}

$$\frac{I_{D2}}{I_{D4}} \approx \frac{P_1\left(2 - 0.45 - \frac{0.58}{2}\right)P_3}{P_1\left(2 - V_{T4} - \frac{0.58}{2}\right)P_3} = \frac{1297}{1141} \Rightarrow V_{T4} \approx 0.60 \text{ V}$$

$$\frac{I_{D2}}{I_{D5}} \approx \frac{P_1\left(2-0.45-\frac{0.58}{2}\right)P_3}{P_1\left(2-V_{T5}-\frac{0.58}{2}\right)P_3} = \frac{1297}{1039} \Rightarrow V_{T5} \approx 0.70 \text{ V}$$

Now we use the relation $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right)$ to find $2|\Phi_F|$

$$\text{Let } x = 2\phi_F\,(<0) \Rightarrow \frac{V_{T4}-V_{T0}}{V_{T5}-V_{T0}} = \frac{\sqrt{|1-x|}-\sqrt{|x|}}{\sqrt{|2-x|}-\sqrt{|x|}} = \frac{\sqrt{1-x}-\sqrt{-x}}{\sqrt{2-x}-\sqrt{-x}} \approx \frac{0.60-0.45}{0.70-0.45} \Rightarrow$$

$$x \approx -0.60 \text{ V} \Rightarrow 2|\phi_F| \approx 0.60 \text{ V}$$

b) *continued*

Insert numerical values into e.g. set 4

$$V_{T4} = V_{T0} + \gamma\left(\sqrt{\left|V_{SB4} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right) \approx 0.45 + \gamma\left(\sqrt{\left|1-(-0.60)\right|} - \sqrt{\left|-0.60\right|}\right) \approx 0.60$$

$$\Rightarrow \gamma \approx 0.30 \text{ V}^{1/2}$$

d) To find *W*/*L*, we e.g. start by finding λ from data set 2 and 3 that are numerically close

$$\frac{I_{D2}}{I_{D3}} = \frac{P_1P_2(1+\lambda\cdot 1.8)}{P_1P_2(1+\lambda\cdot 2.5)} = \frac{1297}{1361} \Rightarrow \lambda \approx 0.081 \text{ V}^{-1}$$

W/*L* can now be found from any of data sets, e.g. set 2

$$I_{D2} \approx 122\cdot 10^{-6}\cdot\frac{W}{L}\cdot 0.58\cdot\left(2-0.45-\frac{0.58}{2}\right)(1+0.081\cdot 1.8) \approx 1297\cdot 10^{-6} \Rightarrow \frac{W}{L} \approx 13$$

a), b), c), d): check assumption on threshold voltages

$$\left.\begin{array}{l} V_{BS1} = V_{BS2} = V_{BS3} = 0 \Rightarrow V_{T1} = V_{T2} = V_{T3} = V_{T0} \approx 0.45 \text{ V} \le 1.42 \text{ V} \\ V_{T4} \approx 0.60 \text{ V} \le 1.42 \text{ V} \\ V_{T5} \approx 0.70 \text{ V} \le 1.42 \text{ V} \end{array}\right\} \Rightarrow \text{assumption is ok}$$

3 a) Sheet resistance has the unit Ω/square since the resistance is constant per square of wire in between the terminals. This property is due to that the wire has constant thickness.

b) Resistance R_{wire} as a function of the wire length *L* and width *W*

$$R_{wire} = \frac{L}{W_{wire}}R_{sq} \Rightarrow L = \frac{R_{wire}}{R_{sq}}W_{wire} = \frac{2}{0.07}3 \text{ µm} \approx 86 \text{ µm}$$

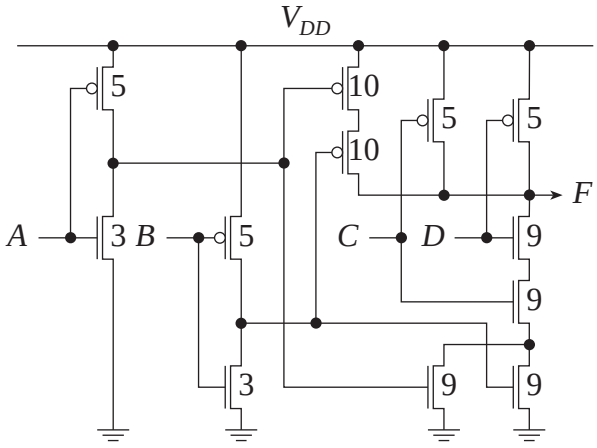
c) Total wire capacitance *C*:

$$C = W_{wire}LC_{area} + 2\left(W_{wire}+L\right)C_{edge} = 3\cdot 86\cdot 0.019 + 2\left(3+86\right)0.025 \text{ fF} \approx 9.3 \text{ fF}$$

4 a) Switch nets for function *F*:

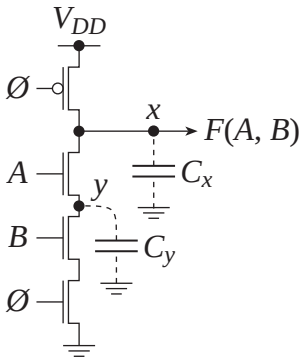
$$F = AB + \overline{CD} = AB + \overline{C} + \overline{D} \Rightarrow \begin{cases} S_p = F(\overline{A},\overline{B},\overline{C},\overline{D}) = \overline{A}\,\overline{B} + C + D \\ S_n = \overline{F(A,B,C,D)} = \overline{\overline{A}\,\overline{B} + C + D} = \left(\overline{A}+\overline{B}\right)CD \end{cases}$$

Two inverters are needed for A' and B'. A transistor schematic is shown below.



b) Aspect ratios are indicated directly by the transistors in the schematic above

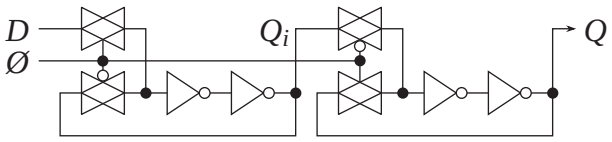
5 a) $F(A,B) = \overline{AB} \Rightarrow S_n = AB$. The corresponding transistor schematic is shown in the figure to the right.



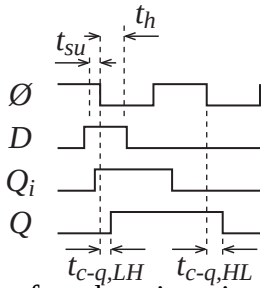
b) Capacitance C_x of node x indicated in the figure above is first precharged to V_{DD}, which is done by setting clock Ø low. Then the evaluation starts by setting clock Ø high, where a low A or low B disconnects the output from the supply, causing $F(A, B)$ to remain at approximately V_{DD} due to the previous precharge. If instead both A and B are high, the output is discharged and becomes low.

c) For case $F(A, B) = F(0, 1)$, capacitance C_y of node y indicated in the figure above is discharged. If the next evaluation is $F(A, B) = F(1, 0)$, the voltage of node x should remain at V_{DD}, but is instead reduced due to sharing of C_x's charge with C_y. Depending on how much the output voltage is reduced, we may need to redesign the circuit to ensure proper operation.

6 a) A positive edge-triggered master-slave D flip-flop is shown below



b) A timing diagram is shown to the right.



Setup time t_{su}: The time before the falling edge of the clock that the input data D must be valid.

Hold time t_h: The time that the input must be held stable after the falling edge of the clock. Note that the hold time of a circuit can be negative in certain situations.

Clock-to-output delays $T_{c\text{-}q,LH}$ and $T_{c\text{-}q,HL}$: The time after the triggering clock edge until the output Q is stable.

If the setup time or the hold time is violated the circuit might enter a metastable, undecided, state. The output will eventually reach a stable point, either high or low, but the final state will be more or less random.