Solutions to exam in TSEI03 Digital Circuits 2018-10-22

1.

a) The signal must be kept stable a time before (*setup time*) and a time after (*hold time*) the clock edge that initiates the memory state.

b) An *overlap capacitance* is the capacitance between the part of the gate and the source or drain areas that overlaps.

c) A *noise margin* is defined as the difference between the best output voltage and the worst input voltage that can be accepted. It measures the amount of noise that can be added to a node between two cascaded, identical gates without ruining the function.

d) *Charge leakage* will ruin the level when the gate is is dynamic state for a long time. Hence a minimal sample frequency is required for proper operation.

e) The gain is less than one for voltages up to V_{IL} and for voltages above V_{IH}. Hence noise is attenuated for these voltages.

2.

a) V_d is given by the voltage drop over the resistor due to constant current

$V_d = V_{dd} - RI$

$V_d = V_{dd} - RI = 2.5 - 10 \cdot 10^3 \cdot 50 \cdot 10^{-6}\ \text{V} = \underline{2.0\ \text{V}}$

Small R causes small voltage drop over R, and large over MOSFET. Try with saturated operating mode and solve for V_{GS}

$$I_d = \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 = 50\ \mu\text{A} \Rightarrow V_{GS} = \sqrt{I_d \frac{2}{k'}\frac{L}{W}} + V_T =$$

$$= \sqrt{50 \cdot 10^{-6} \frac{2}{115 \cdot 10^{-6}} \frac{0.25}{2.5}} + 0.43\ \text{V} = 0.72\ \text{V}$$

Find V_S

$V_S = V_G - V_{GS} = \underline{1.28\ \text{V}}$

Check operation mode

$V_{\min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(0.72 - 0.43, 2.0 - 1.28, 0.63\right) = V_{GT}$

The MOSFET is <u>saturated</u>.

b) Find V_d

$V_d = V_{dd} - RI = 2.5 - 30 \cdot 10^3 \cdot 50 \cdot 10^{-6}\ \text{V} = \underline{1.0\ \text{V}}$

Large R causes large voltage drop over R, and small over MOSFET. Try with linear operating mode and solve for V_S

$$I_d = k'\frac{W}{L}\left[\left(V_{GS}-V_T\right)V_{DS}-\frac{V_{DS}^2}{2}\right] = k'\frac{W}{L}\left[\left(V_G-V_S-V_T\right)\left(V_D-V_S\right)-\frac{\left(V_D-V_S\right)^2}{2}\right] = 50\ \mu\text{A}$$

$$\Leftrightarrow 115\cdot 10^{-6}\,\frac{2.5\cdot 10^{-6}}{0.25\cdot 10^{-6}}\left[\left(2.0-V_S-0.43\right)\left(1.0-V_S\right)-\frac{\left(1.0-V_S\right)^2}{2}\right] = 50\cdot 10^{-6} \Leftrightarrow$$

$$V_S^2 - 3.14V_S + \frac{2361}{1150} = 0 \Leftrightarrow V_S \approx 1.57 \pm 0.64\ \text{V} \Rightarrow$$

$$V_S \approx \underline{0.93\ \text{V}}$$

Check operation mode

$$V_{\min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(2.0-0.93-0.43, 1.0-0.93, 0.63\right) = V_{DS} = 0.07\ \text{V}$$

The MOSFET is <u>linear</u>.

3.

a) Sheet resistance has unit Ω/square since the resistance is constant for a square of wire in a certain layer. This property is due to that the wire has constant thickness.

b) Resistance *R* of the wire as a function of length *L*

$$R = \frac{L}{W}R_{sq} \Rightarrow L = \frac{R}{R_{sq}}W \approx 57\ \mu\text{m}$$

c) Total wire capacitance *C*

$$C = W_{min}LC_{area} + 2LC_{edge} \approx\ 13\ \text{fF}$$

4.

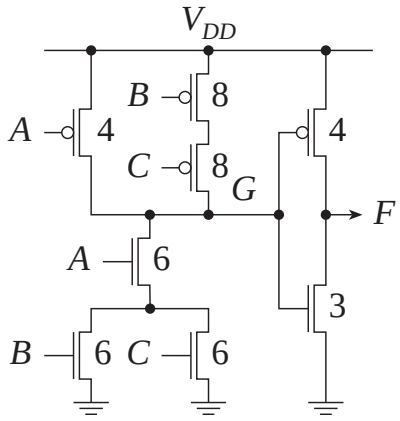
a) Simplify the logic function to contain as few variable entries as possible

$$F = AB + AC = A\left(B+C\right)$$

Since a static CMOS gate is inverting, we can design the function as the inverted output $G = F'$ and add an inverter to the output to obtain F
Switch nets for function G

$$G = \overline{A\left(B+C\right)} \Rightarrow \begin{cases} S_p = G(\overline{A},\overline{B},\overline{C}) = \overline{\overline{A}\left(\overline{B}+\overline{C}\right)} = A+BC \\ S_n = \overline{G(A,B,C)} = A\left(B+C\right) \end{cases}$$

Transistor schematic



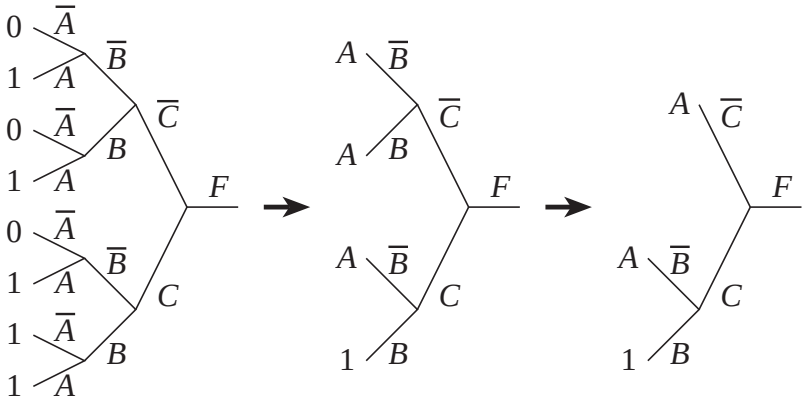
b) The worst-case resistance occurs when a single path conducts. A common sizing strategy is to design the widths of every single conduction path to be equal (when possible). Using $R \propto L/W$, the aspect ratios shown by the transistors in the schematic above can be calculated using this strategy

5.

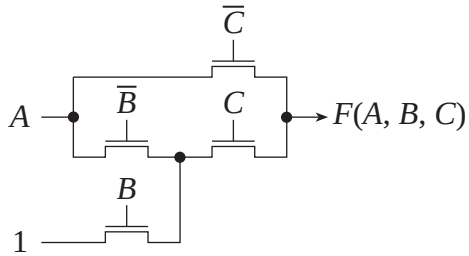
a) Pass transistor logic

b) $A \neq B$, $C = 1$ yields a short circuit between A and $B \Rightarrow$ output F will be undefined.

c) Below is a binary tree representing the function and its simplification in two steps.

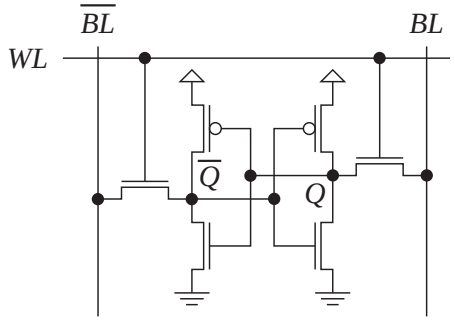


d) The optimized pass transistor circuit is shown below.



6.

a) Transistor schematic of a six-transistor CMOS SRAM cell



b) For example, to store $\bar{Q}$ = 0, Q = 1, WL is initially set to 0, $\overline{BL}$ is set to 0, and BL is set to 1. Then WL is pulsed high long enough to allow the crosscoupled inverter pair to change state hence storing the wanted content.

c) To read the cell content, WL is initially 0 while $\overline{BL}$ and BL are precharged to 1. Then WL is pulsed high long enough for the sense amplifier to detect the voltage drop on the bit-line that is pulled towards 0 by the weak transistors in the cell. Finally the sense amplifier amplifies the voltage difference to a full swing 0 and the result is output.

d) For proper write operation, the ratio between the pull-up PMOSFET and the select NMOSFET must be designed low enough to allow a 0 on the bit-line change the state of the corresponding memory node. For proper read operation, the ratio between the pull-down NMOSFET and the select NMOSFET needs to be designed high enough to prevent the memory node from changing state from 0 to 1 when the cell is connected to the precharged bit-line.