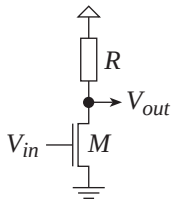
SOLUTIONS TO EXAM IN TSEI03 DIGITAL CIRCUITS 2017-10-18

1 a) The source is the terminal where the charge carriers enters the MOSFET and the drain is where they exit the MOSFET. For an n-channel MOSFET the source is the terminal with lowest potential compared with the drain, and for a p-channel MOSFET the source is the terminal with highest potential.

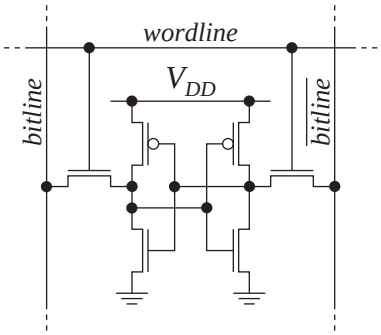
b) $C_{ox}WL$

c) An NMOS inverter consists of an nMOSFET and a load resistance (often implemented with a MOSFET) connected according to the schematic to the right. A low input switches off the MOSFET, causing the current through the resistor to charge the output to high. A high input switches on the MOSFET, which connects the output to ground, yielding a low output voltage.



d) The input signal must be stable during the *setup time* before and the *hold time* after the triggering clock edge arrives.

e) Six-transistor static RAM cell:



2 $V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{|2\Phi_F|}\right) = 0.40 + 0.40\left(\sqrt{|0.5 + 0.60|} - \sqrt{|-0.60|}\right)$ V ≈ 0.51 V

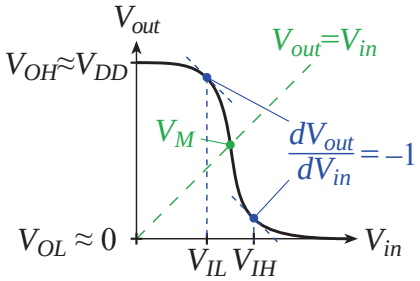
$V_{GS} = 1.0$ V $> V_T \approx 0.51$ V $\Rightarrow$ MOSFET is conducting

$V_{\min} = \min\left(|V_{GT}|, |V_{DS}|, |V_{DSAT}|\right) = \min\left(1.0 - 0.51, 1.5, 0.63\right)$ V $= |V_{GT}| \Rightarrow$ MOSFET is saturated

Relative error of I_{Dn}

$$e_{rel} = \left| \frac{k_n' \frac{W}{L} \frac{V_{GT}^2}{2}}{k_n' \frac{W}{L} \frac{V_{GT}^2}{2}\left(1 + \lambda V_{DS}\right)} - 1 \right| = \left| \frac{1}{1 + \lambda V_{DS}} - 1 \right| = \left| \frac{1}{1 + 0.06 \cdot 1.5} - 1 \right| \approx 0.083 = 8.3\ \%$$

3 VTC of a CMOS inverter:

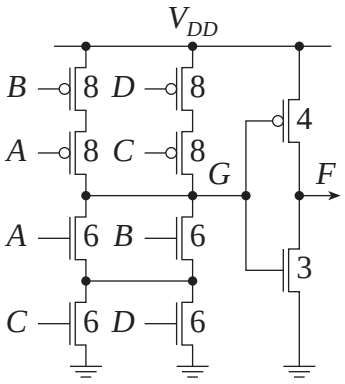


4 Since we are designing a non-inverting function, it is advantageous to realize the inverted function $G = F'$ and obtain F with a CMOS inverter at the output G.

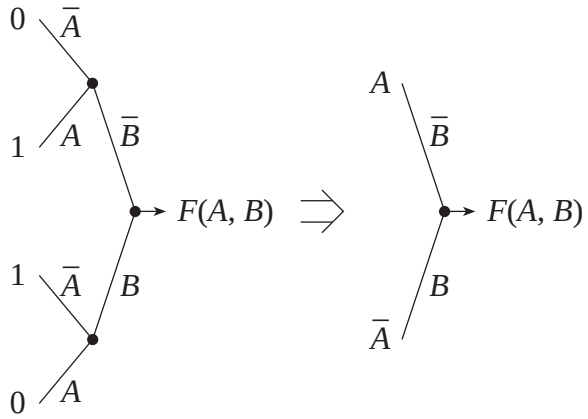
Switch nets: $G(A,B,C,D) = \overline{(A+B)(C+D)} \Rightarrow$

$$\begin{cases} S_p = G(\overline{A},\overline{B},\overline{C}) = \overline{(\overline{A}+\overline{B})(\overline{C}+\overline{D})} = AB + CD \\ S_n = \overline{G(A,B,C)} = \overline{\overline{(A+B)(C+D)}} = (A+B)(C+D) \end{cases}$$

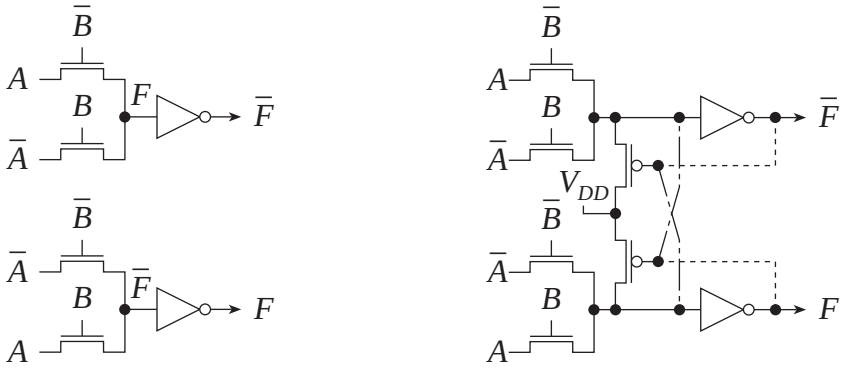
Transistor schematic with aspect ratios:



5 a) Realize e.g. as a binary tree and simplify



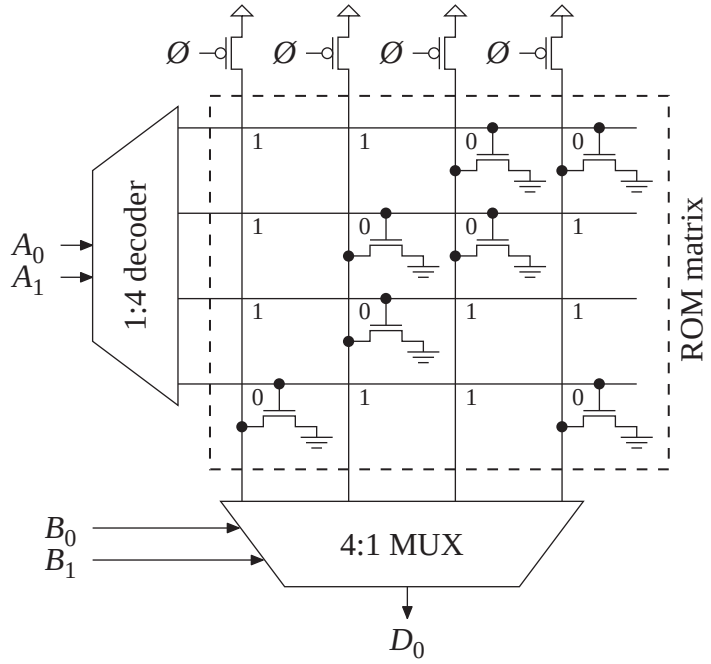
Replace branches with NMOSFETs and add inverter to output. Realize complementary output e.g. by inverting inputs to tree like in the figure to the left below:



b) Add keepers to the nodes with reduced swing before the inverters either connected
i) tradionally like shown with dashed line in the figure to the right above, or
ii) to the complementary net shown with dot-dashed line

6 a) The delay becomes less if both word and bit lines have a low, balanced capacitance, which is obtained with a square shaped ROM matrix. Hence a 4-by-4 matrix should be a good choice for a 16-bit ROM.

b) A block diagram for a 4-by-4 ROM is shown below.



c) Connect a transistor between the bitline and ground, controlled by the proper word line for a corresponding zero in the matrix. Leave the ones in the matrix unconnected. See the schematic inside the ROM matrix in the figure above.

7 a) $F(A, B) = AB$

b) Node x must first be precharged to V_{DD}, which is done by setting clock $Ø$ low. Then the evaluation starts by setting clock $Ø$ high, where a low A or low B disconnects x from the output, causing x to remain at V_{DD} due to the charged C_x. If instead both A and B are high, C_x is discharged and x becomes low. $F = x'$ is output due to the inverter on the output.

c) For case $F(A, B) = F(0, 1)$, C_y is discharged. If next evaluation is $F(A, B) = F(1, 0)$, node x is supposed to remain at V_{DD}, but does actually get a reduced voltage due to sharing of its charge with the initially discharged C_y.

d) A weak bleeder pMOSFET M_b can be introduced according to the figure to the right that conducts when C_x is precharged. The conduction replaces charges lost due to charge sharing.