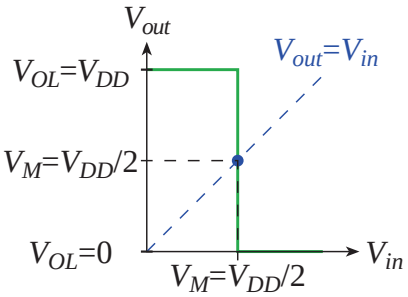
SOLUTIONS TO EXAM IN TSEI03 DIGITAL CIRCUITS 2017-01-07

1 a) Since $V_{out} > 0$, $V_{SB1} > 0 \Rightarrow V_{T1} > V_{T2} = V_{T0}$, i.e. V_T of M_1 is higher than V_T of M_2

b) An overlap capacitance is the capacitance between the part of the gate and the source or drain areas that overlaps.

c) Both the latch and the flip-flop are memory circuits, but while the latch is transparent during one clock phase, the flip-flop is never transparent. This behavior of the flip-flop is usually obtained by cascading two latches clocked on opposite clock phases.

d) The VTC of an ideal inverter is shown below



2 $V_T = V_{T0} + \gamma\left(\sqrt{\left|V_{SB} - 2\Phi_F\right|} - \sqrt{\left|2\Phi_F\right|}\right) = -0.40 - 0.40\left(\sqrt{\left|-0.5 - 0.60\right|} - \sqrt{\left|-0.60\right|}\right)$ V ≈ -0.51 V

$V_{GS} = -1.5$ V $< V_T \approx -0.51$ V $\Rightarrow$ MOSFET is conducting

$V_{\min} = \min\left(\left|V_{GT}\right|, \left|V_{DS}\right|, \left|V_{DSAT}\right|\right) = \min\left(1.5 - 0.51, 1.0, 1.0\right) = \left|V_{GT}\right| \Rightarrow$ MOSFET is saturated

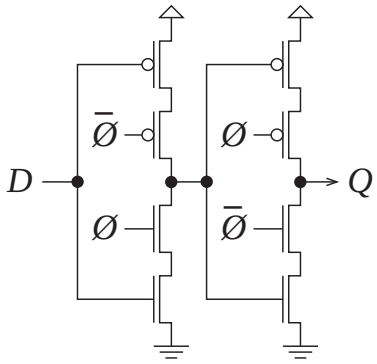
Relative error of I_{Dp}

$$e_{rel} = \left| \frac{k_p' \frac{W}{L} \frac{V_{GT}^2}{2}}{k_p' \frac{W}{L} \frac{V_{GT}^2}{2}\left(1 + \lambda V_{DS}\right)} - 1 \right| = \left| \frac{1}{1 + \lambda V_{DS}} - 1 \right| = \left| \frac{1}{1 + \left(-0.10\right)\left(-1.0\right)} - 1 \right| \approx 0.091 = 9.1\,\%$$

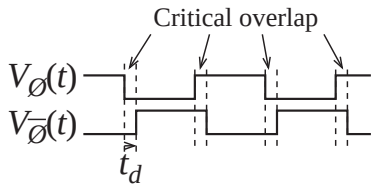
3 a) A: n+, B: p+, C: p+, D: n+, E: n+, F: p+, G: n–, H: p–

b) 1: VIA, 2: field oxide, 3: PMOS source, 4: PMOS gate, 5: PMOS drain,
6: NMOS drain contact, 7: metal 1, 8: metal 2, 9: n-well contact, 10: gate oxide,
11: field oxide, 12: NMOS gate, 13: NMOS source, 14: p-well contact

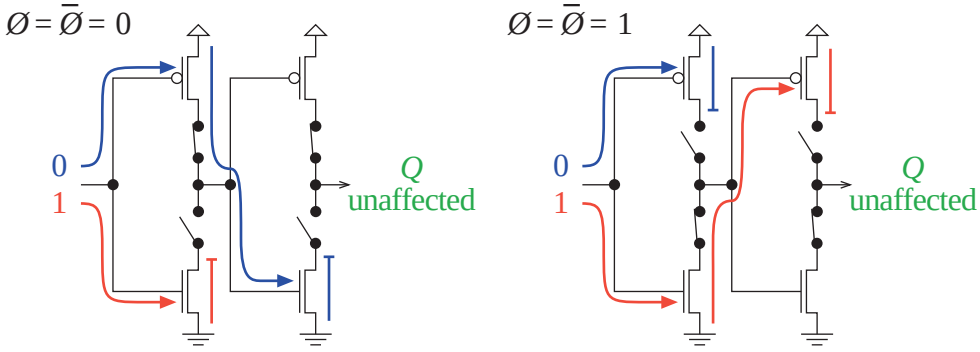
4 a) Connect two C^2MOS latches in series such that the first latch is transparent before the triggering clock edge and in memory state after the edge. In this case a high Ø should make the latch transparent, and after the positive edge a low Ø should activate the dynamic memory state. The second latch should then be connected in opposite. Below is a schematic for the flip-flop.



b) Below is a timing diagram for the clock phases when the complement is delayed t_d.



The flip-flop works normally when the clock and its complement really are complementary. However, in the timing diagram we can see periods where the phases overlap, causing the phases to simultaneously have a low or high value for times of t_d. Let us analyze these critical overlap states to find out if the flip-flop still behaves properly. In the figure below the two error cases of both clock phases being low or high have been illustrated by replacing the clock transistors with switches that are on or of depending on case.



If a low input is present at the flip-flop input, we can see that for the case to the left when the phases both are low, the signal will be inverted by the first latch and then is propagated to the second latch that blocks the low input from propagating to the output. If on the other hand a high input is present at the flip-flop input, we see that the signal is directly blocked by the first latch. Hence the flip-flop is never transparent for this case and works properly.

For the case with both clock phases high as shown to the left, we have the complementary case with respect to clock transistors that are on and off, and lows and highs as input. Here a low input is directly blocked from propagating by the first latch, and a high input is blocked from propagating by the second latch, making the flip-flop to not be transparent for this case as well.

Since this flip-flop does not become transparent, which a flip-flop never should be, we conclude that it will work properly although the phases are not complementary during a clock skew t_d. Problems may however still occur if rise and fall times are long, but this was not to be considered here.

5 a) Domino logic

b) Denoting the intermediate node at the inverter input *G*, the function is

$$S_n = A + B + C \Rightarrow G = \overline{S_n\left(A,B,C\right)} = \overline{A + B + C}$$

$$F = \overline{G} \Rightarrow F = A + B + C$$

c) The clocked PMOSFET is used to precharge *G* high, which will be the output value if the logic net does not conduct. The clocked NMOSFET is used to evaluate the logic function by connecting the logic net to ground. If the net conducts, *G* will be discharged to 0.

d) *G* is either precharged or evaluated, and *F* is a static output. The only case with possible charge sharing is during precharge, but assuming normal operation the internal node is connected to the supply via the evaluation MOSFET. Hence charge sharing *cannot occur* for this circuit (for an input without glitches as required in domino logic).

e) Charge leakage can become a problem if *G* is high during the evaluation phase and the phase is long enough. Then subthreshold leakage of the logic net will eventually discharge *G* partially, causing the inverter to consume a larger static current and leaving less margin for noise.

f) Use minimum *L* for all MOSFETs

The PMOSFET pull-ups consist of single transistors $\Rightarrow W_{P,inv} = 3$
The inverter NMOSFET consists of a single transistor $\Rightarrow W_{N,inv} = 2$

Design all NMOSFETs in a single path of the precharged gate to be the width of $W_{N,inv}$

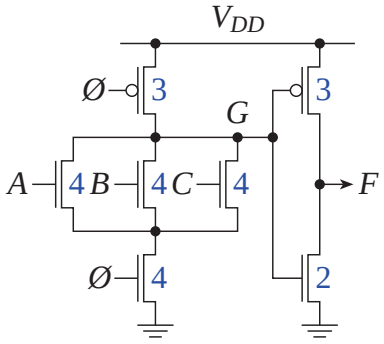
$$R_{on} \propto \frac{L}{W} \Rightarrow \frac{L}{W_{N,A}} + \frac{L}{W_{N,Ø}} = \frac{L}{W_{N,B}} + \frac{L}{W_{N,Ø}} = \frac{L}{W_{N,C}} + \frac{L}{W_{N,Ø}} = \frac{L}{W_{N,inv}} = \frac{1}{2}$$

$$\Rightarrow \frac{1}{W_{N,A}} + \frac{1}{W_{N,Ø}} = \frac{1}{W_{N,B}} + \frac{1}{W_{N,Ø}} = \frac{1}{W_{N,C}} + \frac{1}{W_{N,Ø}} = \frac{1}{2}$$

Design all NMOSFETs above with same width W_N

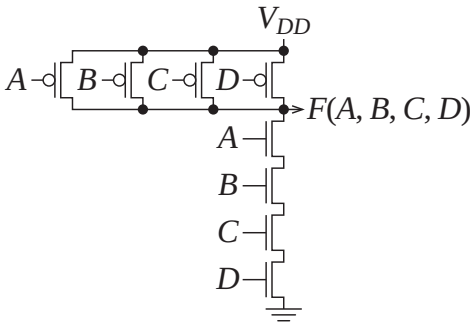
$$\frac{1}{W_N} + \frac{1}{W_N} = \frac{1}{2} \Rightarrow W_N = 4$$

The gate with aspect ratios indicated is shown in the schematic to the right



6 a) Here we can e.g. choose to implement a four-input NAND gate, i.e. $F\left(A,B,C,D\right)=\overline{ABCD}$

b) $S_p = F\left(\overline{A},\overline{B},\overline{C},\overline{D}\right) = A+B+C+D,\ S_n = \overline{F\left(A,B,C,D\right)} = ABCD \Rightarrow$ schematic



c) The equivalent resistance is *highest* when only one of the path conducts. For the pull-up this is when *A* or *B* or *C* or *D* is low, while the other signals are high. For the pull-down all MOSFETs must be on to yield a low output, requiring *A* and *B* and *C* and *D* to be high.

The equivalent resistance is *lowest* when all paths conduct. For the pull-up this is when *A* and *B* and *C* and *D* is low, and for the pull-down when *A* and *B* and *C* and *D* are high.