DIGITAL CIRCUITS

Exam

TSEI03

Time:	Wednesday 2017-10-18, 8:00—12:00
Place:	TER2
Teacher:	Mark Vesterbacka, phone 013-281324
Allowed aids:	Calculator and attached formulary (last two pages)
Max score:	70
Grades:	30 points for 3 40 points for 4 50 points for 5
Solutions:	Posted on the course web
Display:	Time and place will be posted with the LADOK results

1 a) What terminal is the *source* and what terminal is the *drain* in a MOSFET? (2 p)

b) What is the maximal value on the *gate capacitance* of a MOSFET? (2 p)

c) Describe the operation of an *NMOS inverter*. (2 p)

d) What restrictions are imposed on the flip-flop inputs to avoid *metastability*? (2 p)

e) Draw a *six-transistor SRAM cell* schematic. (2 p)

2 Consider a NMOS implemented in a 0.25 µm technology. The width-to-length ratio is $W/L = 2$ and the MOSFET is biased to $V_{GS} = 1.0$ V, $V_{DS} = 1.5$ V, and $V_{SB} = 0.50$ V. How large is the relative error in I_D if λ is assumed to be 0 instead of 0.06 V? (10 p)

3 Draw the voltage transfer characteristic of a typical CMOS inverter. Indicate V_{IL}, V_{OL}, V_{IH}, V_{OH}, and V_M in the drawing. (6 p)

4 Design a static CMOS circuit with function $F = (A+B)\cdot(C+D)$. Size all transistor nets to have similar output resistance as an inverter with $W_p/L_p = 4$ and $W_n/L_n = 3$. (10 p)

5 Design a complementary pass transistor logic circuit with function $F(A, B) = \overline{A}B + A\overline{B}$. Assume that complements to A and B are available.

a) Implement the circuit with at most four NMOSFETs plus two inverters. (8 p)

b) Suggest a solution to reduce the short-circuit currents of the inverters. (4 p)

6 Design a 16-bit ROM with the memory content {1,1,0,0,1,0,0,1,1,0,1,1,0,1,1,0} and a one-bit output.

a) What would be a good aspect ratio of the ROM matrix to have a short delay? (2 p)

b) Draw a block diagram over the complete ROM containing row and column decoders, precharged bit line pull-ups, and memory matrix. (4 p)

c) Draw the transistor schematic of the NOR ROM matrix. (4 p)

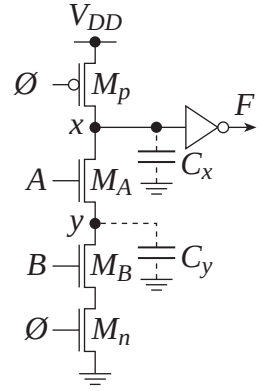
7 A dynamic gate with two parasitic capacitors C_x and C_y indicated is shown in the figure to the right.

a) What logic function has been implemented? (2 p)

b) Explain the operation of the circuit. (4 p)

c) Explain how charge sharing may occur. (3 p)

d) Suggest a way of mitigating the problem with charge sharing. (3 p)



Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

V_{DSAT} dependency on channel length

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{\text{V}}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq} C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.