DIGITAL CIRCUITS

Exam

TSEI03

Time:	Saturday 2017-01-07, 8:00—12:00
Place:	TER2
Teacher:	Jerzy Dąbrowski, phone 013-281224
Allowed aids:	Calculator and attached formulary (last two pages)
Max score:	70
Grades:	30 points for 3 40 points for 4 50 points for 5
Solutions:	Posted on the course web
Display:	Time and place will be posted with the LADOK results

1

a) Which MOSFET in Figure 1 has the highest *threshold voltage* if V_{out} is positive? Motivate your answer. (2 p)

b) What is an *overlap capacitance*? (2 p)

c) What is the main difference in function between a *latch* and a *flip-flop* circuit? (2 p)

d) Sketch the *voltage transfer characteristic* of an ideal inverter. Indicate V_{OL}, V_M, and V_{OH} and in the drawing. (4 p)

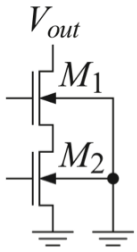

Figure 1. MOSFETs.

2 Consider a PMOS implemented in a 0.25 µm technology. The width-to-length ratio is W/L = 2 and the MOSFET is biased to V_{GS} = –1.5 V, V_{DS} = –1.0 V, and V_{SB} = –0.50 V. How large is the relative error in I_D if λ is assumed to be 0 instead of –0.10 V? (10 p)

3 A cross section of a static CMOS inverter implemented in a 45 nm n-well CMOS technology is shown in Figure 2 below.

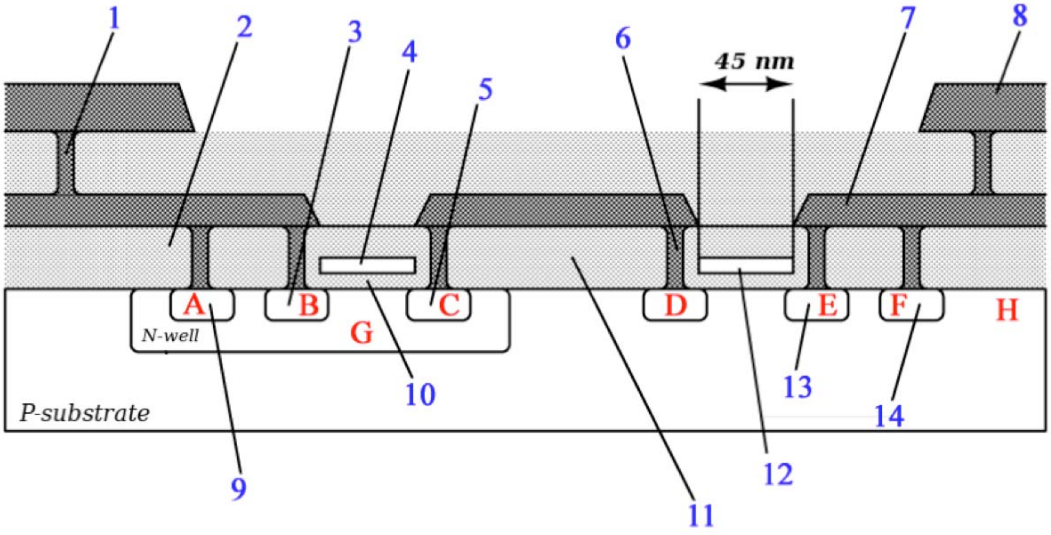

Figure 2. Cross section of a static CMOS inverter.

a) Assign doping levels p+, n+, p–, and n– to the objects indicated by letters A-H. (3 p)

b) Assign the following names to the objects indicated by the numbers 1-14: field oxide, gate oxide, p-well contact, n-well contact, PMOS gate, PMOS drain, PMOS source, NMOS gate, NMOS source, NMOS drain contact, metal 1, metal 2, VIA.(7 p)

4 A dynamic D flip-flop should be implemented using C^{2}MOS latches. Both the clock $Ø$ and its complement $Ø'$ are available.

a) Draw the transistor schematic of a negative edge-triggered flip-flop. (6 p)

b) Assuming sharp edges of the clock phases, show that the flip-flop still works as a flip-flop even if there is clock skew delaying the complement of the clock. (6 p)

5 A realization of a logic function $F(A, B, C)$ is shown in Figure 3.

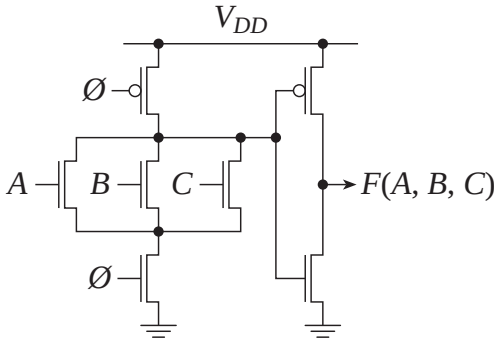

Figure 3. Transistor schematic of a logic gate.

a) What logic style has been used? (2 p)

b) What logic function $F(A, B, C)$ has been implemented? (2 p)

c) What is purpose of the clocked MOSFETs? (2 p)

d) Can charge sharing occur in the circuit? Motivate your answer. (2 p)

e) Can charge leakage be a problem in the circuit? Motivate your answer. (2 p)

f) Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 3$. (6 p)

6 Design a static CMOS gate that implements a Booelan function $F(A, B, C, D)$. You choose what function to implement, but it has to be a function of four variables.

a) What logic function have you implemented? (2 p)

b) Draw the transistor schematic of your implementation. (6 p)

c) What input pattern(s) would give the lowest and highest equivalent pull-up or pull-down resistance? (4 p)

Equations for the MOS transistor

Definition of source (*S*) and drain (*D*)

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

Voltage notations

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

Unified model

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***V_{DSAT}* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

Subthreshold region

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{V}$]	V_{DSAT} [V]	k' [μA/V^2]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	–0.30
PMOS	–0.40	–0.40	–1.00	–30	–0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/μm^2]	C_O [fF/μm]	C_j [fF/μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \le 0,\ V_{GTp} \ge 0$	$C_{ox}WL$	0	0
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$	0	$C_{ox}WL/2$	$C_{ox}WL/2$
$V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$	0	$2C_{ox}WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq} C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

Boolean algebra

De Morgans' theorem

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

Expansion in sum

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

Expansion in product

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$\upsilon = 1/\sqrt{lc}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j".

R_{ij} = "the sum of all resistances in P_{ij}".

Time constant from node 0 to i: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.