Lesson 7

11.1) For this problem you are given a cell library consisting of full adders and two-input Boolean gates (i.e. AND, OR, INVERT, etc.).

a) Design an N-bit two's complement subtracter using a minimal number of Boolean logic gates. The result of this process should be a block diagram. Specify the value of any required control signals (e.g. , C_{in}).

b) Express the delay of your design as a function of N, t_{carry}, t_{sum}, and the Boolean gate delays (t_{and}, t_{or}, t_{inv}, etc.).

11.2) The circuit of Fig. 11.1 implements a 1-bit datapath function in dynamic (precharge/ evaluate) logic.

a) Write down the Boolean expressions for outputs F and G. On which clock phases are outputs F and G valid?

b) To what datapath function could this unit be most directly applied (e.g., addition, subtraction, comparison, shifting)?

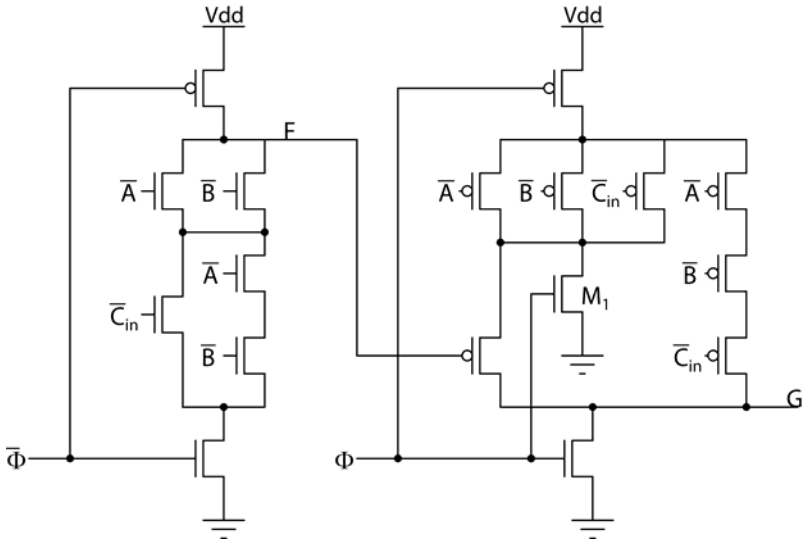


Figure 11.1. Datapath module bit-slice.

11.3) Consider the dynamic logic circuit of Fig. 11.1.

a) What is the purpose of transistor M_1? Is there another way to achieve this end that would reduce capacitive loading on Φ?

b) How can the evaluation phase of F be sped up by rearranging transistors? No transistors should be added, deleted, or resized.

11.4) The adder circuit in Fig. 11.2 makes extensive use of the transmission gate EXOR.

a) Explain how this gate operates. Derive the logic expression for the various circuit nodes. Why is this a good adder circuit?

b) Derive a first-order approximation of the capacitance on the C_o-node in equivalent gate- capacitances. Assume that gate and diffusion capacitances are approximately identical. Compare your result with the circuit of figure 11-6 in the course book.

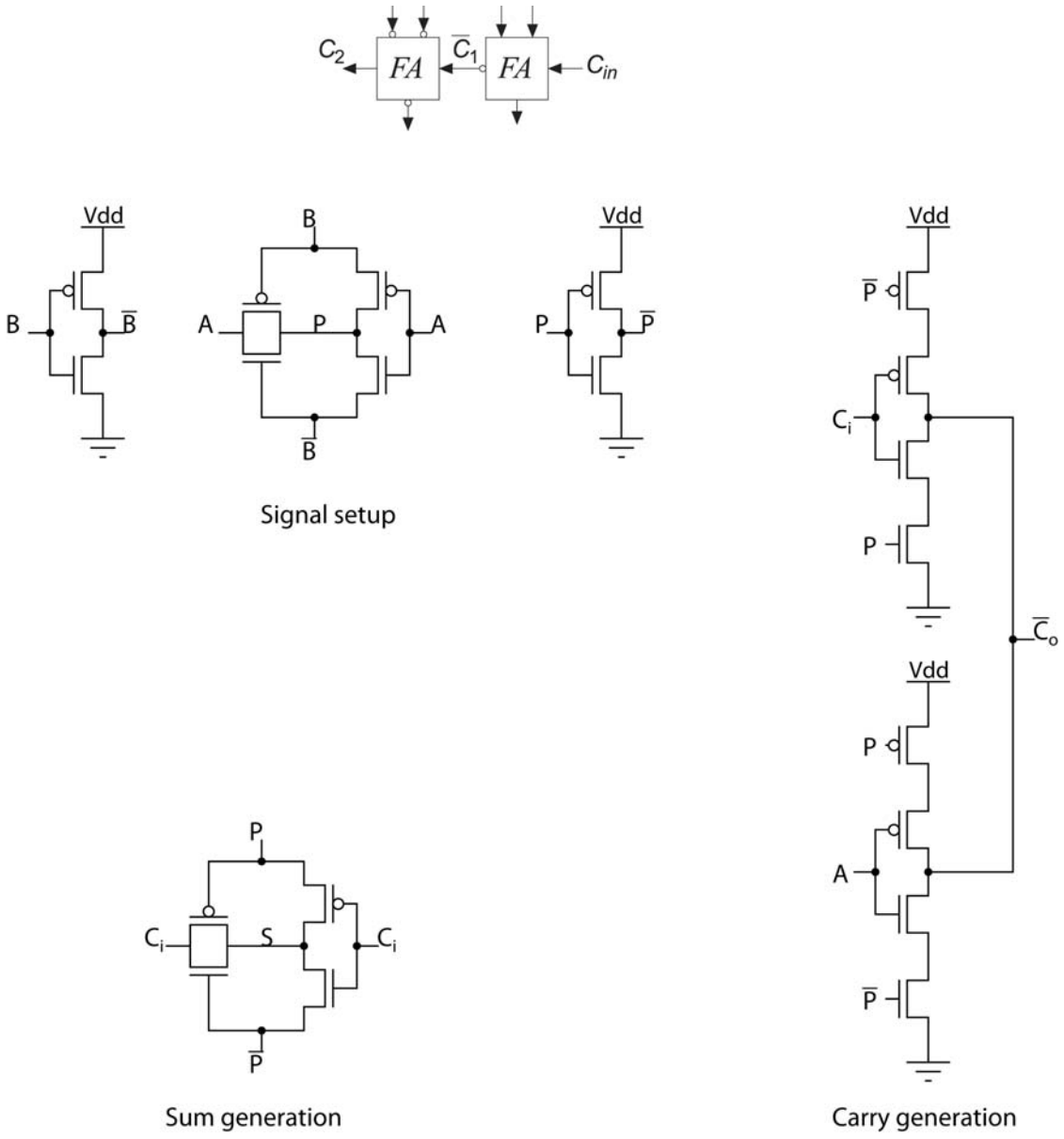
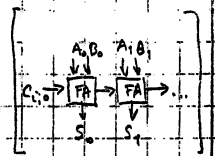


Figure 11.2. Adder circuit.

11.1 For this problem you are given a cell library consisting of full adders and two-input Boolean logic gates (i.e. AND, OR, INVERT etc.)



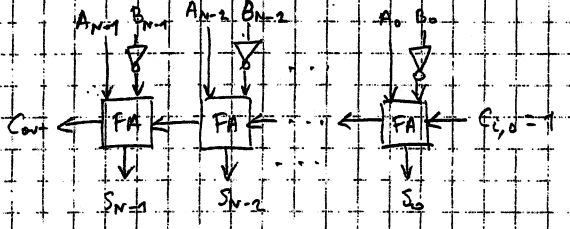
a) Design an N-bit two's complement subtracter using a minimal number of Boolean logic gates. The result of this process should be block diagram. Specify the value of any required control signals (e.g. Ci,0)

"A two's complement subtracter can be realized by combining a two's complement adder with an extra inversion stage"

Two's complement numbers:

- POSITIVE NUMBERS: Keep the bits as they are
- NEGATIVE NUMBERS: (INVERT ALL BITS), (ADD ONE)

ex		
	111	7
	110	6
	101	5
	100	4
	011	3
	010	2
	001	1
	000	0
	111	-1
	110	-2
	101	-3
	100	-4
	011	-5
	010	-6



$A - B = A + \bar{B} + 1$ SUBTRACTION IN TWO'S COMPLEMENT

b) Express the delay of your design as a function of N, t_{carry}, t_{sum} and the Boolean gate delays (t_{and}, t_{or}, t_{inv}, etc.)

$$t = t_{inv} + (N-1)\,t_{carry} + t_{sum}$$

- t_{inv}: INVERT THE INPUTS OF B.
- $(N-1)\,t_{carry}$: CARRY RIPPLES THROUGH THE CHAIN UP TO S_{N-1}
- t_{sum}: CALCULATION OF S_{N-1}

(11.2) The circuit of figure X11-1 implements a 1-bit datapath function in dynamic (precharge/evaluate) logic.

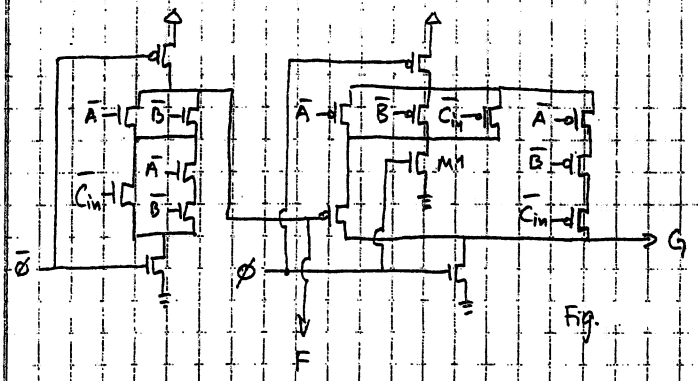


Fig.

a) Write down the Boolean expressions for outputs F and G. On which clock phases are outputs F and G valid?

$F = \overline{S_n} = \overline{(\bar{A}+\bar{B})(\bar{C}_{in}+A\bar{B})} = \bar{A}\bar{B} + \bar{C}_{in}(\bar{A}+\bar{B}) = A\bar{B} + C_{in}(A+B)$

F is valid when $\bar{\phi} = 1$

$S_p(A, B, C_{in}, F) = (\bar{A}\bar{B}\bar{C}_{in}) + (\bar{A}+\bar{B}+\bar{C}_{in})F$

$G = S_p(\bar{A}, \bar{B}, \bar{C}_{in}, \bar{F}) = (ABC_{in}) + (A+B+C_{in})\bar{F} =$

$= (ABC_{in}) + (A+B+C_{in})(\bar{A}+\bar{B})(\bar{C}_{in}+A\bar{B}) =$

$= (ABC_{in}) + (A\bar{A} + A\bar{B} + \bar{A}B + B\bar{B} + C_{in}\bar{A} + C_{in}\bar{B})(\bar{C}_{in}+A\bar{B}) =$

$= (ABC_{in}) + A\bar{B}\bar{C}_{in} + A\bar{B}\bar{A}\bar{B} + \bar{A}B\bar{C}_{in} + \bar{A}B\bar{A}\bar{B} + C_{in}\bar{C}_{in}\bar{A} + C_{in}A\bar{B} + C_{in}\bar{C}_{in}\bar{B} + C_{in}A\bar{B} =$

$= ABC_{in} + A\bar{B}\bar{C}_{in} + \bar{A}B\bar{C}_{in} + C_{in}A\bar{B} =$

$= \underbrace{(A\oplus B)\bar{C}_{in}} + \overline{(A\oplus B)}C_{in}$

$= A \oplus B \oplus C_{in}$

G is valid when $\phi = 0$

b) To what datapath function could this unit be most directly applied (e.g. addition, subtraction, comparison, shifting)

F = CARRY OUT
G = SUM
} ⇒ FULL-ADDER!

11.3

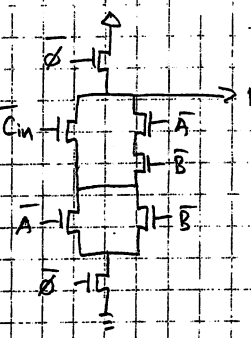
Consider the dynamic logic circuit of figure X11-1. (See Exercise 11.2)

a) What is the purpose of transistor M1? Is there another way to achieve this end that would reduce the capacitive loading on the ϕ?

M1 precharges the evaluation node $(A+B+C_{in})$ to ensure that there is no charge sharing between this node and G. Otherwise erroneously high values may occur.
To reduce clock loading, the gate of M1 may be tied to V_{DD}; that is a static BLEEDER. Use small (W/L) to reduce current and minimize silicon area.

b) How can the evaluation phase of F be sped up by rearranging transistors? No transistors should be added, deleted or resized.

After rearranging:



Place $\bar{C}_{in}$ (slow signal) closest to the output. While the circuitry "waits" for $\bar{C}_{in}$ to arrive, the internal nodes are discharged.

c) Can evaluation of G be sped up in the same manner? Why or why not?

No! G depends on F and C_{in}. C_{in} always arrives before F is computed. F has already been placed closest to G's output.

11.4 The adder circuit of Figure X11-2 makes extensive use of the transmission gate EXOR. $V_{DD} = 5V$

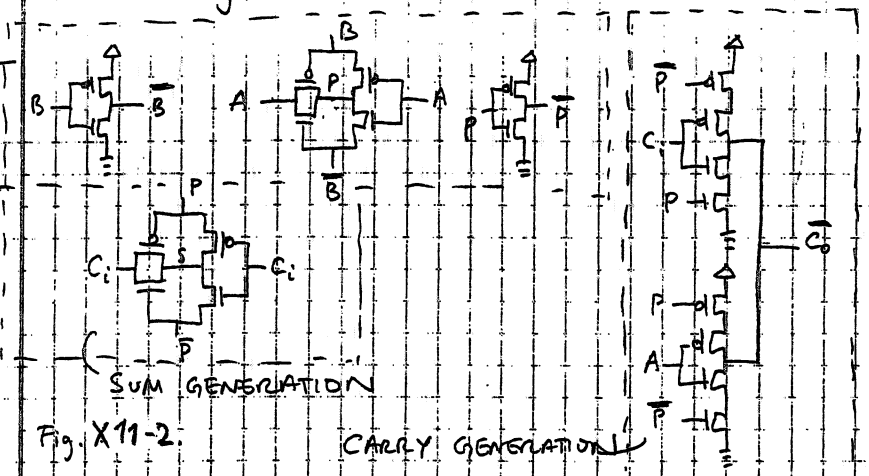
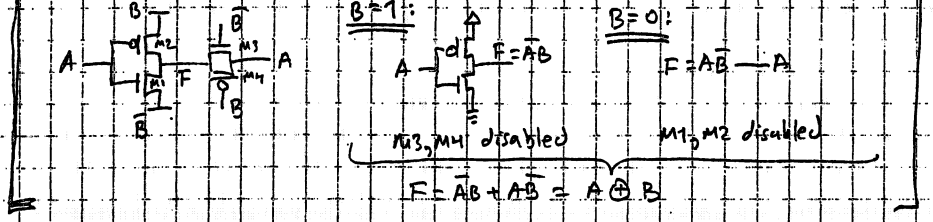


Fig. X11-2.

a) Explain how this gate operates. Derive the logic expression for the various circuit nodes. Why is this a good adder circuit?

TRANSMISSION GATE XOR:



$P = A \oplus B$

$S = P \oplus C_i = A \oplus B \oplus C_i$

$\bar{C}_o = (PC_i + \bar{P}A) = (\bar{A}B + A\bar{B})C_i + A(\bar{A}\bar{B} + AB) =$

This is the PDN

$= \bar{A}BC_i + A\bar{B}C_i + A\bar{A}\bar{B} + AB =$

$= \bar{A}BC_i + A\bar{B}C_i + AB$

P can be calculated before the carry signal arrives. The critical path is now no more than 2 devices in series. To minimize the delay once the carry arrives is key to fast operation of an adder.

11.4 continued...

b) Derive a first-order approximation of the capacitance on the C_o-node in equivalent gate-capacitances. Assume that gate and diffusion capacitances are approximately identical. Compare your results with the circuit of figure 11-6

This circuit loads the C_o-node with 6 diffusion capacitances (4 internal and 2 from next cell) and 4 gate capacitances (from next cell) $\approx$ 10 gate cap

Fig 11-6 has 4 diffusion capacitances and 8 gate capacitances
$\sim$ 12 gate capacitances

12.1) For a memory containing a 4096word X 2048bit array of SRAM cells with a differential bit-line architecture, where the dynamic power consumption is dominated by charging and discharging the bit lines. The cells are tiled at a vertical pitch of 24μm and a horisontal pitch of 15μm. Each cell adds a load of 20fF to BL and BL. Bit lines are in metal1 and are 3μm wide. In this process, metal1 has an area capacitance of C_a=0.031fF/μm^2 and a fringing capacitance of C_f=0.044fF/μm.

a) Compute the capacitance loading each bit line. Break it down into contributions from wiring and and from memory cells.

b) Assume that the bit lines are precharged to 2.5V and are allowed to develop a maximum differential voltage of 2V (symmetric around the precharge voltage) during a read operation,. After reading a PMOS transistor is used to equalize the charges on the bitlines. What is the power consumption by the memory while reading at an access rate of 1MHz? Assume Vdd = 5V.

12.2) A 5-transistor SRAM cell is shown in Fig. 12.1. The bit line is precharged to Vdd before reading. The power supply voltage is 2.5 V and the channel length is 0.25 μm for all transistors.

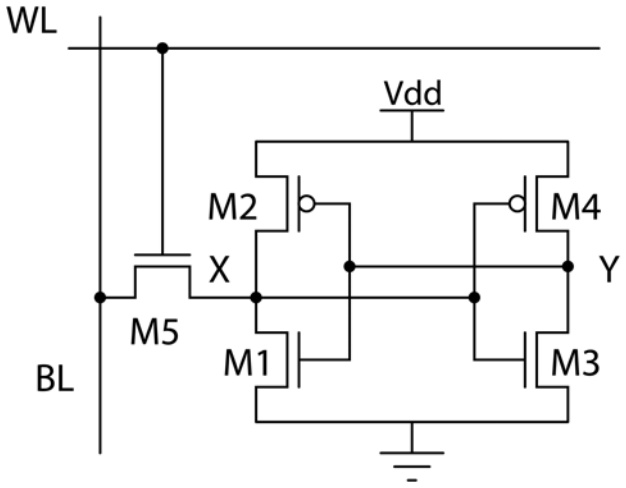


Figure 12.1. Five-transistor SRAM cell.

a) Describe the three constraints that should be imposed on the devices for guaranteeing safe read and write operations. Write down the equations and relations that would help you to size the transistors. Assume

$$V_M = V_{dd}/2$$

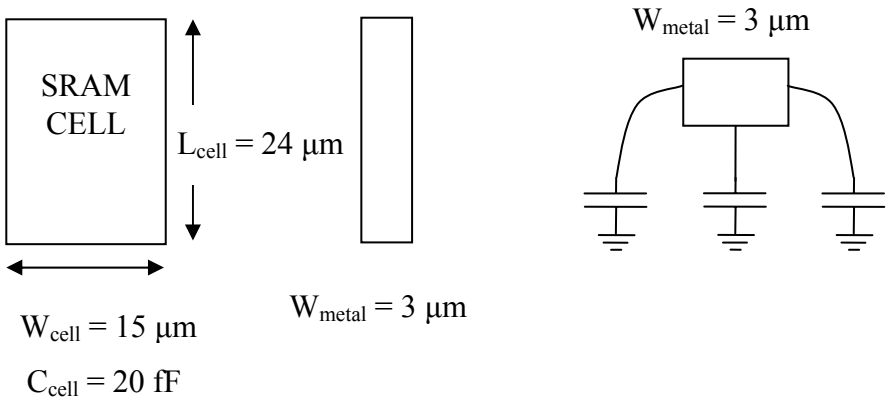
for the inverter formed by M4 and M3.

b) Based on the equations from a), discuss the required relative sizing of the transistors in the cell (e.g. transistor Mx must be *k* times wider than transistor My...).

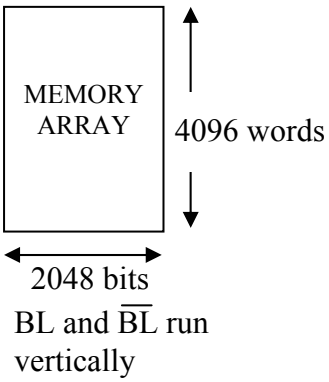
12.3) Draw the transistor diagram of a two-port SRAM cell. A two-port memory can read or write two independent addresses simultaneously. Discuss qualitatively how this affects the transistor sizing in the cell.

12.1

For a memory containing a 4096 x 2048 bit array of SRAM cells with a differential bit line architecture, assume that the dynamic power consumption is dominated by charging and discharging the bit lines. The cells are tiled at a vertical pitch of 24 μm and a horizontal pitch of 15 μm. Each cell adds a load of 20fF to BL and BL. Bit lines are in metal1 and are 3 μm wide. In this process metal1 has an area capacitance of
$C_a = 0.031$ fF/μm^2 and a fringing capacitance of $C_f = 0.044$ fF/μm



a) Compute the capacitance loading each bit line. Break it down into contributions from wiring and from memory cells.



Wiring capacitance / cell:

$C_w = L_{cell} * W_{metal} * C_a + 2 * L_{cell} * C_f =$

$= 24\ \mu m * 3\ \mu m * 0.031\ fF/\mu m^2 + 2 * 24\ \mu m * 0.044\ fF/\mu m$
$= 4.4344$ fF

Total capacitance on the bit line:

$C_{BL} = 4096 (C_w + C_{cell}) = 4096 (4.344 + 20)$ fF $= 99.7$pF

b) If the bit lines are precharged to 2.5V and are allowed to develop a maximum differential voltage of 2V (symmetric around the precharge voltage) during a read operation, what is the power consumption by the memory while reading at an acess rate of 1 MHz?

The charges that has to be taken from the power supple is $\Delta Q = \Delta V * C$
The corresponding energy taken from the power supply is $E = \Delta Q * V_{DD} = \Delta V * C * V_{DD}$
During equalization, no new charges have to be added. Hence $P_{bitline} = f * C * \Delta V * V_{DD}$
And so $P_{Memory} = 2048 * P_{bitline} = 1.02$ W

(12.2) a) cont'd

(II) Write a "one" in x.

V_x must be forced above V_M.

$I_5 > I_1$ for $V_x \leq V_M$ must be fulfilled!

☆ Consider $V_x = V_M = \frac{V_{dd}}{2}$ $V_{BL} = V_{dd}$ $V_{WL} = V_{dd}$

M5 $V_{SB} = V_x = \frac{V_{dd}}{2}$ $V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{2|\phi_F|}\right)$

$V_T = 0.43 + 0.40\left(\sqrt{1.25+0.6} - \sqrt{0.6}\right) = 0.6642V$

$V_{min} = \min\left(V_{dd} - V_x - V_T,\ V_{dd} - V_x,\ V_{DSAT}\right) = \min(0.586,\ 1.25,\ 0.63$

$= 0.586 \Rightarrow$ Saturation

$I_5 = 115\cdot10^{-6}\frac{W_5}{L_5}\,0.586\left(0.586 - \frac{0.586}{2}\right)(1 + 0.06\cdot1.25) = 2.122\cdot10^{-5}\frac{W_5}{L_5}$

M1 $V_{min} = \min\left(V_{dd} - V_T,\ V_x,\ V_{DSAT}\right) = \min(2.07,\ 1.25,\ 0.63)$

$V_{min} = 0.63 \Rightarrow$ vel. saturation.

$I_1 = 115\cdot10^{-6}\frac{W_1}{L_1}\,0.63\left(2.07 - \frac{0.63}{2}\right)(1 + 0.06\cdot1.25) = 1.367\cdot10^{-4}\frac{W}{L_1}$

$I_5 > I_1 \Rightarrow W_5 > 6.44\,W_1$

(III) Reading a "zero"

BL starts on Vdd & $V_{WL} = V_{dd}$. This is the same case as in (I) except that $I_5 < |I_2| \Rightarrow W_5 < 0.40\,W_2$

This is contradictory!

(IV) Reading a "one"

No problems! BL is precharged to Vdd and x starts on Vdd.

(I) $\Rightarrow$ $W_5 > 0.40\,W_2$

(II) $\Rightarrow$ $W_5 > 6.4\,W_1$

(IV) $\Rightarrow$ $W_5 < 0.40\,W_2$ (I) & (IV) contradictory!

Precharge BL to Vdd/2 when reading, to make the memory to work!

(12.2) a) (I) Write a "zero" in node X (Vdd in y)

X starts high ($V_X = V_{dd}$) $V_{WL} = V_{dd}$ $V_{BL} = 0V$.

If V_X is forced below V_M, then the right-hand inverter will change its output from 0V to Vdd, which turns off M2 and turn on M1. The writing has succeeded!

Hence, to write a zero in X: $I_5 > |I_2|$ for $V_X \geq V_M$ must be fulfilled.

✡ Consider $V_X = V_M = \frac{V_{dd}}{2}$

M5 $V_{min} = \min(V_{dd} - V_T, V_X, V_{DSAT}) = \min(2.07, 1.25, 0.63)$

$V_{min} = 0.63 \Rightarrow$ vel. sat.

$$I_5 = 115 \cdot 10^{-6} \frac{W_5}{L_5} \, 0.63 \left(2.07 - \frac{0.63}{2}\right)(1 + 0.06 \cdot 1.25) \approx 1.367 \cdot 10^{-4} \frac{W_5}{L_5}$$

M2 $V_{min} = \min(|-V_{dd} + |V_{T_p}||, |V_X - V_{dd}|, |V_{DSAT}|)$

$V_{min} = \min(2.1, 1.25, 1.0) = 1.0 \Rightarrow$ vel. sat.

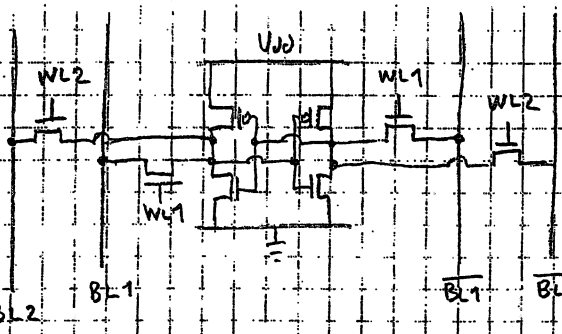
$$|I_2| = 30 \cdot 10^{-6} \frac{W_2}{L_2} \, 1.0 \left(2.1 - \frac{1.0}{2}\right)(1 + (-0.1)(-1.25)) = 5.40 \cdot 10^{-5} \frac{W_2}{L_2}$$

$$I_5 > |I_2| \Rightarrow 1.367 \cdot 10^{-4} \frac{W_5}{L_5} > 5.40 \cdot 10^{-5} \frac{W_2}{L_2}$$

$L_2 = L_5 \Rightarrow$ $W_5 > 0.40 \, W_2$

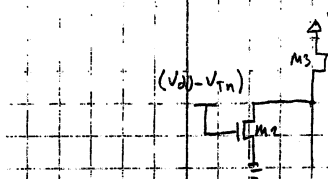
12.3

Draw the transistor diagram of a two-port SRAM cell. A two-port memory can read or write two independent addresses simultaneously. Discuss qualitatively how this affects the transistor sizing in the cell.



Transistor sizing doesn't change as WL1 and WL2 should never be on at the same time

b) Determine the maximum possible current flowing into the cell during a read operation. State clearly your assumptions and simplifications.



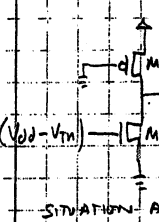
Maximum current flows when M2 STARTS switching

M2 saturation? $V_{DS} > V_{GS} - V_{Tn}$; $V_{DD} > V_{DD} - V_{Tn} - V_{Tn}$; $0 > -2 \cdot V_{Tn}$

ok, M2 SATURATION !

$$I_{d,max} \approx \frac{k_n'}{2}\left(\frac{W}{L_{eff}}\right)(V_{GS}-V_{Tn})^2 = \Big/ \begin{matrix} pp.62: \\ k_n' = 19,6 \cdot 10^{-6} A/V^2 \\ L_{eff} = L - 2 \cdot x_d = \\ = 1,2 - 2 \cdot 0,15 = \\ = 0,9\ \mu m \\ V_{Tn} = 0,743\ V \end{matrix} \Big/ = \frac{19,6 \cdot 10^{-6}}{2}\left(\frac{1,8}{0,9}\right)(3-2 \cdot 0,743)^2 = \approx 45,3\ \mu A$$

c) Determine the size (W/L) of transistor M3 so that the voltage on the bit line BB never drops below 2,5 V during a read operation.



- M3 linear? $V_{SD} < V_{SG} - |V_{Tp}|$; $-2,5 < -|V_{tp}|$; $2,5 < -0,739$

ok, M3 LINEAR

- M2 saturation? $V_{DS} > V_{GS} - V_{Tn}$; $2,5 > V_{DD} - V_{Tn} - V_{Tn}$; $2,5 > 3 - 2 \cdot 0,743$

$2,5 > 1,514$

ok, M2 SATURATION

OBS ! $\left(\frac{W}{L_{eff}}\right)_2 = \left(\frac{1,8}{0,9}\right)$

$$I_{d2} = I_{d3}$$

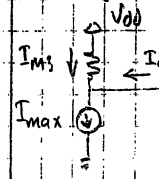
$$\frac{k_n'}{2}\left(\frac{W}{L_{eff}}\right)_2 (V_{GS2}-V_{Tn})^2 = k_p'\left(\frac{W}{L_{eff}}\right)_3 \left[(V_{SG3}-|V_{Tp}|)V_{SD3} - \frac{V_{SD3}^2}{2}\right]$$

$$\left(\frac{W}{L_{eff}}\right)_3 = \frac{\frac{k_n'}{2}\left(\frac{W}{L_{eff}}\right)_2 (V_{GS2}-V_{Tn})^2}{k_p'\left[(V_{SG3}-|V_{Tp}|)V_{SD3} - \frac{V_{SD3}^2}{2}\right]} = \frac{k_n'\left(\frac{W}{L_{eff}}\right)_2 (V_{DD}-2V_{Tn})^2}{2k_p'\left[(V_{DD}-|V_{Tp}|)(V_{DD}-2,5) - \frac{(V_{DD}-2,5)^2}{2}\right]} =$$

$$= \Big/ \begin{matrix} pp.62 \\ k_n' = 19,6\ \mu A/V^2 \\ k_p' = 5,4\ \mu A/V^2 \\ V_{Tn} = 0,743\ V \\ V_{Tp} = -0,739\ V \end{matrix} \Big/ = \frac{19,6 \cdot 2(3-2 \cdot 0,743)^2}{2 \cdot 5,4\left[(3-0,739)(3-2,5) - \frac{(3-2,5)^2}{2}\right]} = 8,27\ldots$$

$$\left(\frac{W}{L_{eff}}\right)_3 \approx 8,3$$

d) Compute the time it takes to achieve a 0,5 V voltage drop on the bit line during a read operation. Assume $C_L = 50\ fF$ and $C_b = 2\ pF$.



$$I_{avg} = I_{cb} \approx \frac{I_{cb}|_{V_{out}=2,5V} - I_{cb}|_{V_{out}=3V}}{2} = \frac{I_{max} - 0}{2} = \frac{45,3 \cdot 10^{-6}}{2}$$

[in general: $C = \frac{Q}{V}$; $I = Q/t$ || $C = \frac{I \cdot t}{V} \Leftrightarrow t = \frac{C \cdot V}{I}$]

$$t = \frac{C_L \cdot \Delta V}{I_{avg}} = \Big/ C_L = C_b = 2\ pF \Big/ = \frac{2 \cdot 10^{-12}(3-2,5)}{\frac{45,3 \cdot 10^{-6}}{2}} = 44,1501\ldots ns \approx 44\ ns$$