Lesson 6

7.1) The indicated waveforms are applied to the JK master-slave flip-flop of Fig 7.1. For this problem, assume that gate delays are short compared to the input signal time scale.

a) Sketch the waveforms that appear at the Q_M and Q_S outputs of the master and slave latches. Assume that the flip-flop is initially in the reset state.

b) Do the waveforms exhibit any 1's catching behavior?

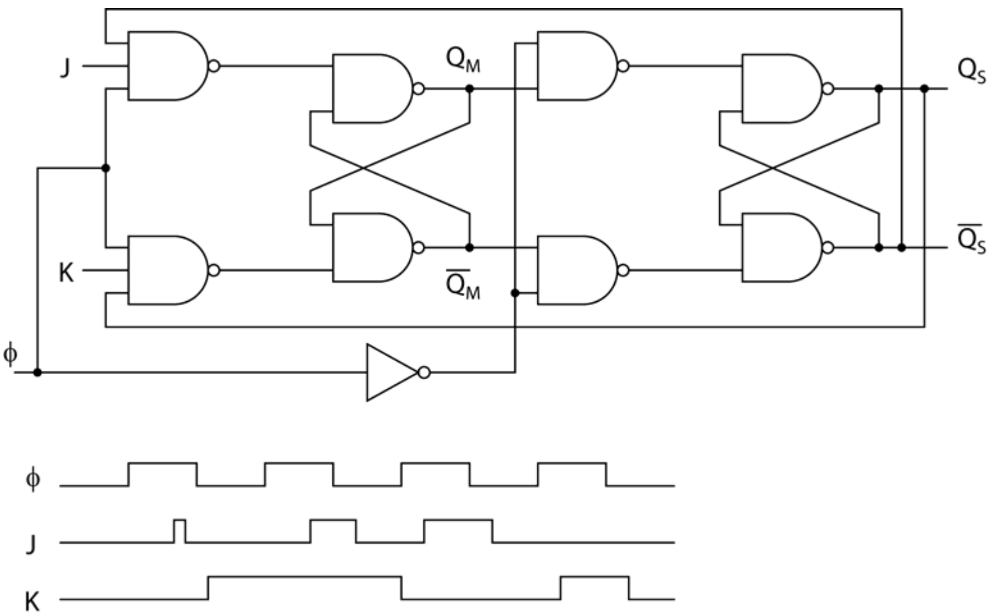


Figure 7.1. JK master-slave flip-flop.

7.2) Consider dynamic implementations of the D flip-flop using either the C^2MOS approach of Figure 7-26 or the TSPC approach of Figure 7-33. The flip-flops are driven by clocks CLK and CLK with a 50% duty cycle.

a) Discuss the impact of clock overlap on the behavior of both flip-flops.

b) Discuss the impact of finite clock rise and fall times on the behavior of both flip-flops.

7.3) Design a pipelined circuit of the function F= (AB+BC)+D. Use C^2MOS latches for the implementation.

a) Draw the schematics of the circuit assuming you are allowed to introduce two pipeline stages between input and output. Try both static and dynamic implementations of the logic. Place the latches so that a maximum clock speed is obtained. What limits clock speed in both cases?

7.4) A five-stage ring oscillator is selected for the implementation of a VCO. The oscillation frequency should be 5MHz for a supply voltage of 3.3V. The basic inverter circuit used in the oscillator is shown in Fig. 7.2. Due to their large sizes, you may consider transistors M2 and M3 to be ideal switches (with zero on-resistance).

a) Determine the DC-voltages needed at nodes H and L to get the required oscillation frequency. Consider only the capacitance shown in the figure. Ignore the channel length modulation factor. Also make sure that rise and fall times are identical. Use the following transistor parameters:

k_n'=19.6 μA/V^2, k_p'=5.4 μA/V^2, V_{tn}=0.743 V, V_{tp}=–0.739 V
L=0.9 μm, W_1=5 μm, W_2=100 μm, W_3=300 μm, W_2=10 μm

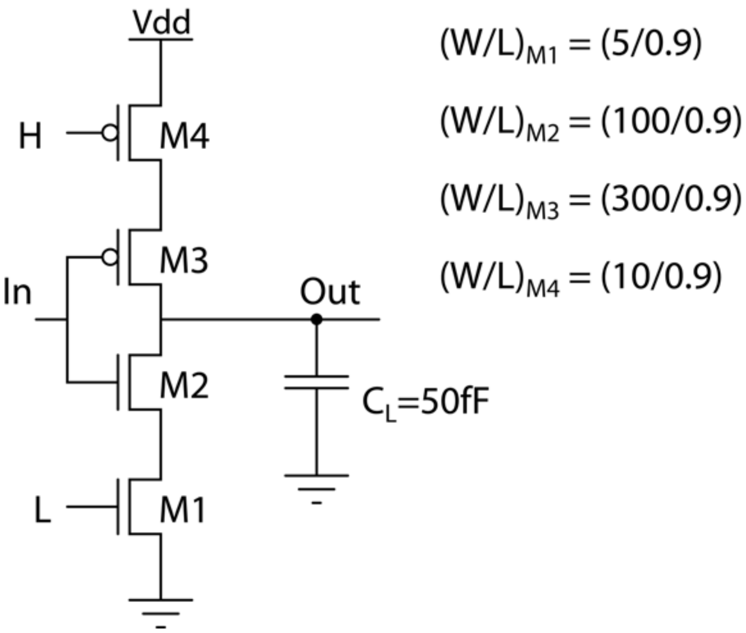


Figure 7.2. Current-starved inverter used in the oscillator.

7.5) Design a finite state machine with the use of registers, multiplexers, inverters, AND-gates and OR-gates, fulfilling the graph shown in Figure 7-3.

Data inputs: *a*, *b*, *c*
Data output: *y*

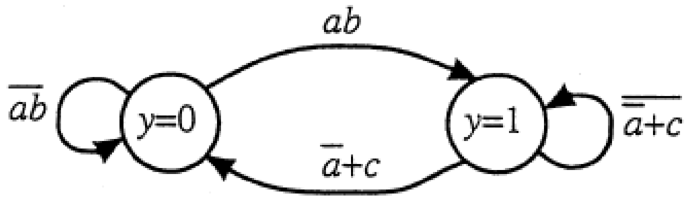


Figure 7-3. A finite state machine

7.6) Design a finite state machine with the use of registers, multiplexers, inverters, AND-gates and OR-gates, fulfilling the graph shown in Figure .
Data inputs: a, b, c
Data output: y (y0y1)

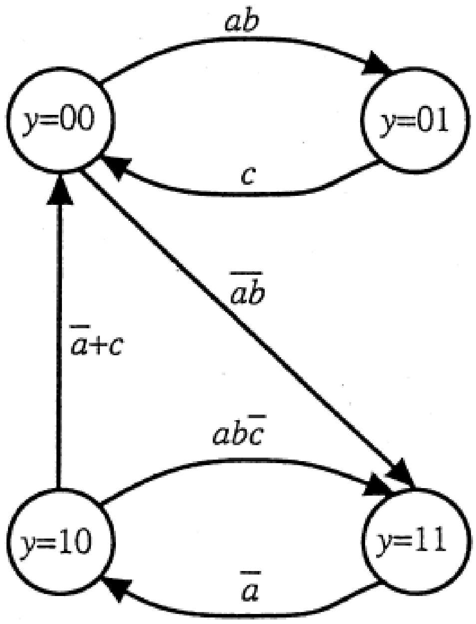
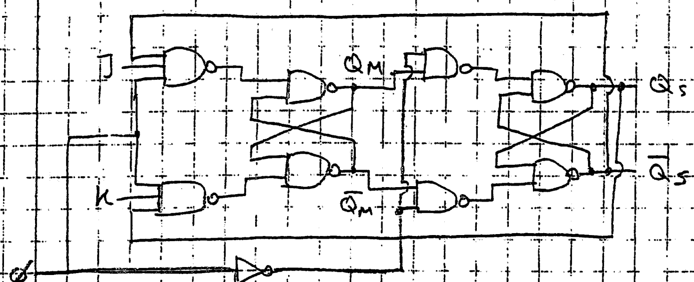


Figure 7-4. A finite state machine

7.1 The indicated waveforms are applied to the JK master-slave flip-flop of figure X7-1. For this problem, assume the gate delays are short compared to the input signal time scale.

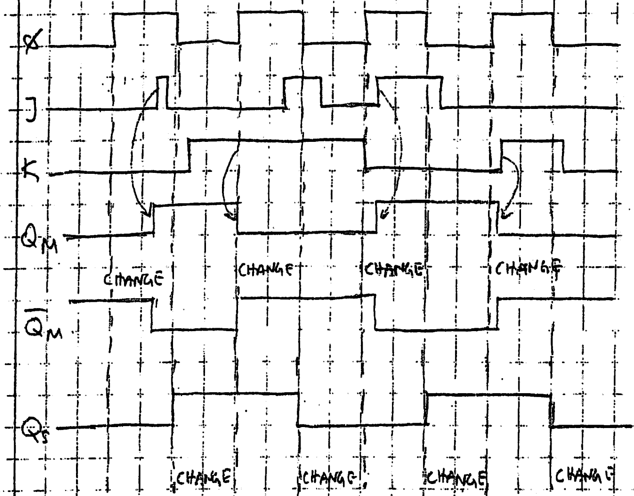


$\phi_M \leftrightarrow$ Pos. flank ϕ

$\phi_s \leftrightarrow$ Neg. flank ϕ

a) Sketch the waveforms that appear at the Q_M and Q_s outputs of the master and slave latches. Assume that the flip-flop is initially in a reset state.

HINT: Set initial states at all nodes. Change the input signals according to the given figure and see what happens at nodes Q_M, $\overline{Q}_M$, Q_s, $\overline{Q}_s$.



b) Do the waveforms exhibit any 1's catching behavior?

YES, the J = 1 glitch is caught:

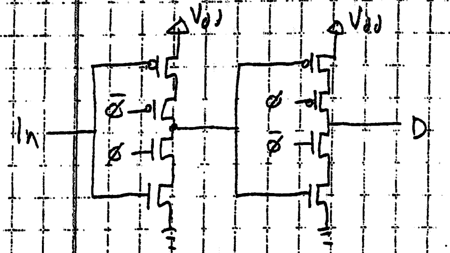
Q_M is set eventhough J returns to zero before the end of the ϕ-cycle.

Hint! JK-flip flop is reset when we start.

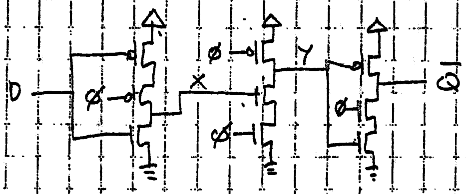
→ $Q_s = 0$

→ $\overline{Q}_s = 1$

(7.2) Consider dynamic implementations of the D flip-flop using either the C^2MOS approach of figure 7-26 or the TSPC approach of figure 7-33. The flip-flops are driven by clocks ϕ and $\bar{\phi}$ with a 50% duty cycle.



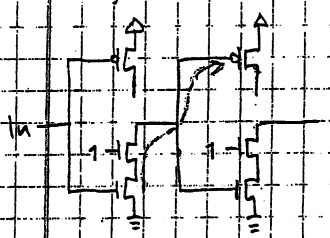
C^2MOS master-slave D flip-flop (Fig 7-26)



Positive edge-triggered D flip-flop (Fig 7-33)

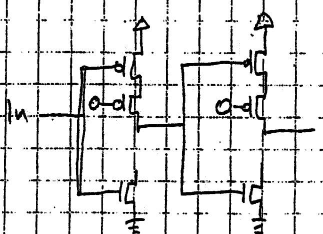
a) Discuss the impact of clock overlap on the behavior of both flip-flops.

Fig 7-26



(1-1) overlap

- A race through the circuit is not possible, since only PDN-networks are active



(0-0) overlap

- A race through the circuit is not possible, since only PUN-networks are active.

Fig 7-33

Race is not possible. Only PUN or PDN are activated, but never simultaneously.

b) Discuss the impact of finite clock rise and fall times on the behavior of both flip-flops.

For sufficiently slow rise/fall times, both n- and p-channel devices can conduct simultaneously. ∴ Race is possible.

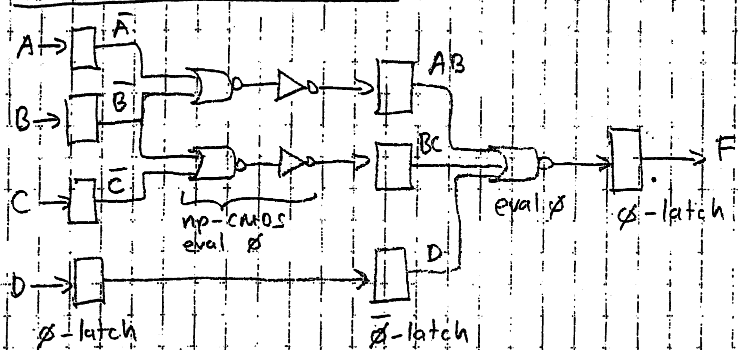
(7.3) Design a pipelined circuit of the function $F = (AB + BC) + D$.
Use C^2MOS-latches for the implementation.

a) Draw the schematics of the circuit assuming you are allowed to introduce two pipeline stages between input and output.
Try both static and dynamic implementations of the logic.
Place the latches so that a maximum clock speed is obtained.
What limits clock speed in both cases?

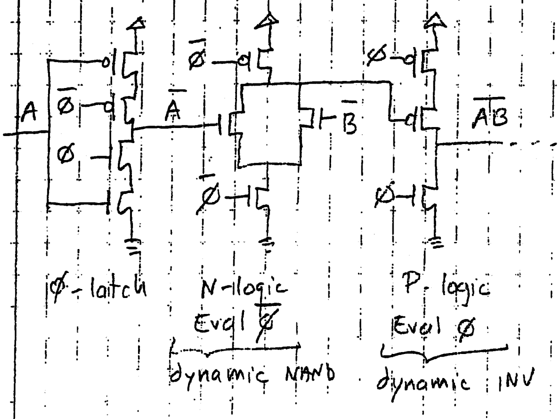
C^2MOS latches INVERT data; rearrange the function to prepare for this

$F = AB + BC + D = \overline{\overline{AB} \cdot \overline{BC} \cdot \overline{D}}$

* DYNAMIC IMPLEMENTATION



PARTIAL CIRCUITRY



f_{CLK} is limited by 3input NOR and delay through a register.

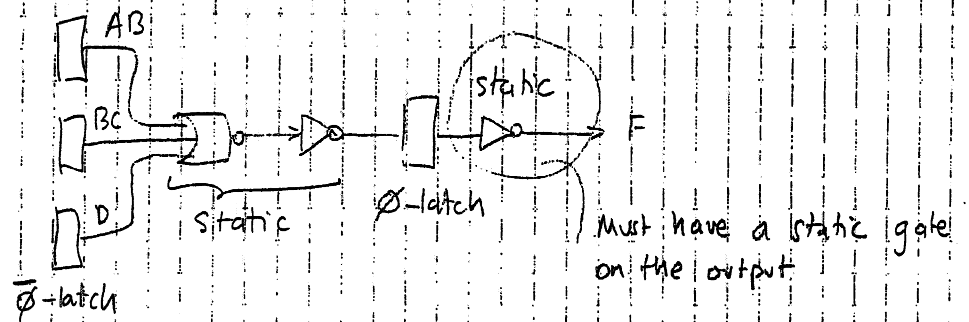
7.3

continued...

a)

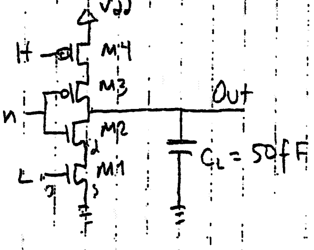
* STATIC IMPLEMENTATION

To avoid race, only non-inverting logic can be placed between registers. Up to the second pipeline, registers are the same. However:



f_{clk} is limited by 3-input NOR, inverter and register.

7.4 A five-stage ring oscillator is selected for the implementation of a VCO. The oscillation frequency should be 5 MHz for a supply voltage of 3,3V. The basic inverter circuit used in the oscillator is shown in figure 6.61. Due to their large sizes, you may consider transistors M2 and M3 to be ideal switches (with zero on-resistance)



$(W/L)_{M1} = (5/1,2)$
$(W/L)_{M2} = (100/1,2)$
$(W/L)_{M3} = (300/1,2)$
$(W/L)_{M4} = (10/1,2)$

a) Determine the DC-voltages needed at nodes H and L to get the required oscillation frequency. Consider only the capacitance in the figure. Ignore the channel length modulation factor. Also make sure the rise and fall times are equal.

For a ring oscillator we have the oscillation period:

$T = 2 \cdot t_p \cdot N$
N = Number of inverters

$$\frac{1}{f} = 2\, t_p \cdot N \qquad t_p = \frac{1}{2 \cdot N \cdot f} = \frac{1}{2 \cdot 5 \cdot 5 \cdot 10^6} = 20\,ns \quad (= t_{pLH} = t_{pHL})$$

$$\left[\, C = \frac{Q}{V} \;;\; I = \frac{Q}{t} \;;\; I = \frac{C \cdot V}{t} \,\right]$$

$$I_{avg} = \frac{C_L \cdot \Delta V}{t_p} \quad \text{where} \quad \begin{aligned} \Delta V &= V_{DD} - V_M = 1,65V, \text{ for } t_{pHL} \\ \Delta V &= V_M - 0 = 1,65V, \text{ for } t_{pLH} \end{aligned}$$

$$I_{avg} = \frac{50 \cdot 10^{-15} \cdot 1,65}{20 \cdot 10^{-9}} = 4,125\,\mu A$$

Assume both M1 and M4 are saturated.

Transistor parameters from pp. 62

$k_n' = 19,6\,\mu A/V^2$ ‖ $k_p' = 5,4\,\mu A/V^2$ ‖ $L_{eff} = 0,9\,\mu m$
$V_{Tn} = 0,743V$ ‖ $V_{Tp} = 0,739V$

* Study M1:

$$I_{avg} = I_{sat} = \frac{k_n'}{2}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{Tn})^2 \iff V_{GS} = \sqrt{\frac{2\, I_{sat}}{k_n'\left(\frac{W}{L_{eff}}\right)}} + V_{Tn}$$

$$\Rightarrow V_L = \sqrt{\frac{2 \cdot (4,125 \cdot 10^{-6})}{19,6 \cdot 10^{-6}\left(\frac{5}{0,9}\right)}} + 0,743 = 1,01825\ldots \approx \underline{\underline{1,02\,V}}$$

Check if M1 was saturated:

$V_{DS} > V_{GS} - V_{Tn}$; $V_D > V_G - V_{Tn}$; $V_D > 1,02 - 0,743 = 0,259$. (saturated most of the time)

7.4

continued...

* Study M4

$$I_{sat} = \frac{k_p'}{2}\left(\frac{W}{L_{eff}}\right)(V_{SG} - |V_{Tp}|)^2$$

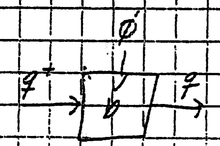
$$\sqrt{\frac{2 I_{sat}}{k_p'\left(\frac{W}{L_{eff}}\right)}} + |V_{Tp}| = V_S - V_G$$

$$V_G = V_S - |V_{Tp}| - \sqrt{\frac{2 I_{sat}}{k_p'\left(\frac{W}{L_{eff}}\right)}}$$

$$\Rightarrow V_{H} = 3{,}3 - 0{,}739 - \sqrt{\frac{2\,(4{,}125 \cdot 10^{-6})}{5{,}4 \cdot 10^{-6}\left(\frac{10}{0{,}9}\right)}} = 2{,}19019\ldots \approx \underline{\underline{2{,}19\text{ V}}}$$

7.5

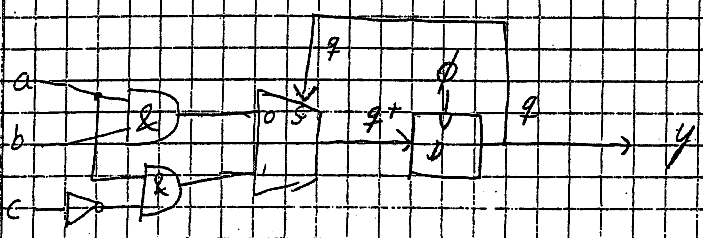
Let the current state be denoted q and the next state denoted q^+.



We choose to use the output of the register as data output y.

$q = 0 \Rightarrow q^+ = ab$

$q = 1 \Rightarrow q^+ = \overline{\bar{a} + c} = a\bar{c}$



(7.6) Use the output from the registers as data output.

q_0 q_1	q_0^+	q_1^+
0 0	$\overline{ab}$	1
0 1	0	$\overline{c}$
1 0	$\overline{\overline{a}+c}$	$ab\overline{c}$
1 1	1	a

$$q_0^+ = \overline{q_0}\,\overline{q_1}\,\overline{ab} + \overline{q_0}q_1\cdot 0 + q_0\overline{q_1}\,a\overline{c} + q_0 q_1$$

$$q_1^+ = \overline{q_0}\,\overline{q_1} + \overline{q_0}\,q_1\overline{c} + q_0\overline{q_1}\,ab\overline{c} + q_0 q_1 a$$