Lesson 1

Chapter 3
PROBLEMS

For all problems, use the device parameters provided in Chapter 3 (Tables 3.2 and 3.5) and the inside back book cover, unless otherwise mentioned. Also assume T = 300 K by default.

1. [E,SPICE,3.2.2]
   a. Consider the circuit of Figure 0.1. Using the simple model, with V_{Don} = 0.7 V, solve for I_D.
   b. Find I_D and V_D using the ideal diode equation. Use $I_s = 10^{-14}$ A and T = 300 K.
   c. Solve for V_{D1}, V_{D2}, and I_D using SPICE.
   d. Repeat parts *b* and *c* using $I_S = 10^{-16}$ A, T = 300K, and $I_S = 10^{-14}$A, T = 350 K.

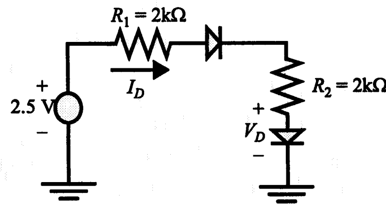


Figure 0.1 Resistor diode circuit.

2. [M, None, 3.2.3] For the circuit in Figure 0.2, V_s = 3.3 V. Assume A_D = 12 μm², ϕ_0 = 0.65 V, and m = 0.5. N_A = 2.5 E16 and N_D = 5 E15.
   a. Find I_D and V_D.
   b. Is the diode forward- or reverse-biased?
   c. Find the depletion region width, W_j, of the diode.
   d. Use the parallel-plate model to find the junction capacitance, C_j.
   e. Set V_s = 1.5 V. Again using the parallel-plate model, explain qualitatively why C_j increases.

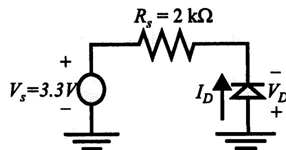


Figure 0.2 Series diode circuit

3. [E, None, 3.3.2] Figure 0.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current I_D for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: k_n' = 115μA/V², V_{T0} = 0.43 V, λ = 0.06 V⁻¹, PMOS: k_p' = 30 μA/V², V_{T0} = −0.4 V, λ = -0.1 V⁻¹. Assume (W/L) = 1. Assume $V_{DSAT,n}$=0.63V, $V_{DSAT,p}$=1.0V.
   a. NMOS: V_{GS} = 2.5 V, V_{DS} = 2.5 V. PMOS: V_{GS} = −0.5 V, V_{DS} = −1.25 V.
   b. NMOS: V_{GS} = 3.3 V, V_{DS} = 2.2 V. PMOS: V_{GS} = −2.5 V, V_{DS} = −1.8 V.
   c. NMOS: V_{GS} = 0.6 V, V_{DS} = 0.1 V. PMOS: V_{GS} = −2.5 V, V_{DS} = −0.7 V.
4. [E, SPICE, 3.3.2] Using SPICE plot the *I-V* characteristics for the following devices.

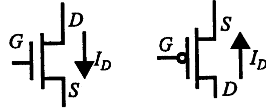


Figure 0.3 NMOS and PMOS devices.

a. NMOS $W = 1.2\mu m$, $L = 0.25\mu m$
b. NMOS $W = 4.8\mu m$, $L = 0.5\mu m$
c. PMOS $W = 1.2\ \mu m$, $L = 0.25\ \mu m$
d. PMOS $W = 4.8\ \mu m$, $L = 0.5\ \mu m$

5. [E, SPICE, 3.3.2] Indicate on the plots from problem 4.
a. the regions of operation.
b. the effects of channel length modulation.
c. Which of the devices are in velocity saturation? Explain how this can be observed on the *I-V* plots.

6. [M, None, 3.3.2] Given the data in Table 0.1 for a short channel NMOS transistor with $V_{DSAT} = 0.6\ V$ and $k' = 100\ \mu A/V^2$, calculate V_{T0}, γ, λ, $2|\phi_f|$, and W/L:

Table 0.1 Measured NMOS transistor data

	V_{GS}	V_{DS}	V_{BS}	I_D (µA)
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	–1	1146
5	2	1.8	-2	1039

7. [E, None, 3.3.2] Given Table 0.2 ,the goal is to derive the important device parameters from these data points. As the measured transistor is processed in a deep-submciron technology, the '**unified model**' holds. From the material constants, we also could determine that the saturation voltage V_{DSAT} equals -1V. You may also assume that $-2\Phi_F = -0.6V$.

NOTE: The parameter values on Table 3.3 do NOT hold for this problem.
a. Is the measured transistor a PMOS or an NMOS device? Explain your answer.
b. Determine the value of V_{T0}.
c. Determine γ.
d. Determine λ.

e. Given the obtained answers, determine for each of the measurements the operation region of the transistor (choose from *cutoff, resistive, saturated, and velocity saturated*). Annotate your finding in the right-most column of the above.

Table 0.2 Measurements taken from the MOS device, at different terminal voltages.

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (μA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	
5	-2.5	-2.5	-1	-72.0	
6	-2.5	-1.5	0	-80.625	
7	-2.5	-0.8	0	-66.56	

8. [M, None, 3.3.2] An NMOS device is plugged into the test configuration shown below in Figure 0.4. The input V_{in} =2V. The current source draws a constant current of 50 μA. *R* is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110*10^{-6}$ V/A^2, $V_T = 0.4$, and $V_{DSAT} = 0.6$V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and channel length modulation can be neglected. i.e λ=0, γ=0. .

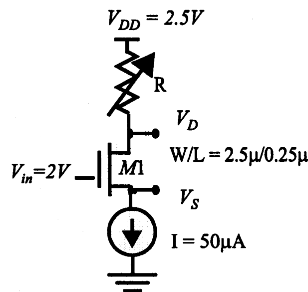


Figure 0.4 Test configuration for the NMOS device.

a. When *R* =10kΩ find the operation region, V_D and V_S.

b. When R= 30kΩ again determine the operation region V_D, V_S

c. For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively

9. [M, None, 3.3.2] Consider the circuit configuration of Figure 0.5.

a. Write down the equations (and only those) which are needed to determine the voltage at node X. Do NOT plug in any values yet. Neglect short channel effects and assume that $\lambda_p = 0$.

b. Draw the (approximative) load lines for both MOS transistor and resistor. Mark some of the significant points.

c. Determine the required width of the transistor (for $L = 0.25\mu m$) such that X equals 1.5 V.

d. We have, so far, assumed that M_1 is a long-channel device. Redraw the load lines assuming that M_1 is velocity-saturated. Will the voltage at X rise or fall?

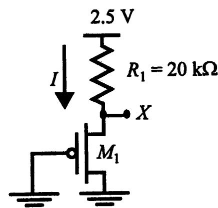


Figure 0.5 MOS circuit.

10. [M, None, 3.3.2] The circuit of Figure 0.6 is known as a *source-follower* configuration. It achieves a DC level shift between the input and output. The value of this shift is determined by the current I_0. Assume $\gamma = 0.4$, $2|\phi_f| = 0.6$ V, $V_{T0} = 0.43$ V, $k' = 115$ $\mu A/V^2$, and $\lambda = 0$. The NMOS device has W/L = 5.4μ/1.2μ such that the short channel effects are not observed.

a. Derive an expression giving V_i as a function of V_o and $V_T(V_o)$. If we neglect body effect, what is the nominal value of the level shift performed by this circuit.

b. The NMOS transistor experiences a shift in V_T due to the body effect. Find V_T as a function of V_o for V_o ranging from 0 to 1.5V with 0.25 V intervals. Plot V_T vs. V_o.

c. Plot V_o vs. V_i as V_o varies from 0 to 1.5 V with 0.25 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter? At V_o (body effect) = 1.5 V, find V_o (ideal) and, thus, determine the maximum error introduced by body effect.

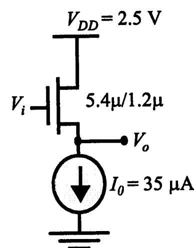


Figure 0.6 Source-follower level converter.

11. [M, SPICE, 3.3.2] Problem 11 uses the MOS circuit of Figure 0.7.

a. Plot V_{out} vs. V_{in} with V_{in} varying from 0 to 2.5 volts (use steps of 0.5V). $V_{DD} = 2.5$ V.

b. Repeat *a* using SPICE.

c. Repeat *a* and *b* using a MOS transistor with $(W/L) = 4/1$. Is the discrepancy between manual and computer analysis larger or smaller. Explain why.

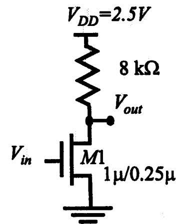


Figure 0.7 MOS circuit.

12. [E, None, 3.3.2]Below in Figure 0.8 is an I-V transfer curve for an NMOS transistor. In this problem, the objective is to use this I-V curve to obtain information about the transistor. The transistor has $(W/L)=(1\mu/1\mu)$. It may also be assumed that velocity saturation does not play a role in this example. Also assume $-2\Phi_F = 0.6V$. Using Figure 0.8 determine the following parameters: device V_{TO}, γ, λ.

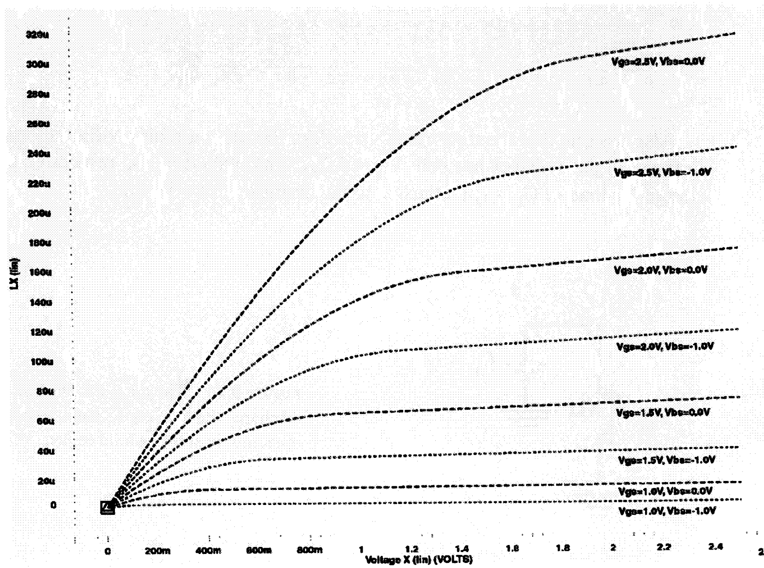


Figure 0.8 I-V curves

13. [E, None , 3.3.2]The curves below in Figure 0.9 represent the gate voltage(V_{GS}) vs. drain current (I_{DS}) of two NMOS devices which are on the same die and operate in subthreshold region. Due to process variations on the same die the curves do not overlap.

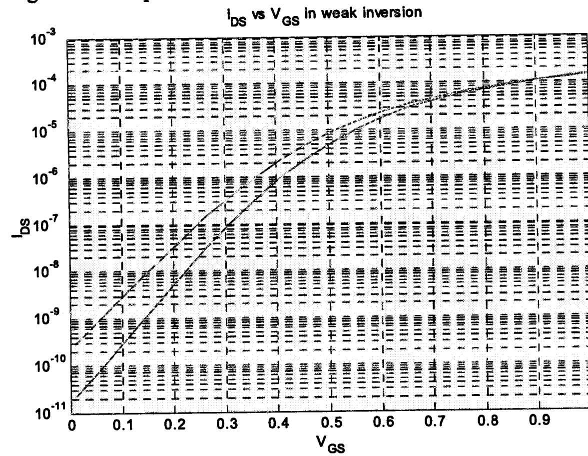


Figure 0.9 Subthreshold current curves. Difference is due to process variations

Also assume that the transistors are within the same circuit configurations as Figure 0.10 in If the in put voltages are both V_{in} = 0.2V. What would be the respective durations to discharge the load of C_L = 1pF attached to the drains of these devices.

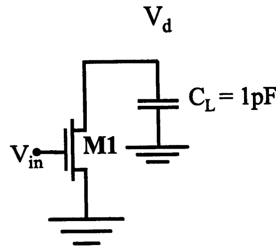


Figure 0.10 The circuit for testing the time to discharge the load capacitance through a device operating in subthreshold region.

14. [M, None, 3.3.2] Short-channel effects:

a. Use the fact that current can be expressed as the product of the carrier charge per unit length and the velocity of carriers ($I_{DS} = Qv$) to derive I_{DS} as a function of W, C_{ox}, $V_{GS} - V_T$, and carrier velocity v.

b. For a long-channel device, the carrier velocity is the mobility times the applied electric field. The electrical field, which has dimensions of V/m, is simply $(V_{GS} - V_T) / 2L$. Derive I_{DS} for a long-channel device.

c. From the equation derived in *a*, find I_{DS} for a short-channel device in terms of the maximum carrier velocity, v_{max}.

Based on the results of *b* and *c* describe the most important differences between short-channel and long-channel devices.

15. [C, None, 3.3.2] Another equation, which models the velocity-saturated drain current of an MOS transistor is given by

$$I_{dsat} = \frac{1}{1+(V_{GS}-V_t)/(E_{sat}L)}\left(\frac{\mu_0 C_{ox}}{2}\right)\frac{W}{L}(V_{GS}-V_T)^2$$

Using this equation it is possible to see that velocity saturation can be modeled by a MOS device with a source-degeneration resistor (see Figure 0.11).

a. Find the value of R_S such that $I_{DSAT}(V_{GS}, V_{DS})$ for the composite transistor in the figure matches the above velocity-saturated drain current equation. *Hint: the voltage drop across R_S is typically small.*

b. Given E_{sat} = 1.5 V/μm and $k' = \mu_0 C_{ox}$ = 20 μA/V^2, what value of R_S is required to model velocity saturation. How does this value depend on W and L?

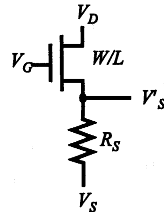


Figure 0.11 Source-degeneration model of velocity saturation.

16. [E, None, 3.3.2] The equivalent resistances of two different devices need to be computed.

a. First, consider the fictive device whose I-V characteristic is given in Figure 0.12. Constant k has the dimension of S (or1/Ω). V_0 is a voltage characteristic to the device. Calculate the equivalent resistance for an output voltage transition from 0 to $2V_0$ by integrating the resistance as a function of the voltage.

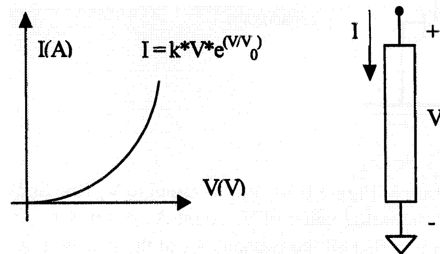


Figure 0.12 Fictive device whose equivalent resistance is to be calculated.

b. Next, obtain the resistance equation 3.43 using the Figure 0.13. Assuming the V_{GS} is kept at V_{DD}, Calculate the Req as output (V_{DS}) transitions from V_{DD} to $V_{DD}/2$.(Figure 0.13).

Hint: Make sure you use the Short channel Unified MOS Model equations. **Hint:** You will need to use the expansion. $ln(1+x) \approx x - x^2/2 + x^3/3$

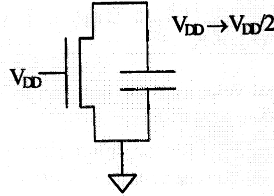


Figure 0.13 The equivalent resistance is to be computed for the H→L transition.

17. [M, None, 3.3.3] Compute the gate and diffusion capacitances for transistor *M1* of Figure 0.7. Assume that drain and source areas are rectangular, and are 1 μm wide and 0.5 μm long. Use the parameters of Example 3.5 to determine the capacitance values. Assume $m_j = 0.5$ and $m_{jsw} = 0.44$. Also compute the total charge stored at node *In*, for the following initial conditions:

a. $V_{in} = 2.5$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

b. $V_{in} = 0$ V, $V_{out} = 2.5$ V, 0.5 V, and 0 V.

18. [E, None, 3.3.3]Consider a CMOS process with the following capacitive parameters for the NMOS transistor: C_{GSO}, C_{GDO}, C_{OX}, C_J, m_j, C_{jsw}, m_{jsw}, and PB, with the lateral diffusion equal to L_D. The MOS transistor M1 is characterized by the following parameters: W, L, AD, PD, AS, PS.

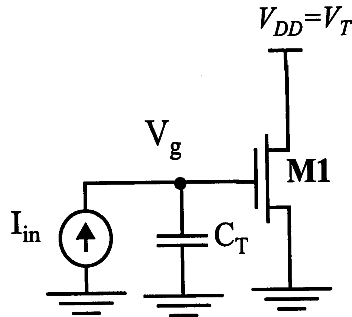


Figure 0.14 Circuit to measure total input capacitance

a. Consider the configuration of Figure 0.14. V_{DD} is equal to V_T (the threshold voltage of the transistor) Assume that the initial value of V_g equals 0. A current source with value I_{in} is applied at time 0. Assuming that all the capacitance at the gate node can be lumped into a single, grounded, linear capacitance C_T, derive an expression for the time it will take for V_g to reach 2 V_T

b. The obvious question is now how to compute C_T. Among, C_{db}, C_{sb}, C_{gs}, C_{gd}, C_{gb} which of these parasatic capacitances of the MOS transistor contribute to C_T. For those that contribute to C_T write down the expression that determines the value of the contribution. Use only the parameters given above. If the transistor goes through different operation regions and this impacts the value of the capacitor, **determine the expression of the contribution for each region (and indicate the region).**

3.3

NMOS: $\begin{Bmatrix} k_n^{'} = 115\mu A/V^2 \\ V_{t0n} = 0.43V \\ \lambda_n = 0.06V^{-1} \\ V_{DSATn} = 0.63V \end{Bmatrix}$ PMOS: $\begin{Bmatrix} k_p^{'} = -30\mu A/V^2 \\ V_{t0p} = -0.4V \\ \lambda_p = -0.1V^{-1} \\ V_{DSATp} = -1.0V \end{Bmatrix}$

Assume no body effect $\Rightarrow \begin{Bmatrix} V_{Tn} = V_{T0n} \\ V_{Tp} = V_{T0p} \end{Bmatrix}$

L = 0.25μm , $\frac{W}{L} = 1$

a) NMOS

$V_{gs} = 2.5V$, $V_{ds} = 2.5V$

$V_{gt} = V_{gs} - V_T = 2.5 - 0.43 = 2.07V$, $V_{gt} \geq 0 \Rightarrow$ Transistor is on

$V_{\min} = \left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(2.07, 2.5, 0.63) = 0.63V$

$V_{\min} = V_{DSAT} \Rightarrow$ NMOS region of operation is: **Velocity Saturation**

$$I_d = k_n^{'}\frac{W}{L}V_{\min}\left(\left|V_{gt}\right| - \frac{V_{\min}}{2}\right)(1 + \lambda V_{ds})$$

$$I_d = 115 \cdot 10^{-6} \cdot 1 \cdot 0.63\left(2.07 - \frac{0.63}{2}\right)(1 + 0.06 \cdot 2.5) = 146\mu A$$

PMOS

$V_{gs} = -0.5V$, $V_{ds} = -1.25V$

$V_{gt} = V_{gs} - V_T = -0.5 - (-0.4) = -0.1V$, $V_{gt} \leq 0 \Rightarrow$ Transistor is on

$V_{\min} = \min\left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(0.1, 1.25, 1.0) = 0.1V$

$V_{\min} = \left|V_{gt}\right| \Rightarrow$ PMOS region of operation is: **Saturation**

$$I_d = k_n^{'}\frac{W}{L}V_{\min}\left(\left|V_{gt}\right| - \frac{V_{\min}}{2}\right)(1 + \lambda V_{ds})$$

$$I_d = -30 \cdot 10^{-6} \cdot 1 \cdot 0.1\left(0.1 - \frac{0.1}{2}\right)(1 + (-0.1) \cdot (-1.25)) = -169nA$$

b) NMOS

$V_{gs} = 3.3V$, $V_{ds} = 2.2V$

$V_{gt} = V_{gs} - V_T = 3.3 - 0.43 = 2.87V$, $V_{gt} \geq 0 \Rightarrow$ Transistor is on

$V_{\min} = \left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(2.87, 2.2, 0.63) = 0.63V$

$V_{\min} = V_{DSAT} \Rightarrow$ NMOS region of operation is: **Velocity Saturation**

$$I_d = k_n' \frac{W}{L} V_{\min} \left(\left|V_{gt}\right| - \frac{V_{\min}}{2} \right) (1 + \lambda V_{ds})$$

$$I_d = 115 \cdot 10^{-6} \cdot 1 \cdot 0.63 \left(2.87 - \frac{0.63}{2} \right) (1 + 0.06 \cdot 2.2) = 210 \mu A$$

PMOS

$V_{gs} = -2.5V$, $V_{ds} = -1.8V$

$V_{gt} = V_{gs} - V_T = -2.5 - (-0.4) = -2.1V$, $V_{gt} \leq 0 \Rightarrow$ Transistor is on

$V_{\min} = \min\left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(2.1, 1.8, 1.0) = 1.0V$

$V_{\min} = \left|V_{DSAT}\right| \Rightarrow$ PMOS region of operation is: **Velocity Saturation**

$$I_d = k_n' \frac{W}{L} V_{\min} \left(\left|V_{gt}\right| - \frac{V_{\min}}{2} \right) (1 + \lambda V_{ds})$$

$$I_d = -30 \cdot 10^{-6} \cdot 1 \cdot 1.0 \left(2.1 - \frac{1.0}{2} \right) (1 + (-0.1) \cdot (-1.8)) = -56.5 \mu A$$

c) NMOS

$V_{gs} = 0.6V$, $V_{ds} = 0.1V$

$V_{gt} = V_{gs} - V_T = 0.6 - 0.43 = 0.17V$, $V_{gt} \geq 0 \Rightarrow$ Transistor is on

$V_{\min} = \left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(0.17, 0.1, 0.63) = 0.1V$

$V_{\min} = V_{ds} \Rightarrow$ NMOS region of operation is: **Linear**

$$I_d = k_n' \frac{W}{L} V_{\min} \left(\left|V_{gt}\right| - \frac{V_{\min}}{2} \right) (1 + \lambda V_{ds})$$

$$I_d = 115 \cdot 10^{-6} \cdot 1 \cdot 0.1 \left(0.17 - \frac{0.1}{2} \right) (1 + 0.06 \cdot 0.1) = 1.39 \mu A$$

PMOS

$V_{gs} = -2.5V$, $V_{ds} = -0.7V$

$V_{gt} = V_{gs} - V_T = -2.5 - (-0.4) = -2.1V$, $V_{gt} \leq 0 \Rightarrow$ Transistor is on

$V_{\min} = \min\left(\left|V_{gt}\right|, \left|V_{ds}\right|, \left|V_{DSAT}\right|\right) = \min(2.1, 0.7, 1.0) = 0.7V$

$V_{\min} = \left|V_{ds}\right| \Rightarrow$ PMOS region of operation is: **Linear**

$$I_d = k_n' \frac{W}{L} V_{\min} \left(\left|V_{gt}\right| - \frac{V_{\min}}{2} \right) (1 + \lambda V_{ds})$$

$$I_d = -30 \cdot 10^{-6} \cdot 1 \cdot 0.7 \left(2.1 - \frac{0.7}{2} \right) (1 + (-0.1) \cdot (-0.7)) = -39.3 \mu A$$

3.6

Given the data in table 0.1 for a short channel NMOS transistor with $V_{DSAT} = 0.6V$, $k' = 100\mu A/V^2$, calculate V_{T0}, λ, γ, $2|\phi_F|$ and $\frac{W}{L}$

Eq	V_{gs}	V_{ds}	V_{bs}	$I_d[\mu A]$
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	-1	1146
5	2	1.8	-2	1039

Unified MOS model:

$$I_d = k_n' \frac{W}{L}\left((V_{gs} - V_T)V_{\min} - \frac{V_{\min}^2}{2}\right)(1 + \lambda V_{ds})$$
$$V_{\min} = \min((V_{gs} - V_T), V_{ds}, V_{DSAT})$$

- First, determine the region of operation
- To have a transistor in saturation region for any of these given data, V_T should be:

$V_{DSAT} > V_{gs} - V_T \quad \Rightarrow \quad V_T > V_{gs} - V_{DSAT} \quad \Rightarrow \quad V_T > 2.0 - 0.6 \quad \Rightarrow \quad V_T > 1.4$

For this process a threshold voltage of > 1.4V is high so we can assume that all data are taken in velocity saturation. We can always assume a region of operation as long as it is verified afterwards. (Note here that Eq.1 sets an even higher constraint on V_T)

Use Eq.1 & Eq.2 to find V_{T0}:

$$V_{\min} = V_{DSAT} = 0.6V$$
$$\left\{\begin{array}{l} I_{d,1} = k_n' \frac{W}{L}\left((2.5 - V_{T0})0.6 - \frac{0.6^2}{2}\right)(1 + \lambda 1.8) = 1812 \\ I_{d,2} = k_n' \frac{W}{L}\left((2.0 - V_{T0})0.6 - \frac{0.6^2}{2}\right)(1 + \lambda 1.8) = 1297 \end{array}\right\} \Rightarrow \frac{1812}{1297} = \frac{(2.5 - V_{T0})0.6 - \frac{0.6^2}{2}}{(2.0 - V_{T0})0.6 - \frac{0.6^2}{2}}$$

$$\Rightarrow \frac{1812(2.0 - V_{T0})0.6}{1297} - \frac{1812\frac{0.6^2}{2}}{1297} = (2.5 - V_{T0})0.6 - \frac{0.6^2}{2}$$
$$\Rightarrow \frac{1812 \cdot 0.6 \cdot 2.0}{1297} - \frac{1812 \cdot 0.6 \cdot V_{T0}}{1297} - \frac{1812 \cdot 0.6^2}{2 \cdot 1297} = 2.5 \cdot 0.6 - 0.6 \cdot V_{T0} - \frac{0.6^2}{2}$$
$$\Rightarrow 0.105011 = 0.238242 V_{T0}$$
$$\Rightarrow V_{T0} \approx 0.44V$$

Check our assumption that the transistor was in velocity saturation:

$V_{T0} = 0.44 < V_T < 1.4$ so in equations 1,2 and 3 the transistor is in velocity saturation.

Use Eq.2 and Eq.3 to find λ

$$\begin{cases} I_{d,2} = k_n' \frac{W}{L}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)(1+\lambda 1.8) = 1297 \\ I_{d,3} = k_n' \frac{W}{L}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)(1+\lambda 2.5) = 1361 \end{cases} \Rightarrow \frac{1297}{1361} = \frac{(1+\lambda 1.8)}{(1+\lambda 2.5)}$$

$$\Rightarrow 1297(1+\lambda 2.5) = 1361(1+\lambda 1.8) \Rightarrow 792.7\lambda = 64$$

$$\Rightarrow \lambda \approx 0.08V^{-1}$$

To find V_T for Eq.4 and Eq.5, use Eq.2 as reference:

Eq.2 and Eq.4

$$\begin{cases} I_{d,2} = k_n' \frac{W}{L}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)(1+0.08\cdot 1.8) = 1297 \\ I_{d,4} = k_n' \frac{W}{L}\left((2.0-V_{T,4})0.6 - \frac{0.6^2}{2}\right)(1+0.08\cdot 1.8) = 1146 \end{cases} \Rightarrow \frac{1297}{1146} = \frac{(2.0-0.44)0.6 - \frac{0.6^2}{2}}{(2.0-V_{T,4})0.6 - \frac{0.6^2}{2}}$$

$$\Rightarrow \left((2.0-V_{T,4})0.6 - \frac{0.6^2}{2}\right) = \frac{1146}{1297}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)$$

$$\Rightarrow V_{T,4} = 2.0 - \frac{\frac{1146}{1297}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right) - \frac{0.6^2}{2}}{0.6}$$

$$\Rightarrow V_{T,4} \approx 0.587V$$

Eq.2 and Eq.5

$$\begin{cases} I_{d,2} = k_n' \frac{W}{L}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)(1+0.08\cdot 1.8) = 1297 \\ I_{d,5} = k_n' \frac{W}{L}\left((2.0-V_{T,5})0.6 - \frac{0.6^2}{2}\right)(1+0.08\cdot 1.8) = 1039 \end{cases} \Rightarrow \frac{1297}{1039} = \frac{(2.0-0.44)0.6 - \frac{0.6^2}{2}}{(2.0-V_{T,5})0.6 - \frac{0.6^2}{2}}$$

$$\Rightarrow (2.0-V_{T,5})0.6 - \frac{0.6^2}{2} = \frac{1039}{1297}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right)$$

$$\Rightarrow V_{T,5} = 2.0 - \frac{\frac{1039}{1297}\left((2.0-0.44)0.6 - \frac{0.6^2}{2}\right) - \frac{0.6^2}{2}}{0.6}$$

$$\Rightarrow V_{T,5} \approx 0.691V$$

$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB}| + 2|\phi_F|} - \sqrt{2|\phi_F|}\right)$, Eq.4 and Eq.5 gives:

$$\begin{cases} 0.587 = 0.44 + \gamma\left(\sqrt{1+2|\phi_F|} - \sqrt{2|\phi_F|}\right) \\ 0.691 = 0.44 + \gamma\left(\sqrt{2+2|\phi_F|} - \sqrt{2|\phi_F|}\right) \end{cases} \Rightarrow \frac{0.587-0.44}{0.691-0.44} = \frac{\sqrt{1+2|\phi_F|} - \sqrt{2|\phi_F|}}{\sqrt{2+2|\phi_F|} - \sqrt{2|\phi_F|}}$$

$\frac{0.587-0.44}{0.691-0.44}=A$ and $2|\phi_F|=X$ gives:

$$A=\frac{\sqrt{1+X}-\sqrt{X}}{\sqrt{2+X}-\sqrt{X}} \Rightarrow A\sqrt{2+X}-A\sqrt{X}=\sqrt{1+X}-\sqrt{X} \Rightarrow A\sqrt{2+X}-\sqrt{1+X}=(A-1)\sqrt{X}$$

$$\Rightarrow A^2(2+X)+(1+X)-2A\sqrt{(2+X)(1+X)}=(A-1)^2X$$

$$\Rightarrow 2A^2+A^2X+1+X-(A^2-2A+1)X=2A\sqrt{(2+X)(1+X)}$$

$$\Rightarrow 2A^2+1+X(A^2+1-A^2+2A-1)=2A\sqrt{(2+X)(1+X)}$$

$$\Rightarrow (2A^2+1)+2AX=2A\sqrt{(2+X)(1+X)}$$

$$\Rightarrow (2A^2+1)^2+4AX(2A^2+1)+4A^2X^2=4A^2(2+X)(1+X)$$

$$\Rightarrow 4A^4+4A^2+1+4AX+8A^3X+4A^2X^2=8A^2+12A^2X+4A^2X^2$$

$$\Rightarrow 4A^4+4A^2+1-8A^2=12A^2X-4AX-8A^3X$$

$$\Rightarrow 4A^4+4A^2+1-8A^2=X(12A^2-4A-8A^3)$$

$$\Rightarrow X=\frac{4A^4+4A^2+1-8A^2}{12A^2-4A-8A^3}$$

$$\Rightarrow 2|\phi_F|=\frac{4A^4+4A^2+1-8A^2}{12A^2-4A-8A^3}$$

$$\Rightarrow 2|\phi_F|\approx 0.6V$$

Eq.4: $0.587=0.44+\gamma\left(\sqrt{1+0.6}-\sqrt{0.6}\right)$

$$\Rightarrow \frac{0.587-0.44}{\sqrt{1+0.6}-\sqrt{0.6}}=\gamma$$

$$\Rightarrow \gamma\approx 0.3V^{\frac{1}{2}}$$

Use Eq.1 to find W/L:

$$I_{d,1}=100\cdot10^{-6}\frac{W}{L}\left((2.5-0.44)0.6-\frac{0.6^2}{2}\right)(1+0.08\cdot1.8)=1812\cdot10^{-6}$$

$$\Rightarrow \frac{W}{L}=\frac{1812}{100\left((2.5-0.44)0.6-\frac{0.6^2}{2}\right)(1+0.08\cdot1.8)}$$

$$\Rightarrow \frac{W}{L}\approx 15$$

3.8

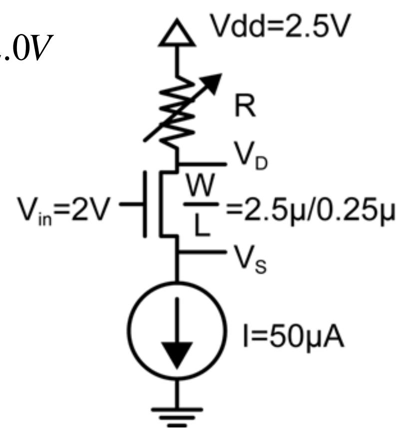
An NMOS device is plugged into the test configuration shown below in figure 0.4. The input V_{in} = 2V. The current source draws a constant current of 50 µA. R is a variable resistor that can assume values between 10 kΩ and 30 kΩ. The transistor M1 experiences short channel effects and as the following parameters: $k' = 110\mu A/V^2$, $V_T = 0.4V$ and $V_{DSAT} = 0.6V$

The transistor has $\frac{W}{L} = \frac{2.5\mu m}{0.25\mu m}$. For simplicity, body effect and channel length modulation can be neglected (λ=0, γ=0)

a)

When R = 10 kΩ, find the operation region, V_D and V_S.

$$V_D = Vdd - R \cdot I = 2.5 - 10 \cdot 10^3 \cdot 50 \cdot 10^{-6} = 2.5 - 0.5 = 2.0V$$



Assume the device is in saturation, this assumption will be verified afterwards. We need to assume one region to calculate the current and

$$I_d = \frac{k_n'}{2}\frac{W}{L}(V_{gs} - V_T)^2 = 50\mu A$$

$$V_{gs} = \sqrt{\frac{50 \cdot 10^{-6}}{\frac{k_n'}{2}\frac{W}{L}}} + V_T = \sqrt{\frac{2 \cdot 50}{110\frac{2.5}{0.25}}} + 0.4 = 0.7015 \approx 0.7V$$

$$V_{gs} = V_g - V_s = 0.7 \Rightarrow V_s = V_g - 0.7 = 2 - 0.7 = 1.3V$$

Now verify that the assumption about saturation region was correct?

$$V_{\min} = \min((V_{gs} - V_T), V_{ds}, V_{DSAT}) = \min((0.7 - 0.4), (2.0 - 1.3), 0.6) = \min(0.3, 0.7, 0.6) = 0.3$$

$V_{\min} = V_{gt} \Rightarrow$ NMOS region of operation is: **Saturation**

Answer: V_D = 2V, V_S = 1.3V, Mode of operation: Saturation

b)

When R = 30 kΩ, again find the operation region, V_D and V_S.

$$V_D = Vdd - R \cdot I = 2.5 - 30 \cdot 10^3 \cdot 50 \cdot 10^{-6} = 2.5 - 1.5 = 1.0V$$

Assume the device is in linear region since $V_D < V_g - V_T$.

$$I_d = k_n' \frac{W}{L}\left((V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2} \right) = 50\mu A$$

$$110 \cdot 10^{-6} \frac{2.5}{0.25}\left((V_g - V_s - V_T)(V_d - V_s) - \frac{(V_d - V_s)^2}{2} \right) = 50 \cdot 10^{-6}$$

$$1100\left((2 - V_s - 0.4)(1 - V_s) - \frac{(1 - V_s)^2}{2} \right) = 50$$

$$1.6 - 2.6V_s + V_s^2 - 0.5 + V_s - 0.5V_s^2 = \frac{50}{1100}$$

$$V_s^2 - 3.2V_s + 2.2 - \frac{1}{11} = 0$$

$$V_s = 1.6 \pm \sqrt{1.6^2 - \left(2.2 - \frac{1}{11} \right)} = 1.6 \pm 0.6715$$

$V_S = 0.93V$ or $V_S = 2.27V$ (unrealistic since higher than drain voltage).

Check region of operation:

$$V_{\min} = \min((V_{gs} - V_T), V_{ds}, V_{DSAT}) = \min((2 - 0.93 - 0.4), (1 - 0.93), 0.6) = \min(0.67, 0.07, 0.6) = 0.07$$

$V_{\min} = V_{ds} \Rightarrow$ NMOS region of operation is: **Linear region**

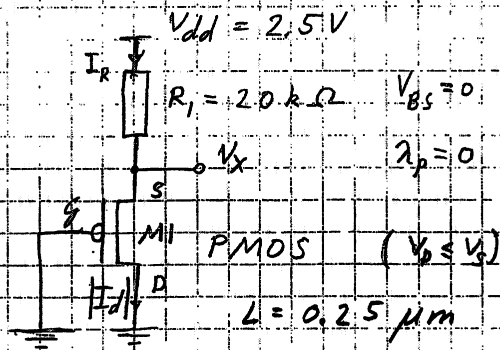
Answer: V_D = 1V, V_S = 0.93V, Mode of operation: Linear

c)

For the case of R = 10 kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

It would increase! V_D is fixed due to the fixed current. $(1+ \lambda V_{ds})$ would try to increase the current to more than the available 50 μA, thus V_{gs} must decrease to compensate for this and keep the current constant. Since V_g is fixed V_S will increase.

(3.9)



$V_{BS} = 0$

$\lambda_p = 0$

$(V_D \le V_S)$

$L = 0.25\,\mu m$

a) Neglect short channel effects

$\Rightarrow$ No velocity saturation exist!

$V_{gt} = -V_X + |V_T|$

$V_{DS} = -V_X$

Assume that M1 is on. $\Rightarrow V_{gt} \le 0$

$\Rightarrow V_X \ge |V_T|$

$$\Rightarrow V_{min} = \min\left(|-V_X + |V_T||,\ V_X\right) = \min\left(V_X - |V_T|,\ V_X\right)$$

$$V_{min} = V_X - |V_T| = |V_{gt}| \Rightarrow \text{saturation}$$

$$|I_D| = |k_p'|\,\frac{W}{L}\,(V_X - |V_T|)\left(V_X - |V_T| - \frac{V_X - |V_T|}{2}\right)$$

$$= |k_p'|\,\frac{W}{L}\,\frac{(V_X - |V_T|)^2}{2}$$

$$I_R = \frac{V_{dd} - V_X}{R}$$

(3.9) a) (cont'd)

Including short channel effects: ($V_{DSAT} = -1V$)

$V_{min} = \min\left(|V_{gt}|, |V_{ds}|, |V_{DSAT}|\right)$

$= \min\left(V_X - |V_T|, V_X, 1\right)$

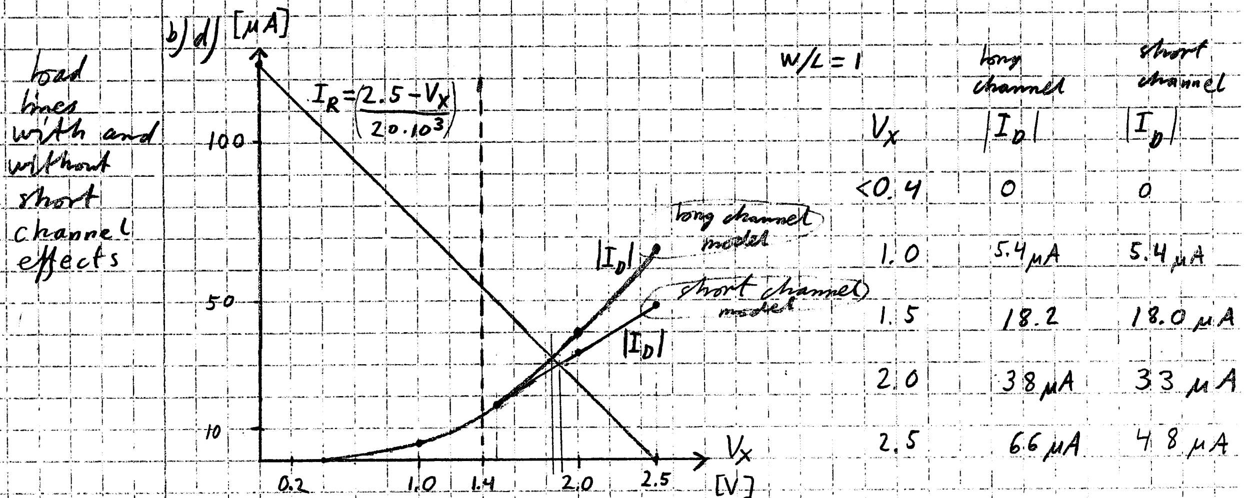
$\underbrace{V_X \geq |V_T|}_{\text{Assuming that M1 is on}} \Rightarrow V_X - |V_T| < V_X$

For which V_X is $1 < V_X - |V_T|$ (results in vel. sat.)

$V_X > 1 + |V_T| = 1.4\,V$

$\therefore$ $V_X < 1.4\,V \Rightarrow$ sat. , $V_X > 1.4\,V \Rightarrow$ vel. sat.

b)/d)



$W/L = 1$

V_X	long channel $\lvert I_D \rvert$	short channel $\lvert I_D \rvert$
<0.4	0	0
1.0	5.4 μA	5.4 μA
1.5	18.2	18.0 μA
2.0	38 μA	33 μA
2.5	66 μA	48 μA

Sat $\Rightarrow |I_D| = |k_p'| \dfrac{W}{L} \cdot \dfrac{(V_X - 0.4)^2}{2}$

Vel. Sat. $\Rightarrow |I_D| = |k_p'| \dfrac{W}{L} \cdot 1 \cdot \left(V_X - 0.4 - \dfrac{1}{2}\right)$

$|k_p'| = 30 \cdot 10^{-6}\ A/V^2$

As seen in figure, V_X rises with short channel effects.

(3.9) c) Determine the width W such that $V_x = 1.5\,V$.

☆ Long channel:

$$\frac{2.5-1.5}{20\cdot10^3} = \frac{30\cdot10^{-6}}{2}\,\frac{W}{0.25\cdot10^{-6}}\,(1.5-0.4)^2$$

$\Rightarrow W \approx 0.69\ \mu m$

☆ Short channel

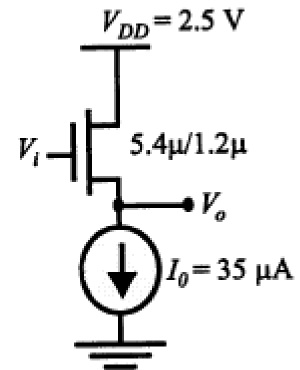
$$\frac{2.5-1.5}{20\cdot10^3} = 30\cdot10^{-6}\cdot\frac{W}{0.25\cdot10^{-6}}\,1.0\cdot(1.5-0.9)$$

$\Rightarrow W \approx 0.69\ \mu m$

3.10

The circuit of figure 0.6 is known as a source-follower configuration. It achieves a DC-level shift between the input and ouput. The value of this shift is determined by the current I_0.
Assume: $\gamma = 0.4$, $k' = 115\mu A/V^2$, $2|\phi_F| = 0.6V$, $\lambda = 0$, $V_{T0} = 0.43V$

and $\frac{W}{L} = \frac{5.4\mu}{1.2\mu}$ (no short channel effects).



a)

Derive an expression giving V_i as a function of V_o and $V_T(V_o)$.
If we neglect body effect, what is the nominal value of the level shift performed by this circuit?

Assume saturated device:

$$I_d = \frac{k_n'}{2}\frac{W}{L}(V_i - V_o - V_T)^2 = I_0$$

$$V_i = \sqrt{\frac{I_0}{\frac{k_n'}{2}\frac{W}{L}}} + V_o + V_T$$

Neglecting body effect ($\gamma = 0$) we have $V_T = V_{T0}$

$$V_i = \sqrt{\frac{I_0}{\frac{k_n'}{2}\frac{W}{L}}} + V_{T0} + V_o$$, where the first two terms is the level shift (LS).

$$LS = \sqrt{\frac{35 \cdot 10^{-6}}{\frac{115 \cdot 10^{-6}}{2}\frac{5.4}{1.2}}} + 0.43 = 0.7977 \approx 0.8V$$

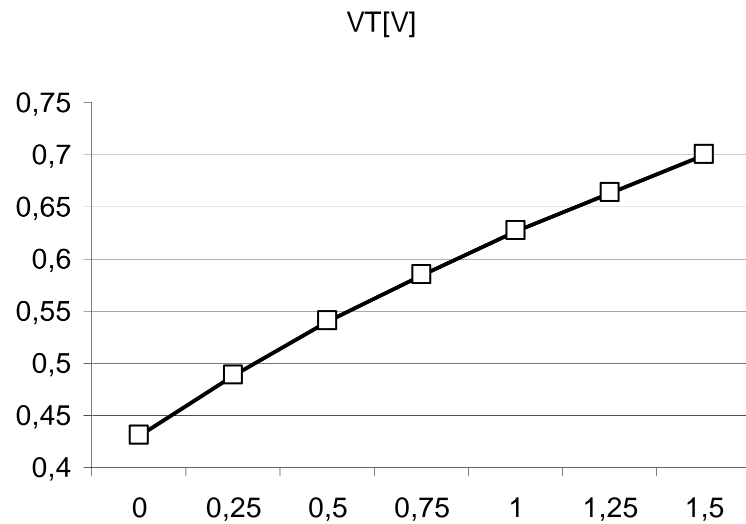
b)

The NMOS transistor experiences a shift in V_T due to the body effect. Find V_T as a function of V_o for V_o ranging from 0 to 1.5V with 0.25V intervals. Plot V_T vs V_o.

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB}| + 2|\phi_F|} - \sqrt{2|\phi_F|}\right)$$

$$V_{SB} = V_o \Rightarrow V_T = 0.43 + 0.4\left(\sqrt{|V_o| + 0.6} - \sqrt{0.6}\right)$$

V_o[V]	V_T[V]
0	0.43
0.25	0.489
0.5	0.540
0.75	0.585
1.00	0.626
1.25	0.664
1.5	0.700

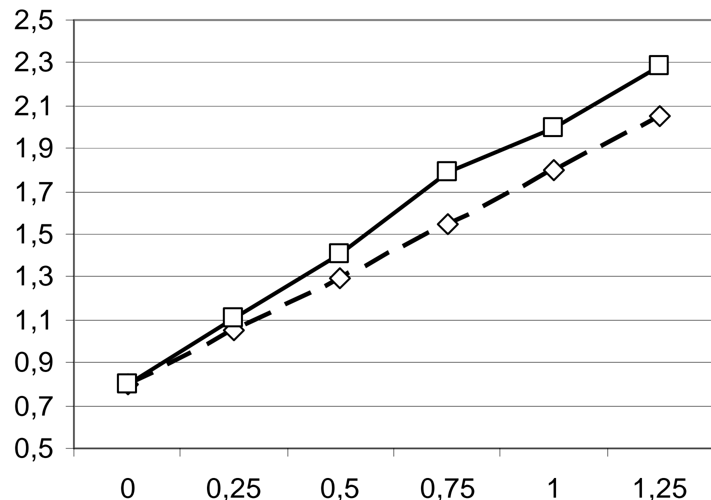


c)

Plot V_o vs V_i as V_o varies from 0 to 1.5 with 0.25V intervals. Plot two curves, one neglecting the body effect, and one accounting for it. How does the body effect influence the operation of the level converter? At V_o(body effect) = 1.5V, find V_o(ideal) and thus determine the maximum error introduced by the body effect.

$$V_i = \sqrt{\frac{2 \cdot I_0}{k_n' \frac{W}{L}}} + V_{T0} + V_o$$

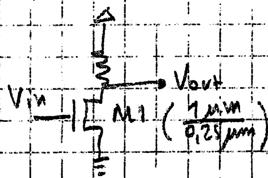
V_o [V]	$V_{i,ideal}$	$V_{i,body}$
0	0,798	0,798
0,25	1,048	1,107
0,5	1,298	1,408
0,75	1,548	1,793
1,00	1,798	1,994
1,25	2,048	2,282
1,5	2,298	2,568



Maximum error is 0.27 V for V_o = 1.5 V

3.17 Compute the gate and diffusion capacitances for transistor M1 of figure 0.7. Assume that drain and source areas are rectangular, and are 1 μm wide and 0,5 μm long. Use the parameters of example 3.5 to determine the capacitance values. Assume $m_j = 0{,}5$ and $m_{jsw} = 0{,}44$. Also compute the total charge stored at node "In", for the following initial conditions:

a) $V_{in} = 2{,}5V$; $V_{out} = 2{,}5V$; $0{,}5V$; $0V$



See example 3.10 p. 112

$L_D = L_S = 0{,}5\,\mu m$; $m_j = 0{,}5$; $m_{jsw} = 0{,}44$

From example 3.10 and table 3.5 (p. 112)

$C_{ox} = 6fF/\mu m^2$; $C_o = 0{,}31 fF/\mu m$; $C_{jo} = 2 fF/\mu m^2$

$\phi_b = 0{,}9V$; $C_{jsw} = 0{,}28 fF/\mu m$; $\phi_{bsw} = 0{,}9V$

GATE CAPACITANCE (Table 3.4 p.109)

Region of operation	C_g
CUT OFF	$C_{ox}WL + 2C_oW$
LINEAR	$C_{ox}WL + 2C_oW$
SAT.; VEL.SAT	$\frac{2}{3}C_{ox}WL + 2C_oW$

DIFFUSION CAPACITANCE (pp. 110 - 111)

$$C_{diff} = C_{bottom} + C_{sw} = C_j L_s W + C_{jsw}(2L_s + W)$$

(p. 83)

$$C_j = \frac{C_{jo}}{\left(1 - \frac{V_{BD}}{\phi_b}\right)^{m_j}} \; ; \; C_{jsw} = \frac{C_{jsw0}}{\left(1 - \frac{V_{BD}}{\phi_{bsw}}\right)^{m_{jsw}}}$$

BD = Bulk - Drain

3.17

a)

* $V_{in} = 2{,}5V$

$V_{out} = 2{,}5V \Rightarrow$ Vel. Saturation

$C_g = \frac{2}{3} \cdot 6 \cdot 1 \cdot 0{,}25 + 2 \cdot 0{,}31 \cdot 1 = \underline{1{,}62 fF}$

$C_{diff,drain} = \frac{2}{\left(1 - \frac{-2{,}5}{0{,}9}\right)^{0{,}5}} \cdot 0{,}5 \cdot 1 + \frac{0{,}28}{\left(1 - \frac{-2{,}5}{0{,}9}\right)^{0{,}44}} \cdot (2 \cdot 0{,}5 + 1) =$

$= \underline{0{,}827 fF}$

$C_{diff,source} = \frac{2}{\left(1 - \frac{0}{0{,}9}\right)^{0{,}5}} \cdot 0{,}5 \cdot 1 + \frac{0{,}28}{\left(1 - \frac{0}{0{,}9}\right)^{0{,}44}} (2 \cdot 0{,}5 + 1) = \underline{1{,}56 fF}$

$Q = C_g V_{in} = 1{,}62 \cdot 10^{-15} \cdot 2{,}5 = \underline{4{,}05 fC}$

* $V_{out} = 0{,}5V \Rightarrow$ LINEAR REGION ($V_{ds} < V_{gs} - V_T$)

$C_g = C_{ox} WL + 2 C_o W = 6 \cdot 1 \cdot 0{,}25 + 2 \cdot 0{,}31 \cdot 1 = \underline{2{,}12 fF}$

$C_{diff,drain} = \frac{2}{\left(1 - \frac{-0{,}5}{0{,}9}\right)^{0{,}5}} \cdot 0{,}5 \cdot 1 + \frac{0{,}28}{\left(1 - \frac{-0{,}5}{0{,}9}\right)^{0{,}44}} \cdot (2 \cdot 0{,}5 + 1) = \underline{1{,}263 fF}$

$C_{diff,source}$ = ALWAYS THE SAME

$Q = C_g \cdot V_{in} = 2{,}12 \cdot 10^{-15} \cdot 2{,}5 = \underline{5{,}3 fC}$

* $V_{out} = 0V \Rightarrow$ LINEAR REGION

C_g = / same as for $V_{out} = 0{,}5V$ / = $\underline{2{,}12 fF}$

$C_{diff,drain} = C_{diff,source} = \underline{1{,}56 fF}$

$Q = C_g \cdot V_{in} = \underline{5{,}3 fC}$

b) $V_{in} = 0V \Rightarrow$ Always cutoff, regardless of V_{ds}

$C_g = C_{ox} WL + 2 C_o W = \underline{2{,}12 fF}$

$Q = C_g \cdot V_{in} = \underline{0C}$

C_{diff} are the same as in part a)

$V_{out} = 2{,}5V$ $C_{diff,drain} = \underline{0{,}827 fF}$

$V_{out} = 0{,}5V$ $C_{diff,drain} = \underline{1{,}263 fF}$

$V_{out} = 0V$ $C_{diff,drain} = C_{diff,source} = \underline{1{,}56 fF}$