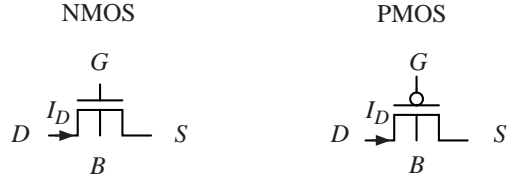


Equations for the MOS transistor



Definition of source (S) and drain (D)

$$\text{NMOS: } V_S \leq V_D \quad \text{PMOS: } V_S \geq V_D$$

Voltage notations

$$V_{GS} = V_G - V_S, \quad V_{DS} = V_D - V_S, \quad V_{SB} = V_S - V_B, \quad V_{GT} = V_{GS} - V_T$$

Threshold voltage

$$V_T = V_{T0} + \gamma(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|})$$

Unified model

$$\text{NMOS: } V_{GT} \leq 0 \quad (\text{PMOS: } V_{GT} \geq 0) \Rightarrow \text{Subthreshold region } (I_D \approx 0)$$

$$\text{NMOS: } V_{GT} \geq 0 \quad (\text{PMOS: } V_{GT} \leq 0) \Rightarrow I_D = k' \frac{W}{L} V_{min} \left(|V_{GT}| - \frac{V_{min}}{2} \right) (1 + \lambda V_{DS})$$

$$V_{min} = \min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$$

$$V_{min} = |V_{GT}| \Rightarrow \text{saturation region}$$

$$V_{min} = |V_{DS}| \Rightarrow \text{resistive (linear, triode) region } (\lambda = 0)$$

$$V_{min} = |V_{DSAT}| \Rightarrow \text{velocity saturation region}$$

V_{DSAT} dependency on channel length

$$V_{DSAT} = L \xi_c$$

Subthreshold region

$$\text{NMOS: } V_{GT} \leq 0 \Rightarrow I_{Dn} = I_{0n} \frac{W}{L} e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}} \left(1 - e^{-\frac{qV_{DSn}}{kT}} \right) (1 + \lambda_n V_{DSn})$$

$$\text{PMOS: } V_{GT} \geq 0 \Rightarrow I_{Dp} = I_{0p} \frac{W}{L} e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}} \left(1 - e^{-\frac{qV_{SDp}}{kT}} \right) (1 + \lambda_p V_{SDp})$$

Model parameters for 0.25 μm CMOS devices

Parameters for drain current calculations

	V_{T0} [V]	γ [$\sqrt{\text{V}}$]	V_{DSAT} [V]	k' [$\mu\text{A}/\text{V}^2$]	λ	Φ_F [V]
NMOS	0.43	0.40	0.63	115	0.06	-0.30
PMOS	-0.40	-0.40	-1.00	-30	-0.10	0.30

Parameters for capacitance calculations

	C_{ox} [fF/ μm^2]	C_O [fF/ μm]	C_j [fF/ μm^2]	m_j	ϕ_b [V]	C_{jsw} [fF/ μm]	m_{jsw}	ϕ_{bsw} [V]
NMOS	6	0.31	2.0	0.50	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

Gate capacitance

Overlap capacitance

$$C_{GSO} = C_{GDO} = C_{ox} x_d W = C_O W$$

Channel capacitance

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

Condition	C_{GCB}	C_{GCS}	C_{GCD}
$V_{GTn} \leq 0, V_{GTp} \geq 0$	$C_{ox} WL$	0	0
$V_{GTn} > 0, V_{GTp} < 0, V_{DS} \leq V_{GT} $	0	$C_{ox} WL/2$	$C_{ox} WL/2$
$V_{GTn} > 0, V_{GTp} < 0, V_{GT} \leq V_{DS} $	0	$2C_{ox} WL/3$	0

Junction capacitance

Junction capacitance as function of voltage

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

Average capacitance during transition from V_1 to V_2

$$C_{eq} = K_{eq} C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1 - m)} [(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}] C_{j0}$$

Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

Switch functions

$$S_N = \overline{F(A, B, \dots)}, S_P = F(\bar{A}, \bar{B}, \dots)$$

Boolean algebra

De Morgans' theorem

$$\overline{\overline{X + Y + Z + \dots}} = \overline{\overline{X} \overline{Y} \overline{Z} \dots}, \quad \overline{\overline{X} \overline{Y} \overline{Z} \dots} = \overline{\overline{X}} + \overline{\overline{Y}} + \overline{\overline{Z}} + \dots$$

Expansion in sum

$$f(X, Y, Z, \dots) = Xf(1, Y, Z, \dots) + \bar{X}f(0, Y, Z, \dots)$$

Expansion in product

$$f(X, Y, Z, \dots) = [X + f(0, Y, Z, \dots)][\bar{X} + f(1, Y, Z, \dots)]$$

Transmission line

Characteristic impedance

$$Z_0 = \sqrt{l/c}$$

Velocity of wave

$$v = 1/\sqrt{l c}$$

Reflection coefficient for a transmission line (Z_0) terminated by a load (Z_L)

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

Elmore delay

P_i = "the path between node 0 and i ".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths P_i and P_j ".

R_{ij} = "the sum of all resistances in P_{ij} ".

Time constant from node 0 to i : $\tau_{di} = \sum_{j=0}^n R_{ij} C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)/k}$, where

k = "tapering factor", N = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.