Digital ICs — Lectures

1) **Introduction** [Ch. 1]   TSEI03/TSTE86
2) **Devices** [Ch. 3, 4]   TSEI03/TSTE86
3) **Interconnect** [Ch. 4, 9]   TSTE86
4) **Circuits** [Ch. 5]   TSEI03/TSTE86
5) **Combinational logic** [Ch. 6]   TSEI03/TSTE86
6) **Sequential circuits** [Ch. 7]   TSEI03/TSTE86
7) **Synchronization** [Ch. 10]   TSTE86
8) **Adders** [Ch. 11]   TSEI03/TSTE86
9) **Multipliers** [Ch. 11]   TSTE86
10) **Memory** [Ch. 12]   TSEI03/TSTE86
11) **Manufacturing** [Ch. 2]   TSTE86
12) **System design** [Ch. 8]   TSTE86

Switch Activity
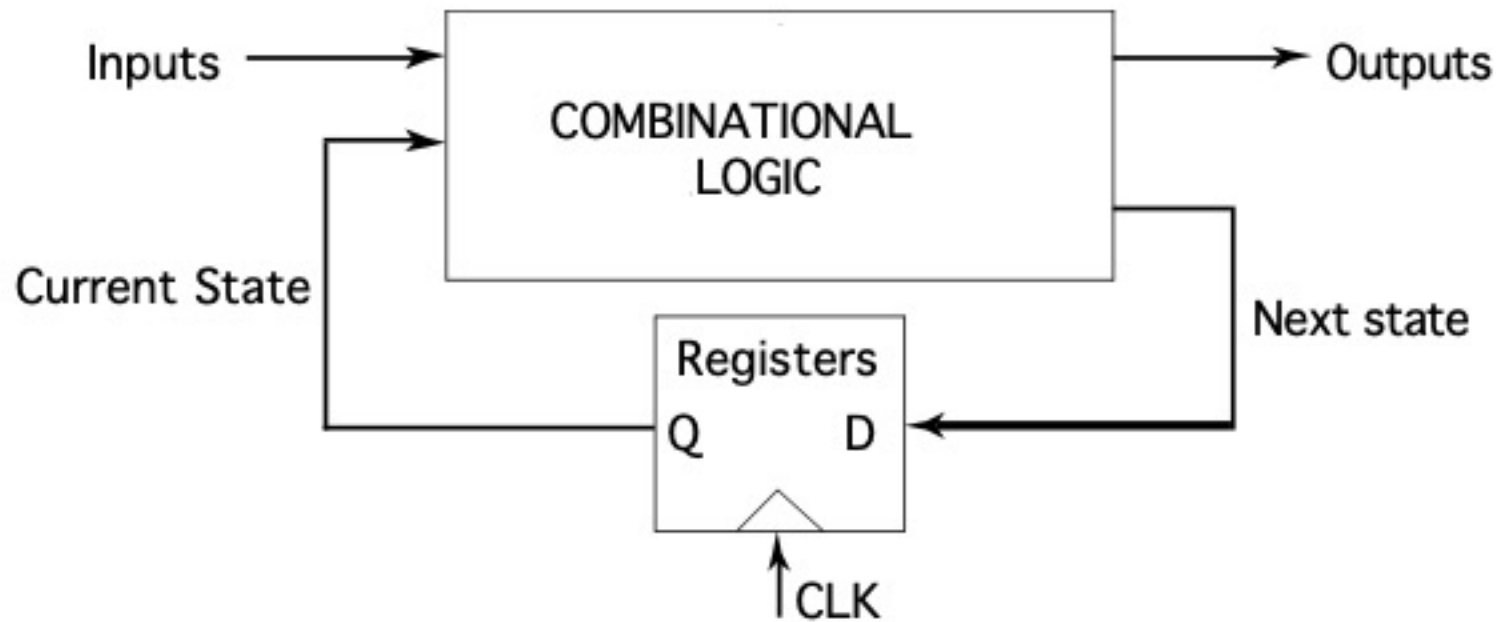
ideal switching

V_{DD} ⇕

T

V_{DD} ⇕

C
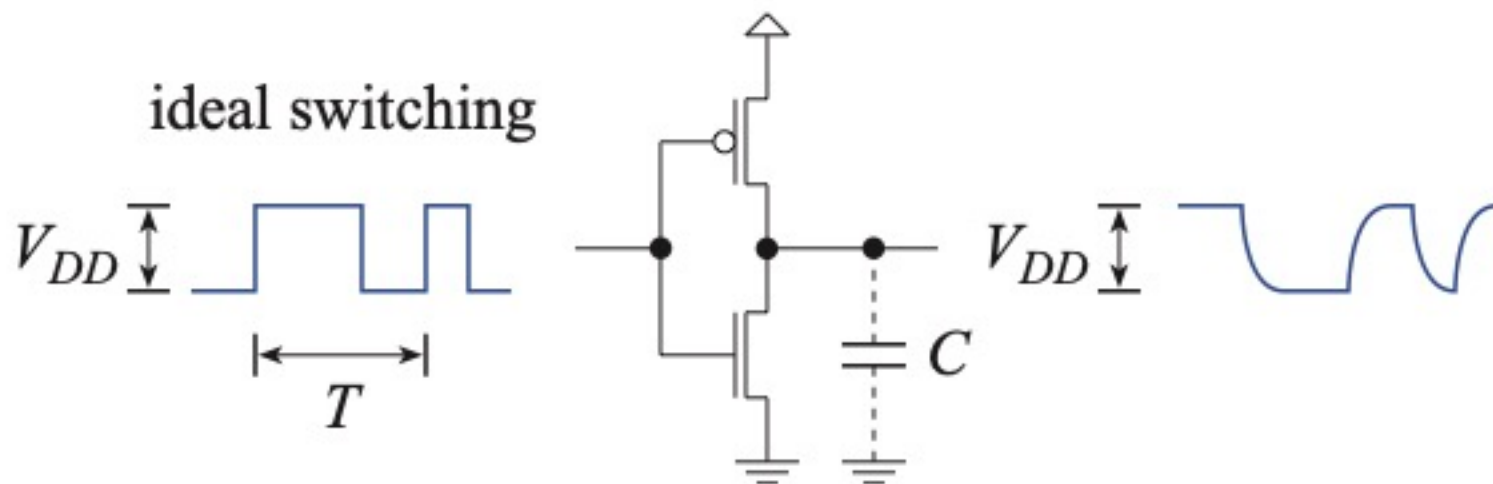
Dynamic power dissipation is

$$P_d = I_{av}V_{DD} = \frac{Q_C}{T}V_{DD} = fCV_{DD} \cdot V_{DD} = af_{clk}CV_{DD}^2$$
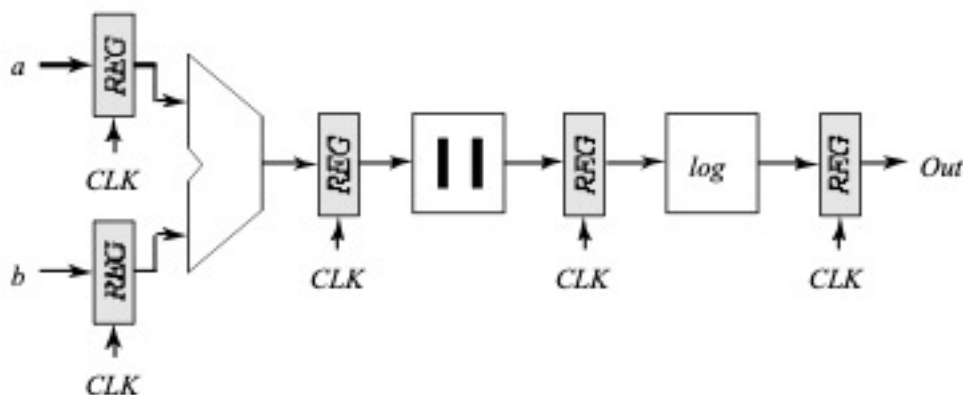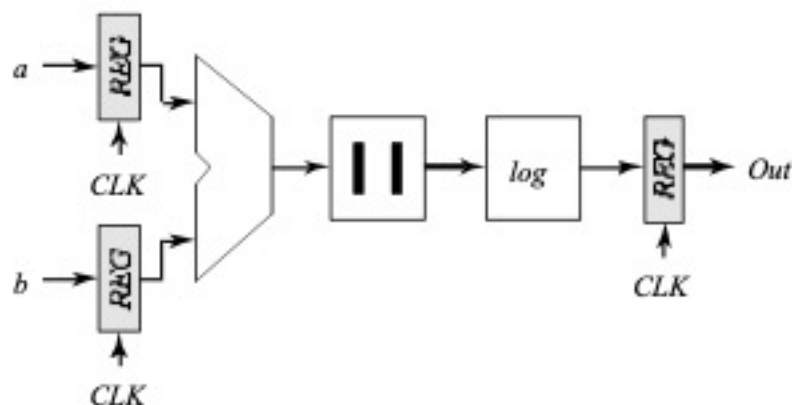
where a is the <u>switch activity</u>

Sequential Logic

Inputs → COMBINATIONAL LOGIC → Outputs

Current State

Next state

Registers
Q   D

CLK

2 storage mechanisms
- positive feedback
- charge-based

Pipelining

Reference

Pipelined

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$|a_1 + b_1|$	
3	$a_3 + b_3$	$|a_2 + b_2|$	$\log(|a_1 + b_1|)$
4	$a_4 + b_4$	$|a_3 + b_3|$	$\log(|a_2 + b_2|)$
5	$a_5 + b_5$	$|a_4 + b_4|$	$\log(|a_3 + b_3|)$

Transcription Gate
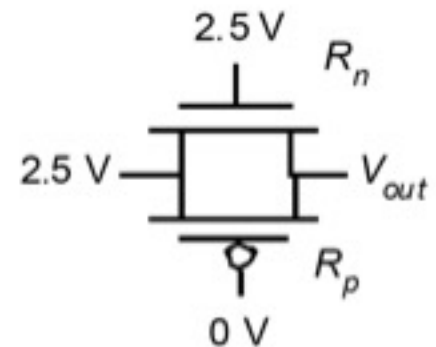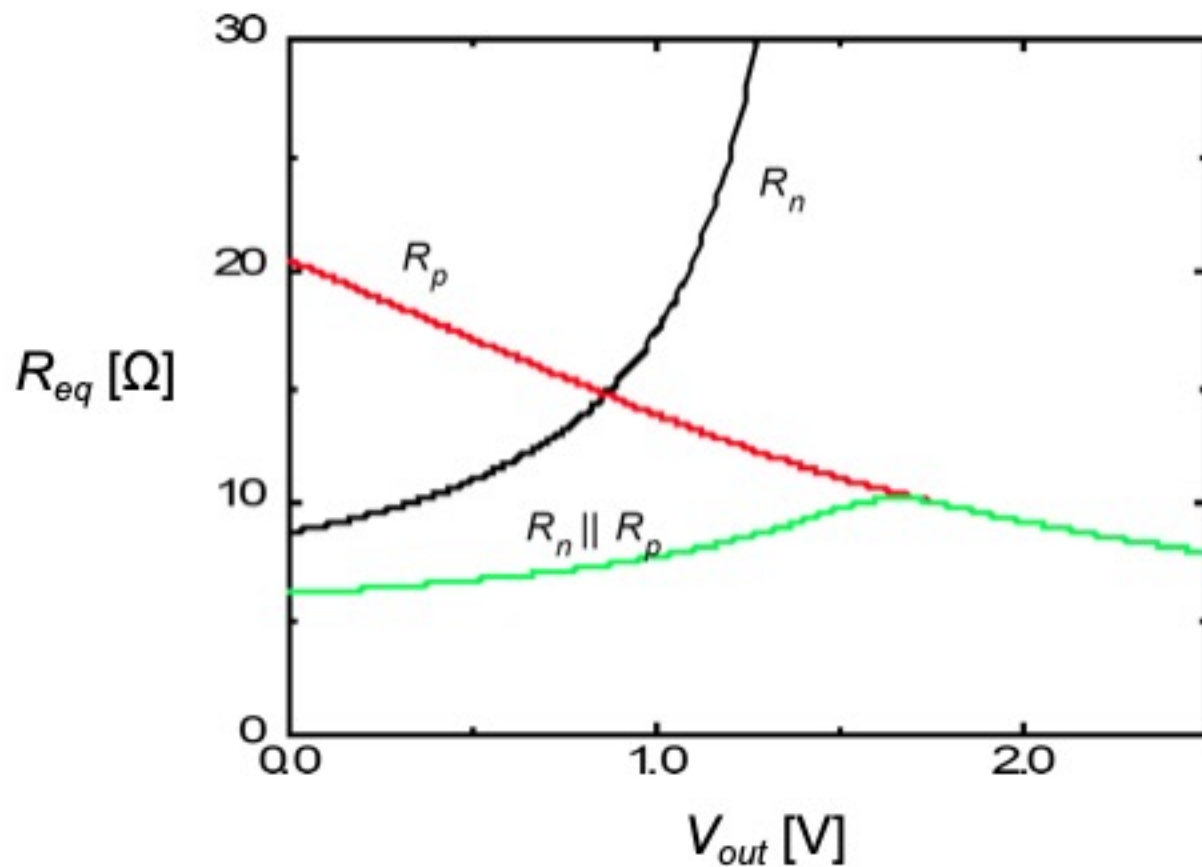
Master-Slave Register
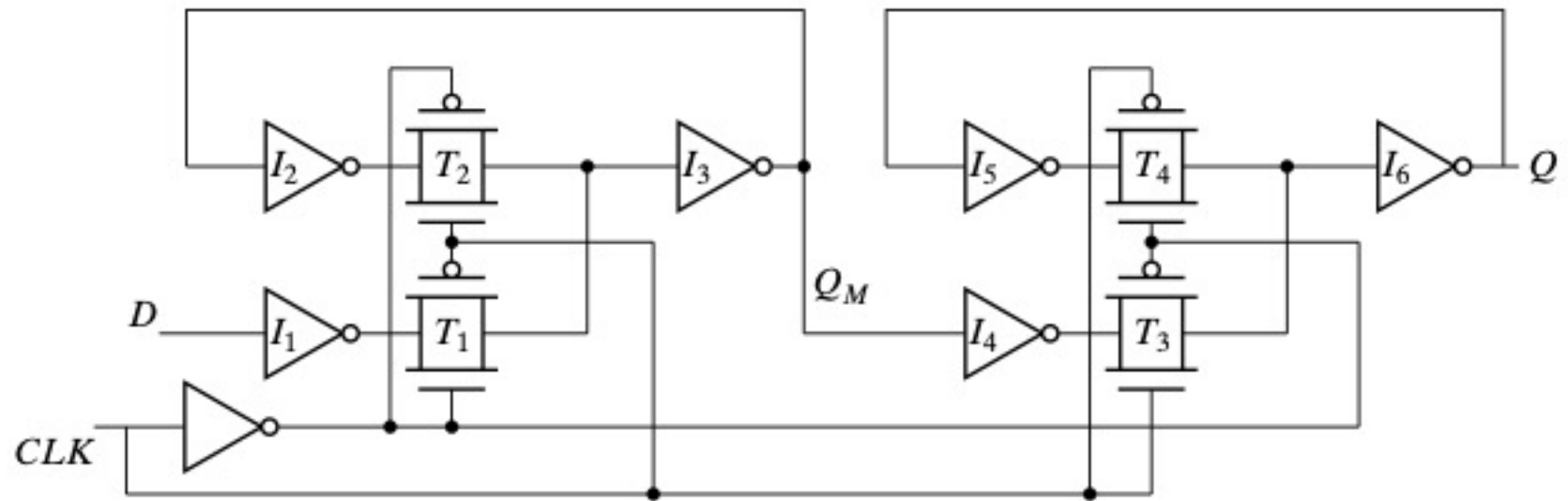
Multiplexer-based latch pair

Positive Feedback

V_{i1} —▷— $V_{o1} = V_{i2}$ —▷— V_{o2}

$V_{o2} = V_{i1}$

V_{o1} vs V_{i1}

V_{i2} vs V_{o2}
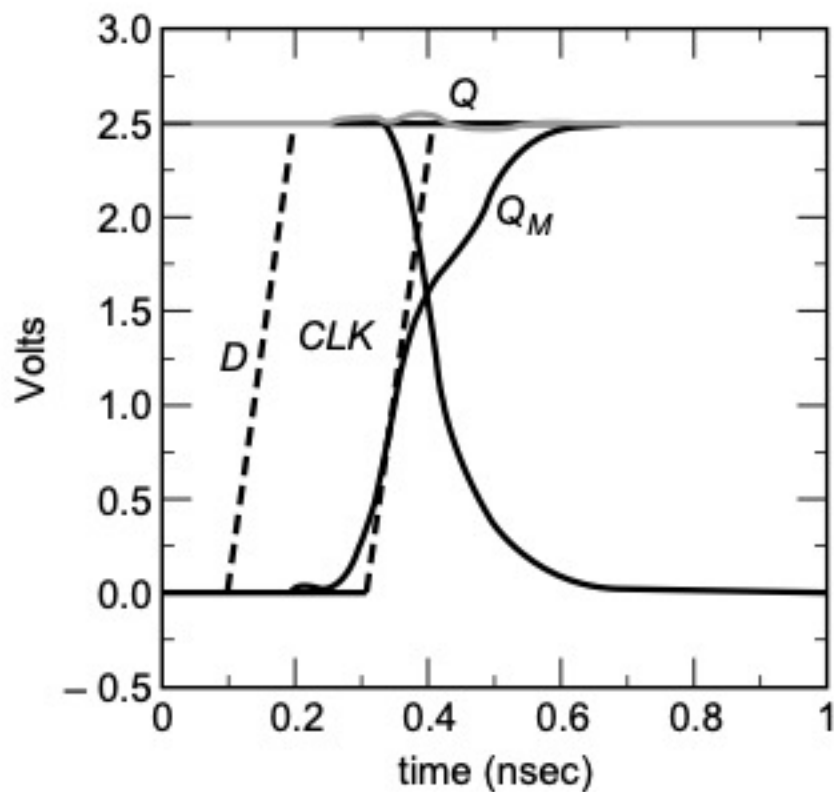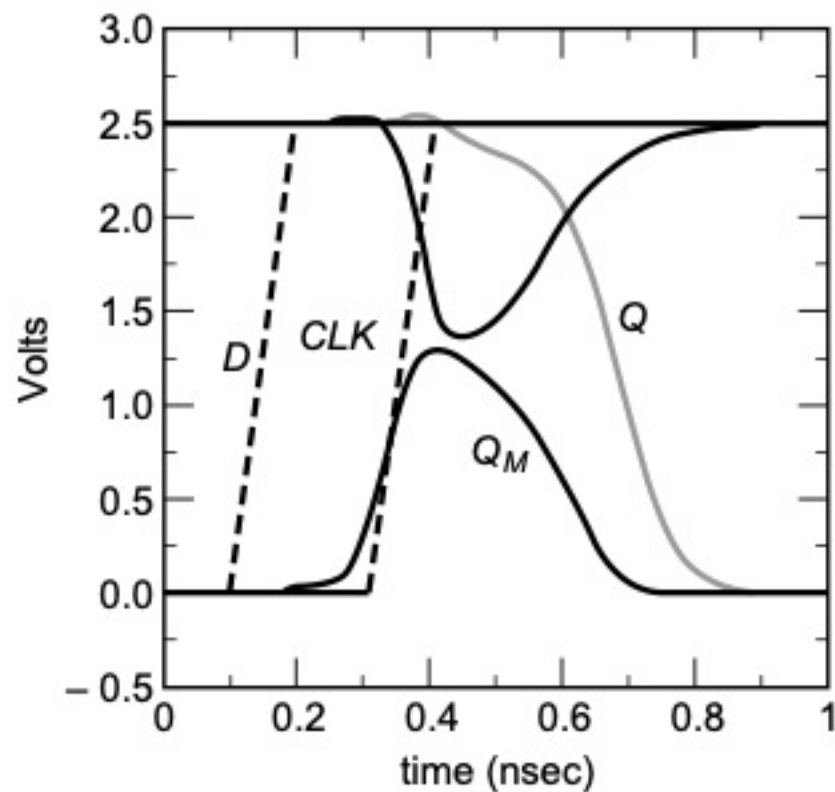
$V_{i2} = V_{o1}$

A

C

B

$V_{i1} = V_{o2}$
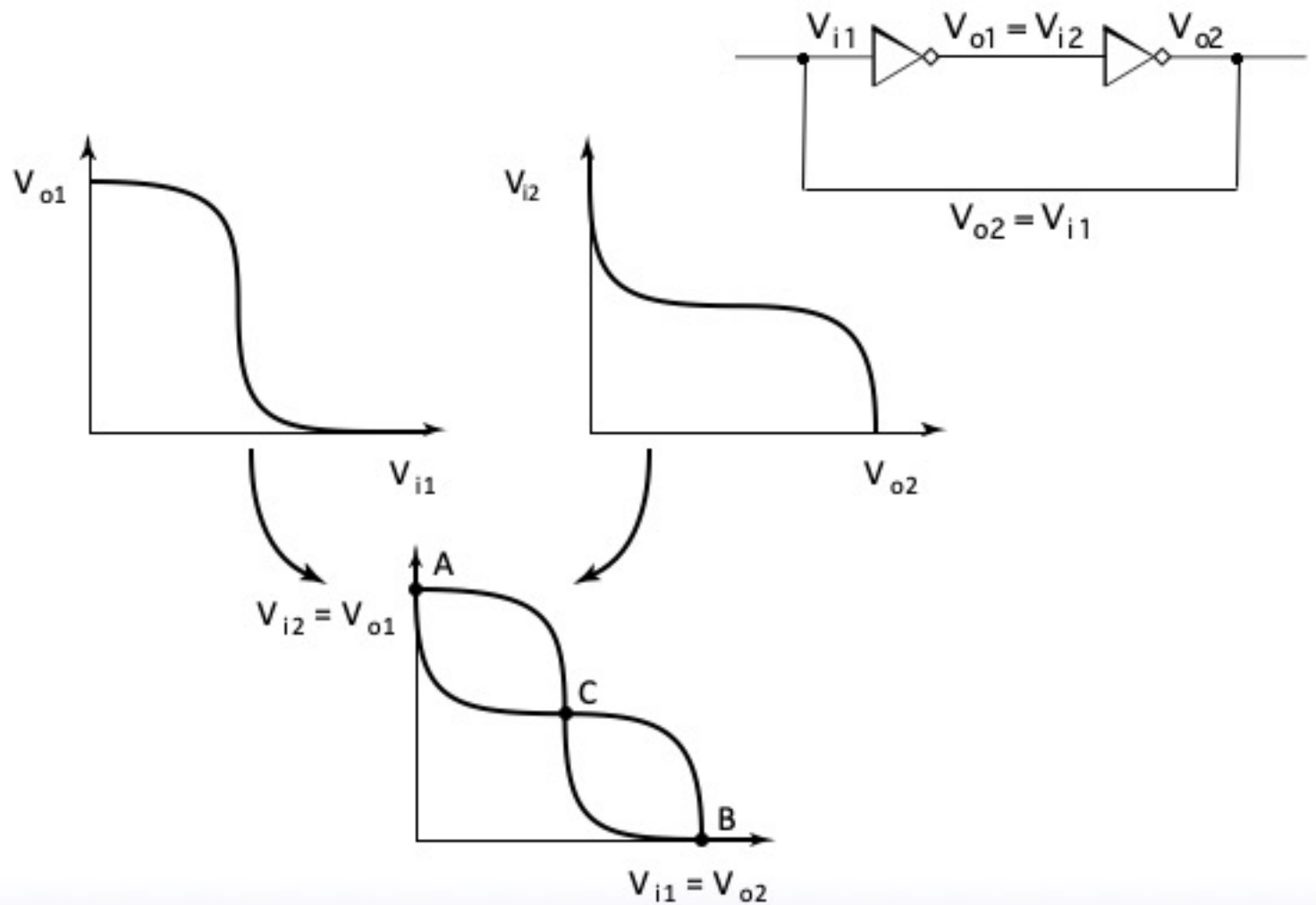
Metastability
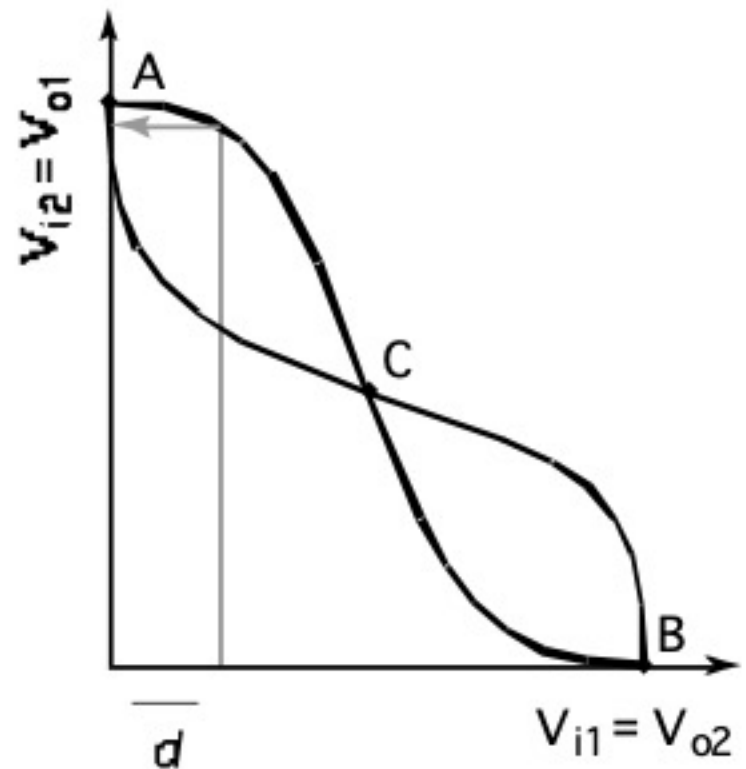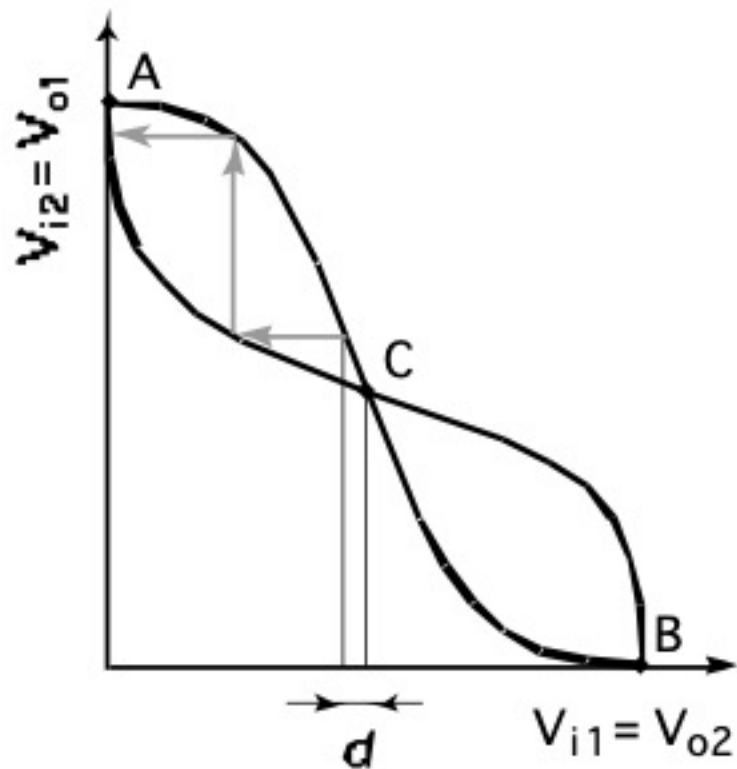
Gain is larger than 1 in the transition region

Setup Time
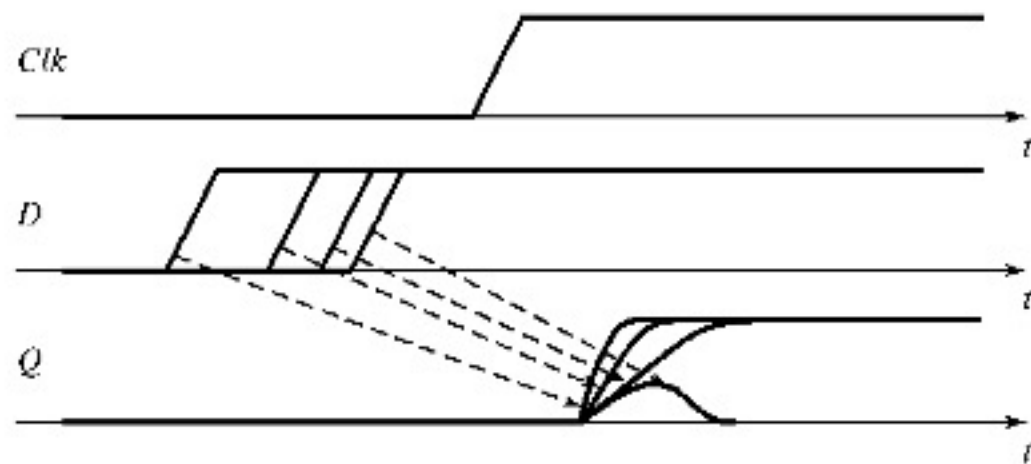

(a) $T_{D->CLK} = 0.21$ nsec

(b) $T_{D->CLK} = 0.20$ nsec

Setup and Hold Times

Clk

D

Q

t_{clk-q}

$1.05(t_{clk-q})$

t_{su}

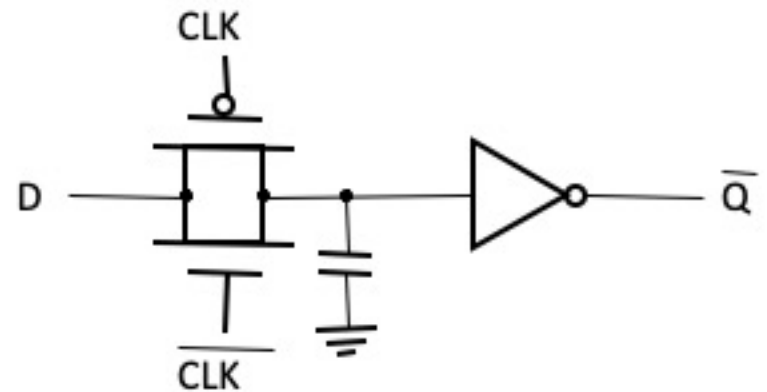τ_H
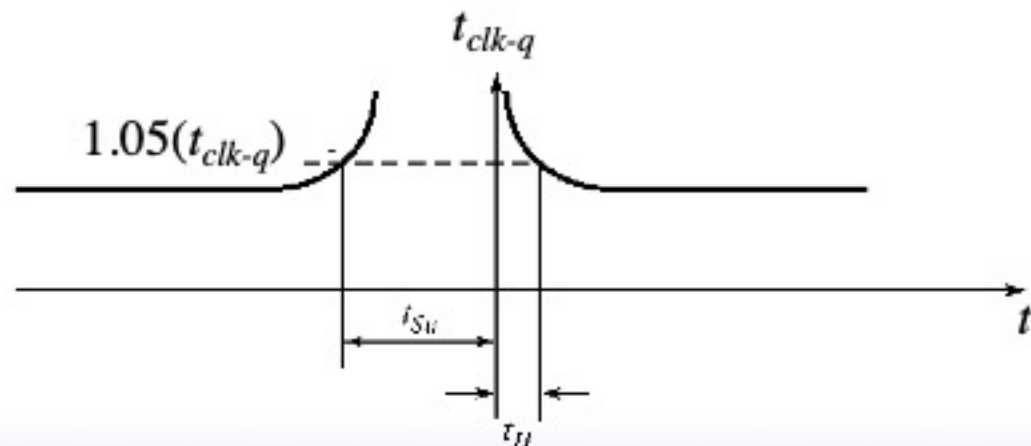
Timing Definitions
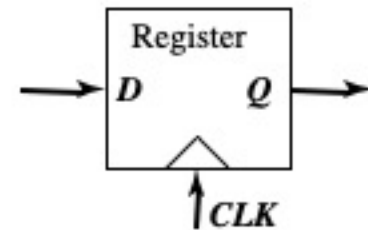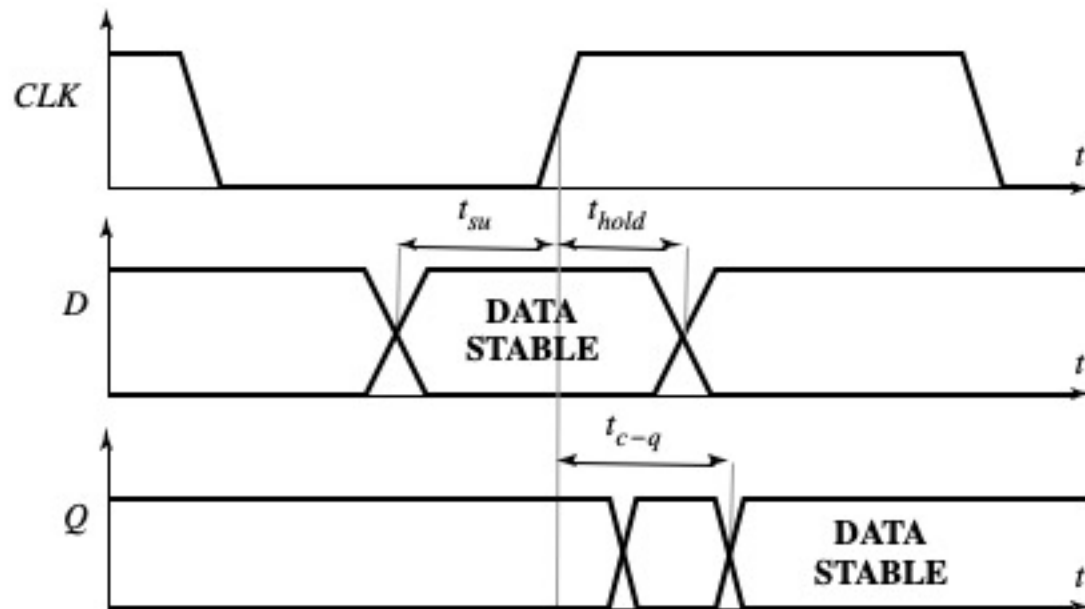
Storage Mechanisms
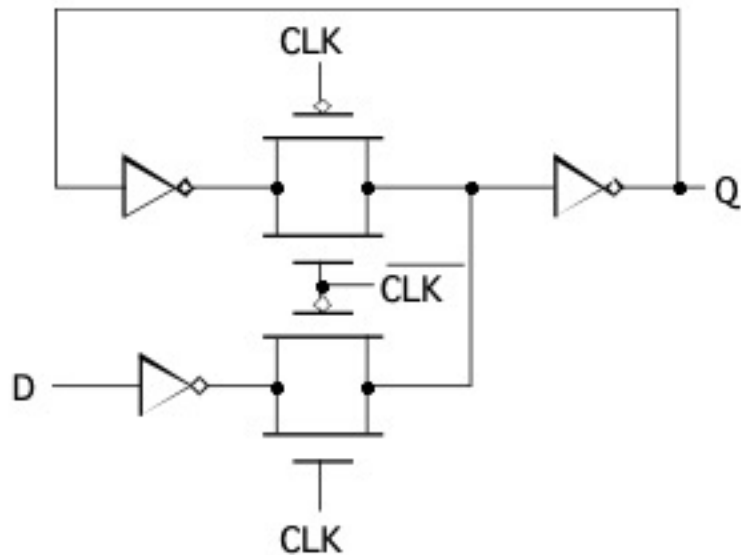
Static latch

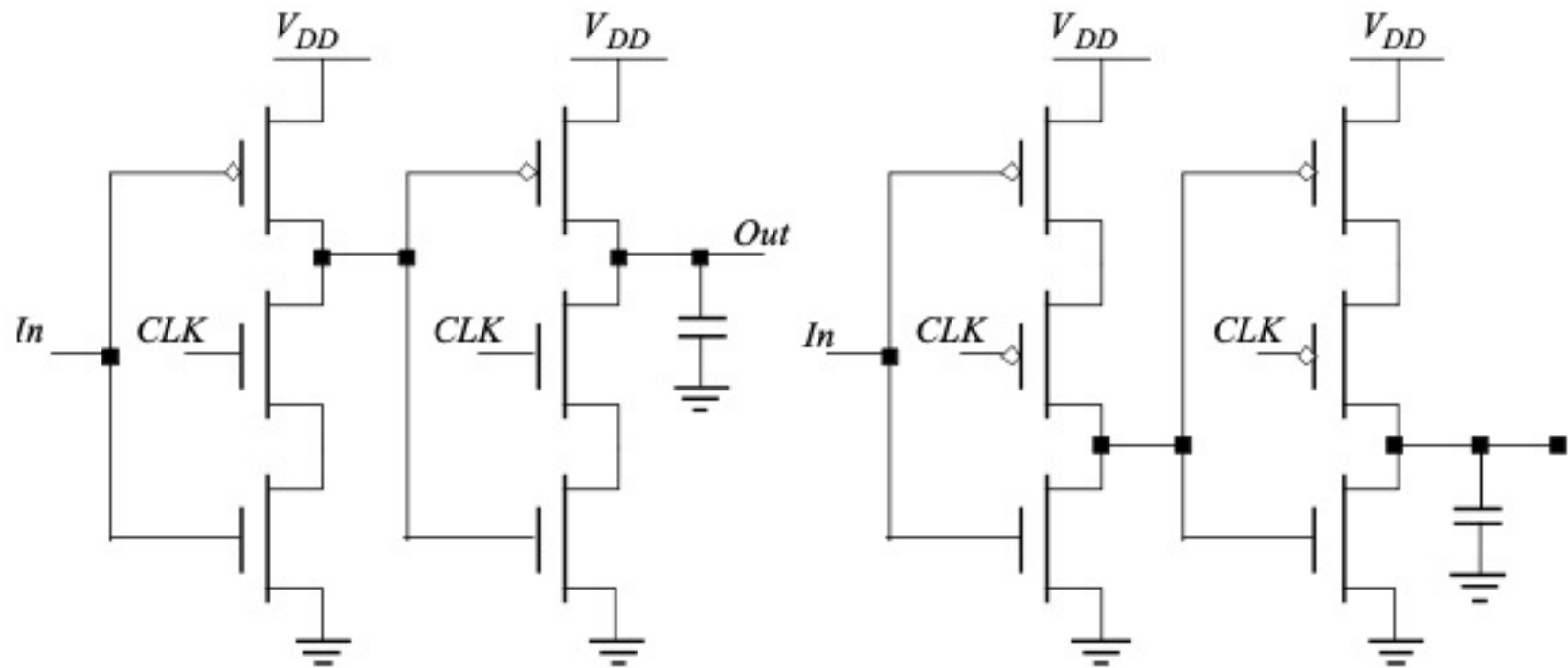Dynamic latch

Keeper
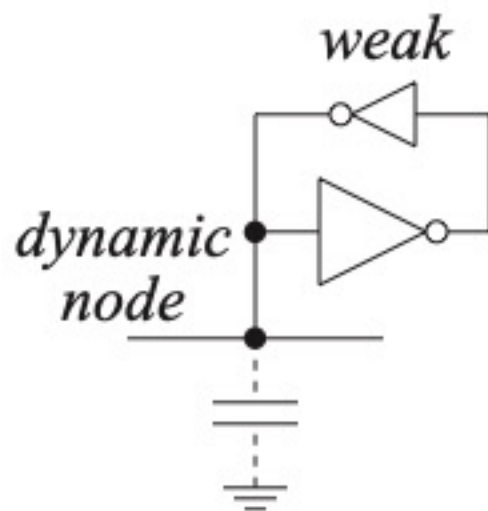
A keeper makes a dynamic circuit static

C²MOS Dynamic Latch

Master Stage   Slave Stage
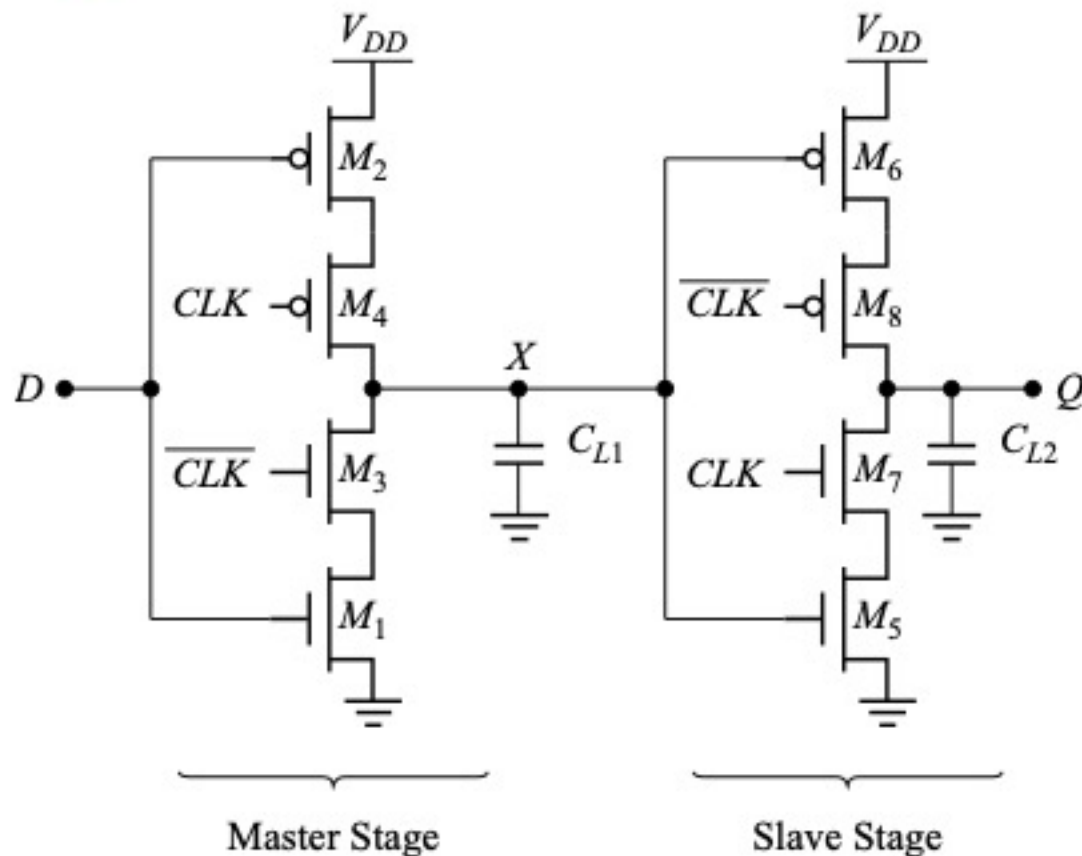
Keepers are often used to make the flip-flop static

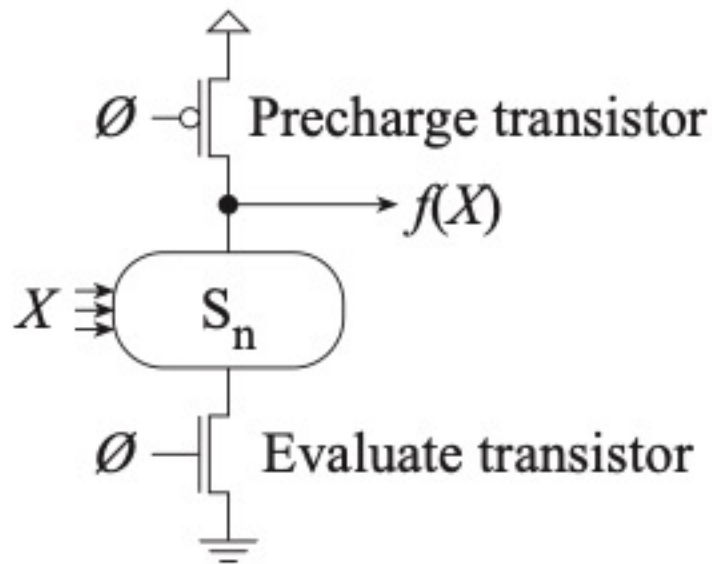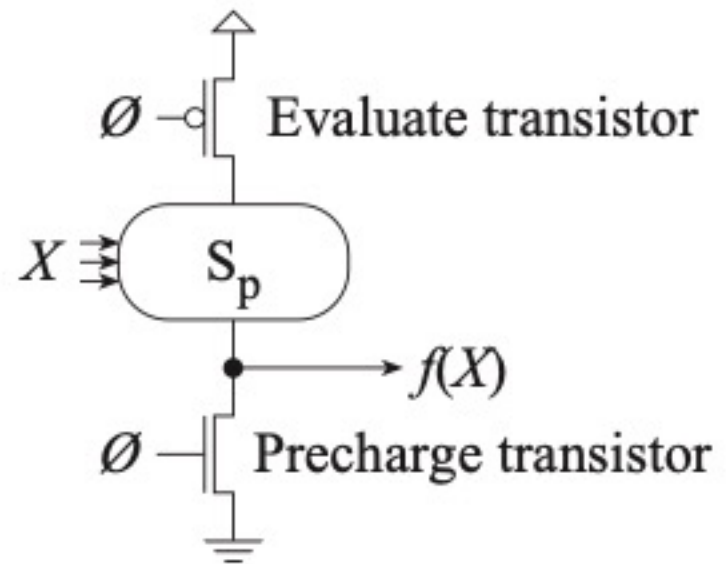# TSPC Dynamic Latch

Positive latch
(transparent when CLK = 1)

Negative latch
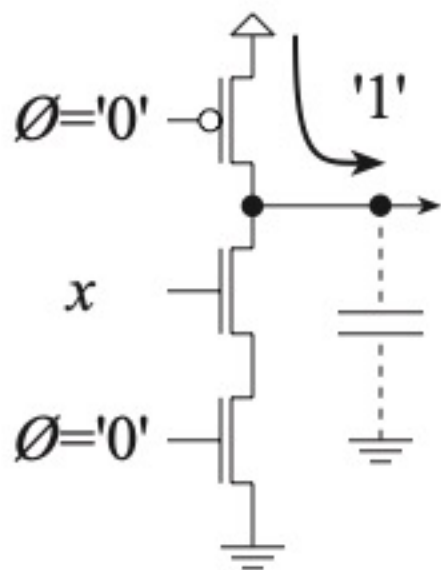(transparent when CLK = 0)

Precharged Logic

Ø —○| Precharge transistor

$f(X)$

X ⇶ S_n

Ø —| Evaluate transistor

NMOS logic

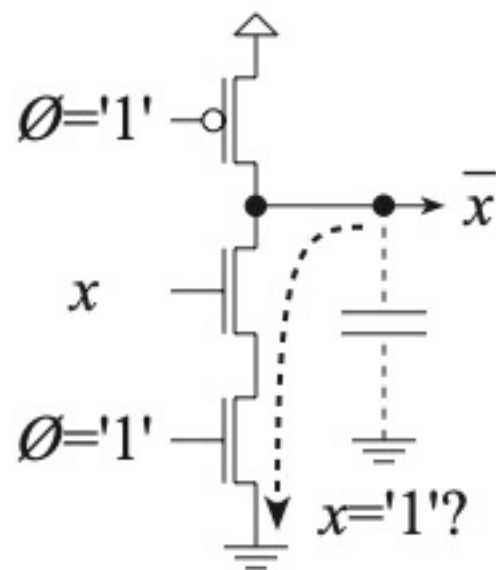Ø —○| Evaluate transistor

X ⇶ S_p
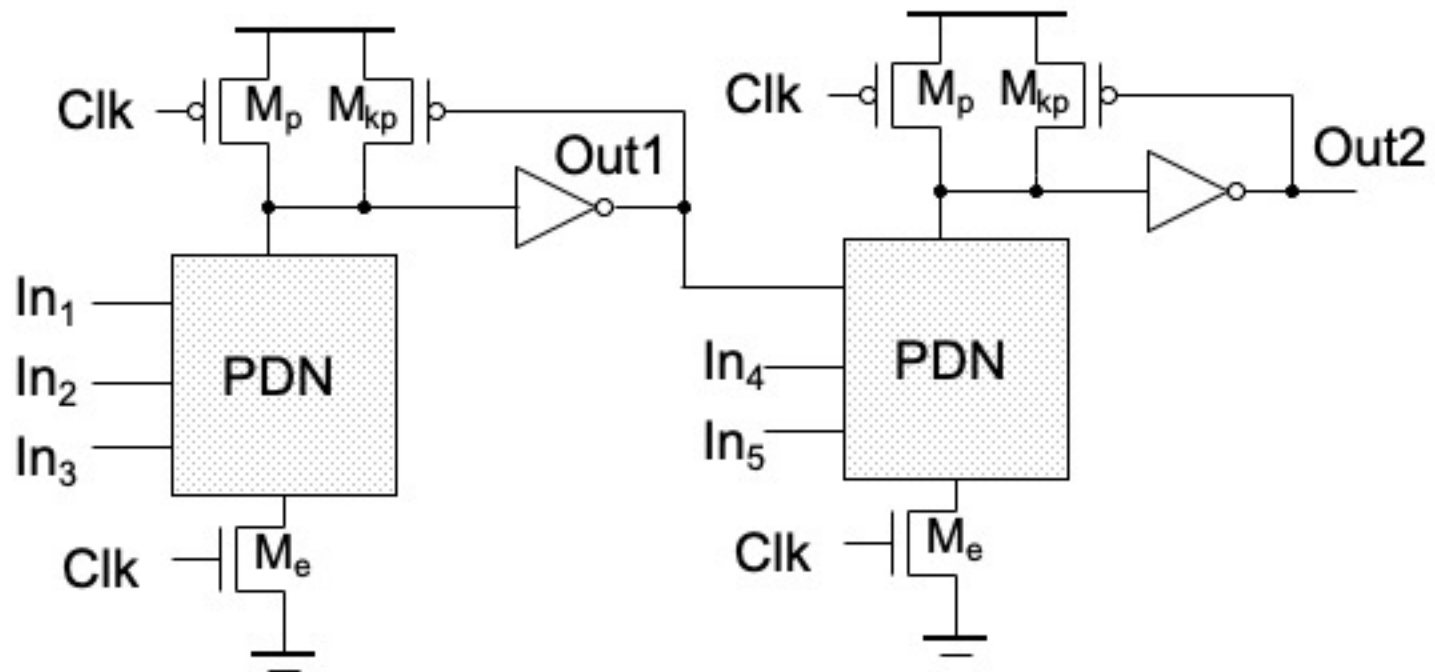
$f(X)$

Ø —| Precharge transistor
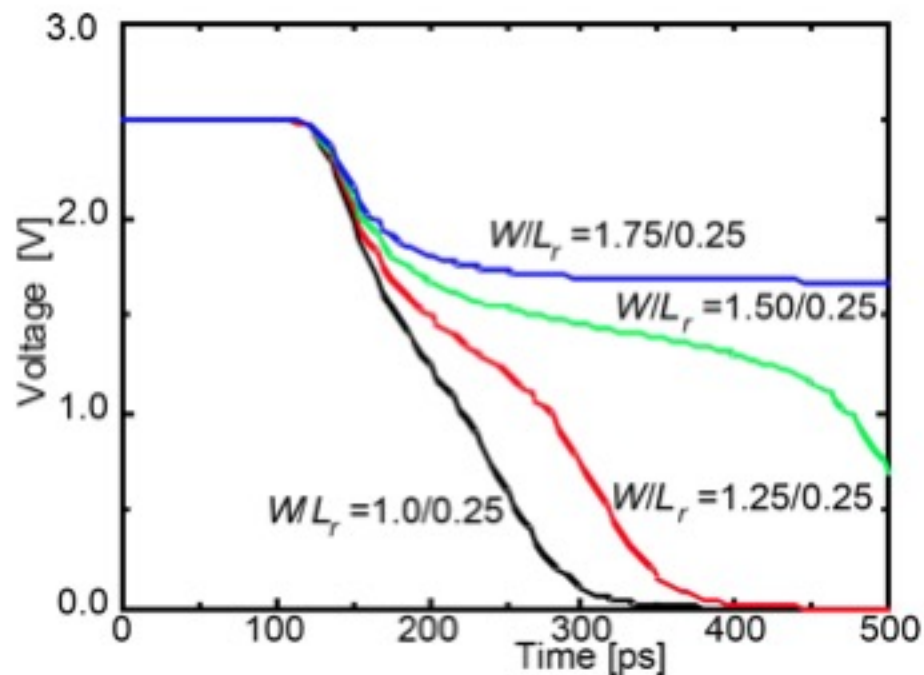
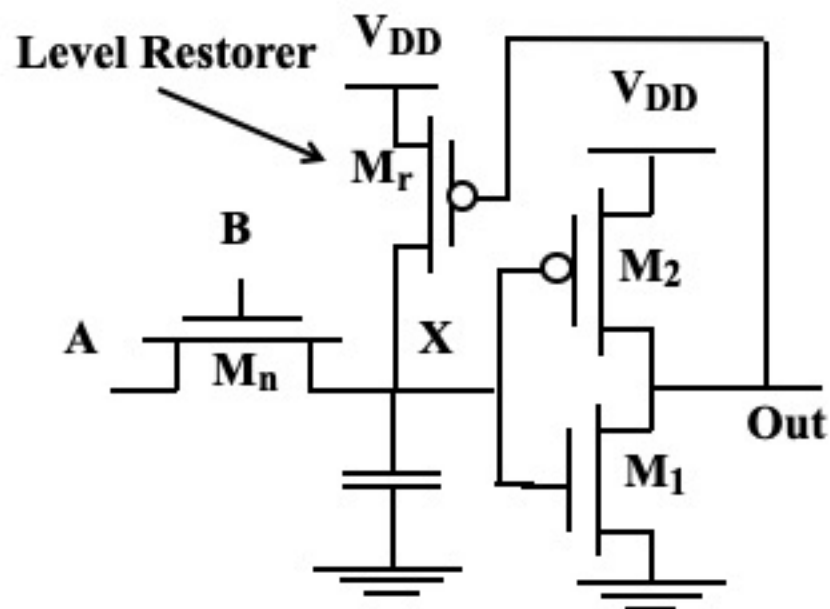PMOS logic

Operation

Precharge phase
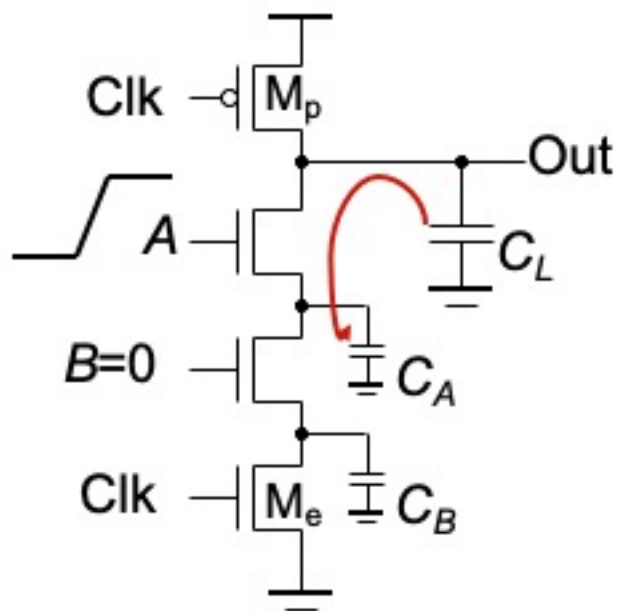
Evaluate phase

Domino Logic
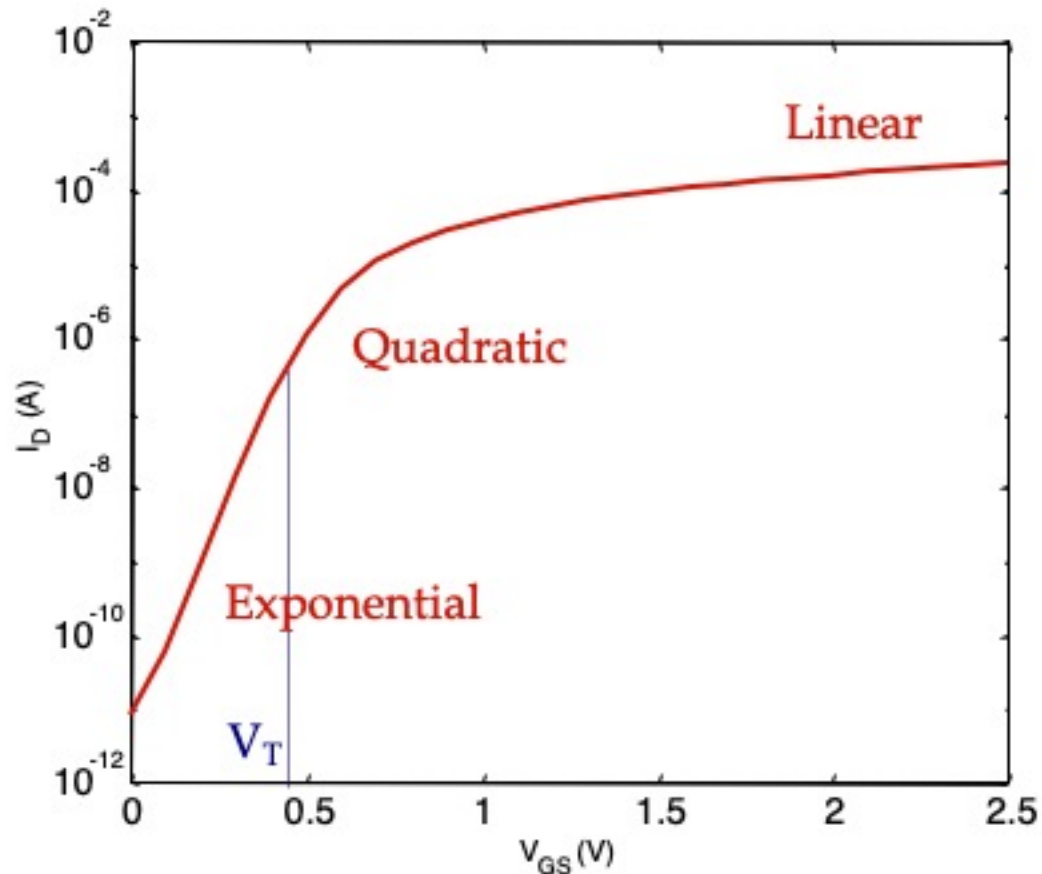
Level Restoring Transistor

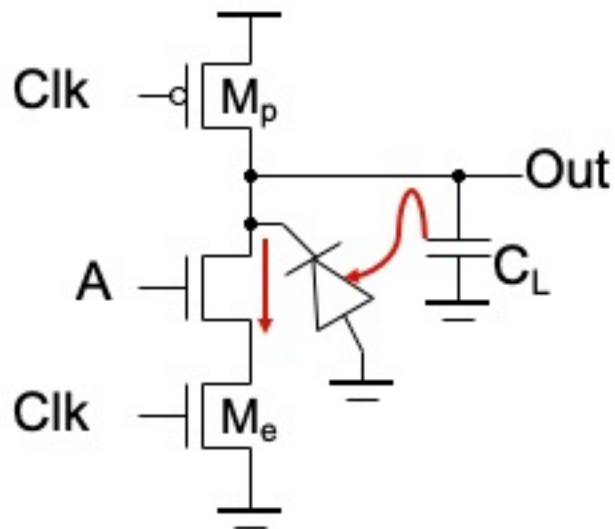Useful in CPL and Domino logic

Charge Sharing

Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness
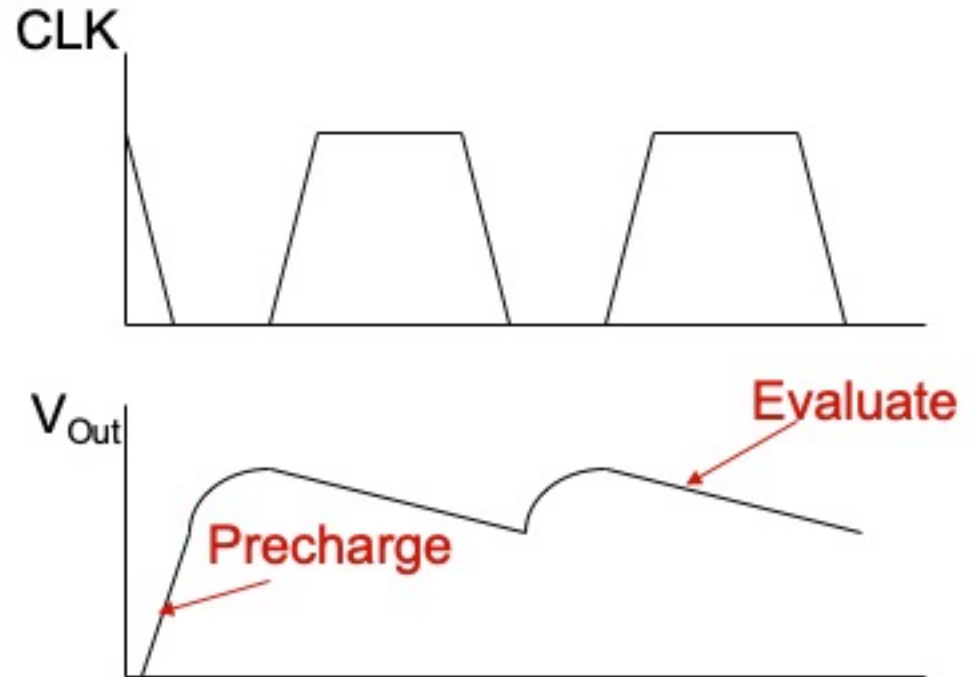
Sub-Threshold Conduction

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right)$$

Charge Leakage

Clk —o[M_p]

A —[ ]

Out

C_L

Clk —[M_e]

Leakage sources

CLK

V_{Out}

Evaluate

Precharge

Dominant component is subthreshold current