Solutions to exam 2020-01-07 in TSTE86 Digital ICs

1.

a) Derive logic function $F = G'$ from the switch net function S_n of the precharged circuit

$$S_n = A(B+C) \Rightarrow G = \overline{S_n(A,B,C)} = \overline{A(B+C)} \Rightarrow F = \overline{G} = A(B+C)$$

b) The clocked PMOSFET is used to precharge G high, which will be the output value if the logic net does not conduct. The clocked NMOSFET is used to evaluate the logic function by connecting the logic net to ground. If the net conducts, G will be discharged to 0.

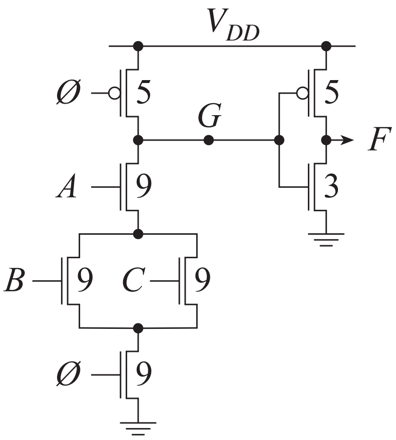
c) Charge sharing may occur according to the following example. If $F(A, B, C)$ is evaluated with $F(0, 1, 0)$, $F(0, 0, 1)$, or $F(0, 1, 1)$, capacitance C_x is discharged. Then if $F(1, 0, 0)$ is evaluated next, the voltage of node G should remain at V_{DD}, but is instead reduced due to sharing of C_G's charge with C_x. Depending on how much the output voltage is reduced, we may need to redesign the circuit to ensure proper operation.

d) Use same (minimum) L for all MOSFETs
The PMOSFET pull-ups consist of single transistors $\Rightarrow W_{P,inv} = 5$
The inverter NMOSFET consists of a single transistor $\Rightarrow W_{N,inv} = 3$
Design all NMOSFETs in a single path to have same width

$$R_{on} \propto \frac{L}{W} \Rightarrow \begin{cases} \frac{L}{W_{N,A}} + \frac{L}{W_{N,B}} + \frac{L}{W_{N,Ø}} = \frac{L}{3} \\ \frac{L}{W_{N,A}} + \frac{L}{W_{N,C}} + \frac{L}{W_{N,Ø}} = \frac{L}{3} \end{cases}$$

$$\Rightarrow \begin{cases} W_{N,A} = W_{N,B} = W_{N,Ø} = 9 \\ W_{N,A} = W_{N,C} = W_{N,Ø} = 9 \end{cases}$$

The circuit with aspect ratios indicated is shown in the schematic to the right



2.

a) V_D is given by the voltage drop over the resistor due to constant current

$V_D = V_{DD} - RI$

$V_D = V_{DD} - RI = 2.5 - 10 \cdot 10^3 \cdot 50 \cdot 10^{-6}$ V $= \underline{2.0 \text{ V}}$

A small R causes a small voltage drop over R, and a large over the MOSFET. Try with saturated operating mode and solve for V_{GS}

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_T)^2 = 50\ \mu\text{A} \Rightarrow$$

$$V_{GS} = \sqrt{I_D \frac{2}{k'}\frac{L}{W}} + V_T = \sqrt{50 \cdot 10^{-6} \frac{2}{115 \cdot 10^{-6}} \frac{0.25}{2.0}} + 0.43 \text{ V} \approx 0.76 \text{ V}$$

Find V_S

$V_S = V_G - V_{GS} = \underline{1.24 \text{ V}}$

Check operation mode

$V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) = \min(0.76 - 0.43, 2.0 - 1.24, 0.63) = V_{GT}$

The MOSFET is <u>saturated</u>.

b) V_D is given by the voltage drop over the resistor due to constant current

$$V_D = V_{DD} - RI = 2.5 - 30 \cdot 10^3 \cdot 50 \cdot 10^{-6} \text{ V} = \underline{1.0 \text{ V}}$$

A large R causes large voltage drop over R, and a small over MOSFET. Try with linear operating mode and solve for V_S

$$I_D = k'\frac{W}{L}V_{DS}\left(V_{GT} - \frac{V_{DS}}{2}\right) \Leftrightarrow V_S^2 - 2\left(V_G - V_T\right)V_S + 2\left(V_G - V_T\right)V_D - V_D^2 - \frac{2I_D L}{k'W} = 0 \Leftrightarrow$$

$$V_S = V_G - V_T \pm \sqrt{\left(V_G - V_T\right)^2 - 2\left(V_G - V_T\right)V_D + V_D^2 + \frac{2I_D L}{k'W}} \approx 1.57 \pm 0.66 \text{ V}$$

$$V_S < V_D \Rightarrow V_S \approx \underline{0.91 \text{ V}}$$

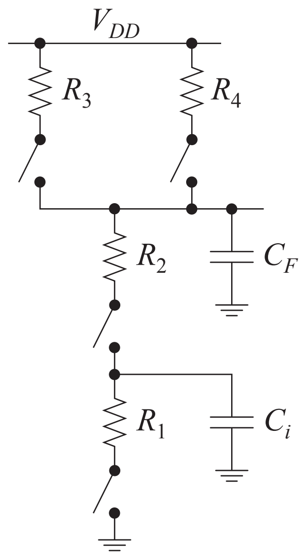
Check operation mode

$$V_{\min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(2.0 - 0.91 - 0.43, 1.0 - 0.91, 0.63\right) = V_{DS}$$

The MOSFET is linear.

3.

a) RC switch model



b) As we can see from equivalent RC model, the case in which both inputs transition go low ($A = 1 \rightarrow 0$, $B = 1 \rightarrow 0$) results in a smaller delay because of two R_p in parallel makes the total resistance to be $R_p/2$.

c) The reason for the different delay involves the internal node capacitance of the pull-down net (i.e. in the connection M_1—M_2). For the case in which $A = 1$ and B transitions from $1 \rightarrow 0$, the pull-up PMOS device only has to charge up the output node capacitance (M_2 is turned off). On the other hand for the case in which $B = 1$ and A transits from $1 \rightarrow 0$, the pull-up PMOS device has to charge both the output and the internal node capacitances, which slows down the transition.

4.

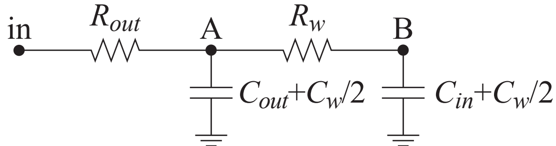
a) Estimate the output resistance R_{out} of the inverter

$$t_{inv} \approx 0.69 R_{out} C_{out} \Rightarrow R_{out} \approx \frac{t_{inv}}{0.69 C_{out}} \approx 10.1 \text{ k}\Omega$$

Estimate resistance R_w and capacitance C_w of the wire

$R_w = rL = 3.75\ \text{k}\Omega,\ C_w = cL = 5.5\ \text{pF}$

The delay can be estimated from e.g. a π model of the wire



Estimate the delay with the Elmore delay formula

$$t_{p1} \approx 0.69\left[R_{out}\left(C_{out} + \frac{C_w}{2} + C_{in} + \frac{C_w}{2}\right) + R_w\left(C_{in} + \frac{C_w}{2}\right)\right] \approx 46\ \text{ns}$$

b) The circuit with the repeater will consist of two sections where the resistance and capacitance of the wire are halved compared to a). This results in the delay estimation

$$t_{p2} \approx 2\cdot 0.69\left[R_{out}\left(C_{out} + \frac{C_w}{2} + C_{in}\right) + \frac{R_w}{2}\left(C_{in} + \frac{C_w}{4}\right)\right] \approx 42\ \text{ns}$$

5.

a) Propagate: $P_i = a_i \oplus b_i$

Generate: $G_i = a_i \cdot b_i$

Sum: $s_i = a_i \oplus b_i \oplus c_{i-1} = P_i \oplus c_{i-1}$

Carry bits ⇒ sum bits:

$s_0 = P_0 \oplus c_{in}$

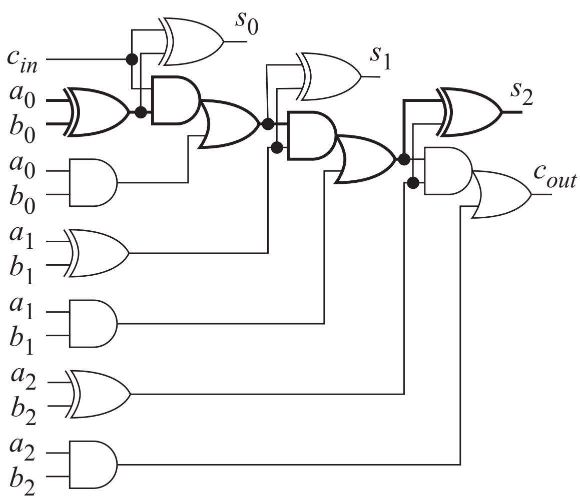
$c_0 = G_0 + P_0 c_{in} \Rightarrow s_1 = P_1 \oplus (G_0 + P_0 c_{in})$

$c_1 = G_1 + P_1 c_1 = G_1 + P_1(G_0 + P_0 c_{in}) \Rightarrow s_2 = P_2 \oplus [G_1 + P_1(G_0 + P_0 c_{in})]$

b) $c_{out} = G_2 + P_2 c_1 = G_2 + P_2[G_1 + P_1(G_0 + P_0 c_{in})] =$

$= a_2 b_2 + (a_2 \oplus b_2)\{a_1 b_1 + (a_1 \oplus b_1)[a_0 b_0 + (a_0 \oplus b_0)c_{in}]\}$

c) A schematic of the 3-bit CLA is shown on next page.



Computation of s_2 is slightly longer than c_{out} and hence critical
Propagation delay: t_p = 90+70+70+90 ps = 320 ps

6.

a) A property that measures the ease of observing the state of an internal circuit node at the circuit output.

b) A property that measures the ease of setting the state of an internal circuit node from the circuit input.

c) A collection of tricks and techniques that aims at increasing the observability and controllability, often tailored to a particular application.

d) A reconfiguration of many registers into a serial shift register. By this the internal register data can be read and written also in state machines, which are very hard to test from the circuit boundaries.

e) On-chip generation of test stimulus and analysis of response. This typically improves test time significantly compared with off-chip test generation.