Linköping Institute of Technology
Department of Electrical Engineering, Division of Integrated Circuits and Systems

# Exam TEN1 in TSTE86 Digital Integrated Circuits

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|---|---|
| **Time:** | Monday 22 October 2018, 14:00—18:00 |
| **Place:** | G32, G33, G34 |
| **Responsible teacher:** | Mark Vesterbacka, phone 013-281324 |
| **Allowed aid:** | Calculator |
| **Max score:** | 60 points |
| **Grades:** | 45 points for 5<br>35 points for 4<br>25 points for 3 |
| **Solutions:** | Posted on the course web |
| **Results:** | Posted through LADOK by 7 November 2018 |

1. The function $F = AB+AC$ shall be implemented in static CMOS logic. The complements to $A$, $B$, $C$ are *not* available.

   a) Implement the function with at most eight transistors. (5 p)

   b) Size all transistors so that the worst-case output resistance is the same as that of an inverter with an PMOS $W/L = 4$ and NMOS $W/L = 3$. (5 p)

2. A pseudo-NMOS inverter designed in 0.25 µm CMOS technology is shown in Figure 1. The supply voltage is 2.5 V and the output load is 100 fF. Channel length modulation may be neglected.

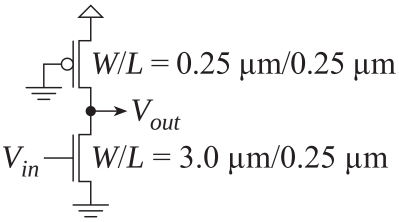


Figure 1. Pseudo-NMOS inverter.

   a) Calculate the output voltage levels $V_{OL}$ and $V_{OH}$. (5 p)

   b) Estimate $t_p$. (5 p)

3. The circuit in Figure 2 is supposed to realize the function $F(A, B, C) = A + BC$. However, the circuit does not work as intended.

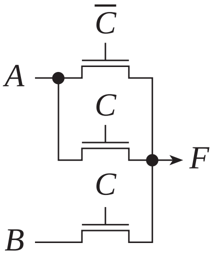


Figure 2. A faulty logic circuit.

   a) What type of logic has been used in this realization? (2 p)

   b) What is the problem with this circuit? (2 p)

   c) Redesign the gate so that the wanted function $F(A, B, C)$ is realized correctly. (6 p)

4. Consider a *static random-access memory* (SRAM) with full-VDD precharge of the bit-lines and sense amplifiers connected to the bit-lines.

   a) Draw the transistor schematic of a six-transistor CMOS SRAM cell. (3 p)

   b) Describe a write operation of the SRAM cell. (2 p)

   c) Describe a read operation of the SRAM cell. (2 p)

   d) Briefly discuss considerations in sizing the cell's MOSFETs. (3 p)

5. A pipelined datapath is shown in Figure 3. A register in the pipeline has the clock-to-output delay $t_{\text{c-q}} = 0.7$ ns, the set-up time $t_{\text{su}} = 0.5$ ns, and the hold time $t_{\text{hold}} = 0.4$ ns.

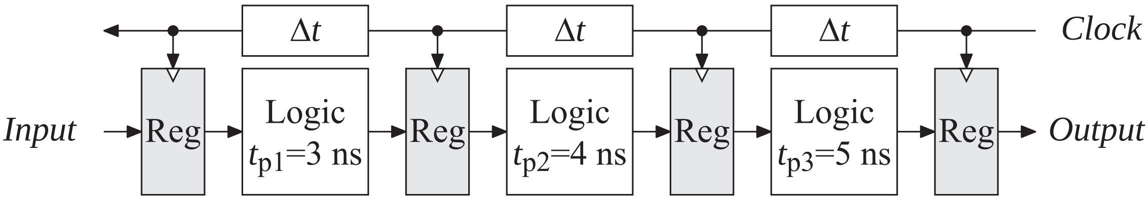


Figure 3. Pipelined datapath.

   a) What is the advantage of pipelining and what is the limitation of dividing a datapath into many pipelined stages? (3 p)

   b) What is the maximum throughput of the datapath if there is no clock skew, i.e. $\Delta t = 0$, and no clock jitter? (3 p)

   c) What is the minimum clock period of the datapath if there is a delay $\Delta t = 0.3$ ns between the registers and a clock jitter of at most 0.1 ns? (4 p)

6. Describe the steps of the semicustom design flow below with one or two sentences per step.

   a) Logic synthesis. (2 p)

   b) Floor planning. (2 p)

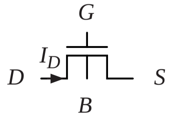
   c) Placement. (2 p)

   d) Routing. (2 p)

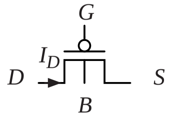
   e) Tape out. (2 p)

## Equations for the MOS transistor

NMOS



PMOS



**Definition of source (*S*) and drain (*D*)**

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

**Voltage notations**

$V_{GS} = V_G - V_S$, $V_{DS} = V_D - V_S$, $V_{SB} = V_S - V_B$, $V_{GT} = V_{GS} - V_T$

**Threshold voltage**

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

**Unified model**

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

**$V_{DSAT}$ dependency on channel length**

$V_{DSAT} = L\xi_c$

**Subthreshold region**

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

## Model parameters for 0.25 μm CMOS devices

**Parameters for drain current calculations**

| | $V_{T0}$ [V] | $\gamma$ [$\sqrt{\text{V}}$] | $V_{DSAT}$ [V] | $k'$ [$\mu$A/V$^2$] | $\lambda$ | $\Phi_F$ [V] |
|---|---|---|---|---|---|---|
| NMOS | 0.43 | 0.40 | 0.63 | 115 | 0.06 | –0.30 |
| PMOS | –0.40 | –0.40 | –1.00 | –30 | –0.10 | 0.30 |

**Parameters for capacitance calculations**

| | $C_{ox}$ [fF/$\mu$m$^2$] | $C_O$ [fF/$\mu$m] | $C_j$ [fF/$\mu$m$^2$] | $m_j$ | $\phi_b$ [V] | $C_{jsw}$ [fF/$\mu$m] | $m_{jsw}$ | $\phi_{bsw}$ [V] |
|---|---|---|---|---|---|---|---|---|
| NMOS | 6 | 0.31 | 2.0 | 0.50 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 6 | 0.27 | 1.9 | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

## Gate capacitance

**Overlap capacitance**

$C_{GSO} = C_{GDO} = C_{ox}x_dW = C_OW$

**Channel capacitance**

$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$

| Condition | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ |
|---|---|---|---|
| $V_{GTn} \le 0$, $V_{GTp} \ge 0$ | $C_{ox}WL$ | 0 | 0 |
| $V_{GTn} > 0$, $V_{GTp} < 0$, $\|V_{DS}\| \le \|V_{GT}\|$ | 0 | $C_{ox}WL/2$ | $C_{ox}WL/2$ |
| $V_{GTn} > 0$, $V_{GTp} < 0$, $\|V_{GT}\| \le \|V_{DS}\|$ | 0 | $2C_{ox}WL/3$ | 0 |

## Junction capacitance

**Junction capacitance as function of voltage**

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

**Average capacitance during transition from $V_1$ to $V_2$**

$$C_{eq} = K_{eq}C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

## Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

## Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

## Boolean algebra

**De Morgans' theorem**

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots,\qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

**Expansion in sum**

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

**Expansion in product**

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

## Transmission line

**Characteristic impedance**

$$Z_0 = \sqrt{l/c}$$

**Velocity of wave**

$$\upsilon = 1/\sqrt{lc}$$

**Reflection coefficient for a transmission line ($Z_0$) terminated by a load ($Z_L$)**

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

## Elmore delay

$P_i$ = "the path between node $0$ and $i$".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths $P_i$ and $P_j$".

$R_{ij}$ = "the sum of all resistances in $P_{ij}$".

Time constant from node $0$ to $i$: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

## Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where $k$ = "tapering factor", $N$ = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.