

Exercise 1

How is the propagation delay of a long wire scaled when the length of the wire is increased?

Exercise 2

In Figure 1 a static CMOS inverter is driving an identical inverter and an interconnect. The interconnect is assumed to be short in length and can be modeled as a lumped capacitor. The parasitic capacitances in the two inverters are dominated by the transistor capacitances. The input capacitance of the inverter is C_{in} , the output capacitance is C_{out} , and the interconnect capacitance is C_w . The propagation delay from the input of the first inverter to the input of the second is t_{p0} . The power supply voltage is $V_{DD} = 1.2$ V and the threshold voltage for the transistors is $|V_T| = 0.4$ V. Assume $C_{in} = C_{out} = C_0$ and $C_w = 3C_0$.

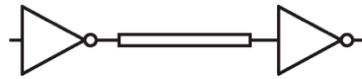


Figure 1. Inverter loaded with interconnect and an identical inverter.

- Estimate the relative change in dynamic power consumption when the transistor widths are reduced to half the original size, and voltage scaling is used to maintain the total propagation delay. Assume long transistor channels.
- Solve the problem in a) for a submicron process with $r = 1.5$. You may solve the numerically with, e.g., iteration.

Exercise 3

To estimate the delay in a given structure of interconnects one can use the Elmore delay which approximates the dominant time constant. A method for computing the Elmore delay of RC networks is described below.

- Let P_i denote the path between node 0 and i .
- Let $P_{ij} = P_i \cap P_j$ denote the common part of the paths P_i and P_j where P_j is the path between node 0 and i .
- Let R_{ij} be the sum of all resistances in P_{ij} , if $P_{ij} = \emptyset$ then $R_{ij} = 0$.

The dominating time constant from 0 and i can be written as:

$$\tau_{di} = \sum_{j=0}^n R_{ij} C_j$$

where n is the number of branches in the structure and C_j is the capacitance in each node. Calculate the Elmore delay from node 0 to node 4 in the H-tree shown in Figure 2 on next page.

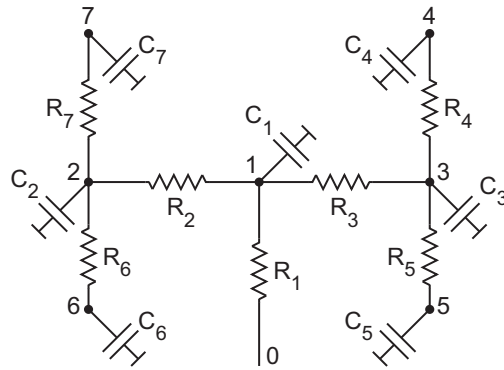


Figure 2. RC network.

Exercise 4

- a) How can clock skew be used to achieve a larger time margin?
- b) What may happen if the clock skew is too large?

Exercise 5

An H tree is often used to obtain a low-skew clock distribution in a synchronous digital system. An H tree with 16 nodes uniformly distributed over a square die with edge length d is shown to the left in Figure 3. The horizontal as well as the vertical distance between two nodes is $d/4$. Another clock tree that can be implemented in technologies that allow 45 degree routing is shown to the right. We will call it an X tree. Both trees are driven by a tapered clock buffer at the root. The capacitance of a leaf node is C_{node} . All wires have the same thickness t_{wire} and an area capacitance of C_{wire} . Fringing capacitance and interwire capacitance are neglected.

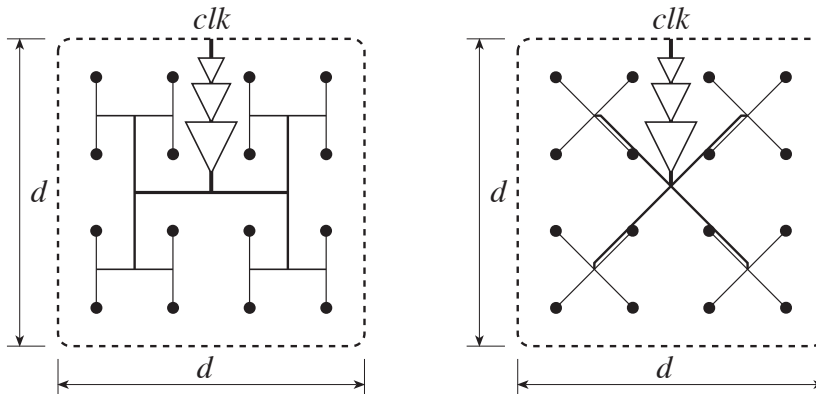


Figure 3. H tree (left) and X tree with 45 degree angles (right).

- a) Consider the energy dissipation caused by the clock tree, i.e. excluding the load at the nodes. How large will the relative energy savings be if the X tree may be used instead of the H tree? Assume that the wires are designed with the same width w_{const} .
- b) Solve the previous problem a) using a tapered clock tree instead. Assume that the trees are designed so that the maximum current density is equal in all wires, the width of the wire connecting a leaf node is w_{leaf} , and $C_{node} \gg C_{wire}dw_{leaf}$.

Exercise 6

- a) Determine an expression of the total wire length of a square shaped H tree where the number of nodes are $N = 4^n$, n is an integer. Figure 4 shows the structure of a square shaped H tree consisting of 16 nodes.

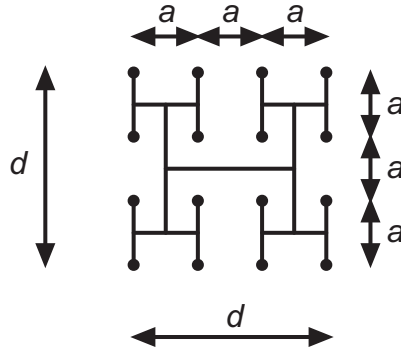


Figure 4. Square shaped H tree.

- b) In several CMOS technologies it is possible to route in 45 degrees. Determine the minimum required wire length for 16 nodes located as in Figure 4.
- c) Determine a π -model of the H tree in Figure 4. Approximate each branch with a π -model of order one. All interconnections are of the same width w and the capacitance of an interconnection can be calculated as $C = k_1 l$ where k_1 is a constant and l is the length of the interconnection. R_{\square} is known. The capacitances of the clock inputs of the interconnected gates is assumed to be equal.
- d) Is it reasonable to use a constant wire width in a large clock tree?
- e) How is it possible to achieve almost zero skew in a Steiner tree?

Exercise 7

Clock gating is useful to reduce the power consumption by turning off the clock signal.

- a) Describe advantages and disadvantages with using clock gating.
- b) What will be the implications of using clock gating in a system based on dynamic circuits?
- c) Assume that we use a simple clock gating scheme where an AND-gate is used for gating the clock. Draw the waveforms of clock, enable, and output clock to highlight the possible timing problem of changing the enable signal.
- d) Suggest an alternative (sequential) circuit to solve the problem in c). Illustrate the validity of your solution by drawing the waveforms as in c).

Exercise 8

An asynchronous and a synchronous N -bit binary counter are shown in Figure 5. Estimate the relative dynamic power consumption of the asynchronous counter compared with the synchronous counter. Do only consider the power used to drive the clock nodes and the counter output. Neglect the power consumed in the internal logic paths. Assume that the capacitance of the clock node of one D flip-flop is C_c and the capacitance of one output bit q_i is C_o . Both counters are glitch free and use the same clock frequency and power supply voltage.

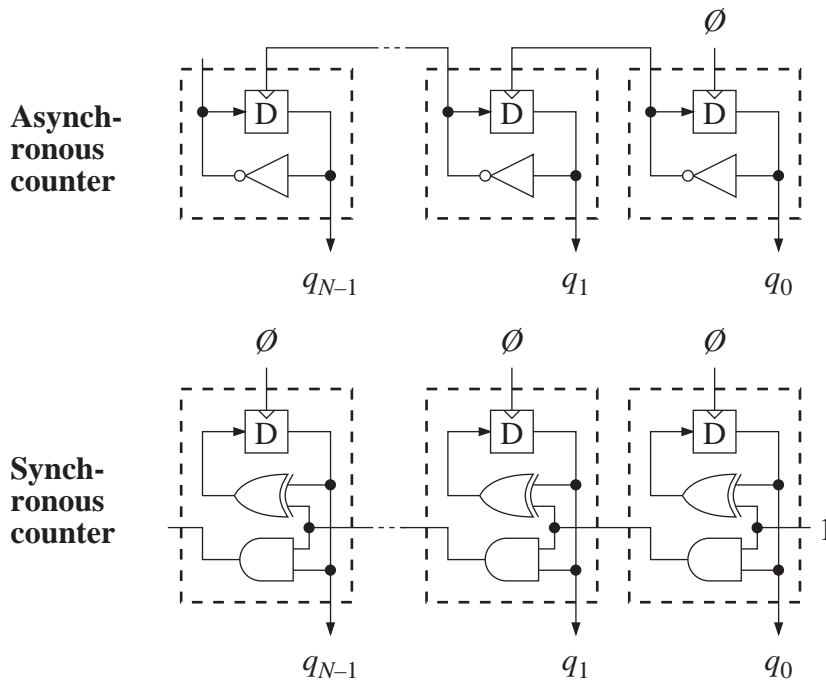


Figure 5. Two binary counters.

Exercise 9

A ripple-carry adder should be implemented for use in an asynchronous circuit.

- Sketch how the adder can be implemented on block level with dual-rail encoding of the carry. Describe the internal carry signals.
- Describe advantages and disadvantages of using dual-rail encoding compared with a handshaking based on fixed delay.
- How may the asynchronous adder save power compared with the corresponding synchronous circuit?

Solution 1

The wire resistance is in proportion to the length L . The wire (area and fringing) capacitance is in proportion to L . Hence, the wire propagation delay (assuming an ideal input) is in proportion to L^2 .

Solution 2

- a) $t_{p0} = (C_{in} + C_{out} + C_w)V_{DD0}/I_0$ where I_0 is the average current during charging and discharging. The new propagation delay after doubling the widths of the transistors and using voltage scaling can be expressed as $t_{p1} = (0.5C_{in} + 0.5C_{out} + C_w)V_{DD1}/I_1$.

We set $t_{p0} = t_{p1}$ and use $I_0 = k(V_{DD0} - |V_T|)^r$ and $I_1 = 0.5k(V_{DD1} - |V_T|)^r$.

$$\frac{(C_{in} + C_{out} + C_w)V_{DD0}}{k(V_{DD0} - |V_T|)^r} = \frac{(0.5C_{in} + 0.5C_{out} + C_w)V_{DD1}}{0.5k(V_{DD1} - |V_T|)^r}$$

$$r = 2 \Rightarrow \frac{5V_{DD0}}{k(V_{DD0} - |V_T|)^2} = \frac{8V_{DD1}}{k(V_{DD1} - |V_T|)^2}$$

Solving the equation yields solutions $V_{DD1} \approx 0.10$ V and $V_{DD1} \approx 1.55$ V, where the latter is the proper solution.

Relative dynamic power consumption

$$\frac{P_1}{P_0} = \frac{\left(\frac{1}{2}C_{in} + \frac{1}{2}C_{out} + C_w\right)V_{DD1}^2}{(C_{in} + C_{out} + C_w)V_{DD0}^2} = \frac{4V_{DD1}^2}{5V_{DD0}^2} \approx 1.34$$

The dynamic power consumption is *increased* 34% using the smaller transistors.

- b) Using the same approach as in a) with $r = 1.5 \Rightarrow$

$$\frac{5V_{DD0}}{(V_{DD0} - |V_T|)^{1.5}} = \frac{8V_{DD1}}{(V_{DD1} - |V_T|)^{1.5}} \Rightarrow \frac{V_{DD1} - |V_T|}{V_{DD0} - |V_T|} = \left(\frac{8V_{DD1}}{5V_{DD0}}\right)^{2/3} \Rightarrow$$

$$\frac{V_{DD1} - |V_T|}{V_{DD1}^{2/3}} = K, \text{ where } K = \frac{8^{2/3}(V_{DD0} - |V_T|)}{5^{2/3}V_{DD0}^{2/3}}$$

Iteration formula

$$V_{DD1}^{[i+1]} = K(V_{DD1}^{[i]})^{2/3} + |V_T|, V_{DD1}^{[0]} = 1.55 \text{ V}, i = 0, 1, \dots \Rightarrow V_{DD1} \approx 1.87 \text{ V}$$

Relative dynamic power consumption

$$\frac{P_1}{P_0} = \frac{4V_{DD1}^2}{5V_{DD0}^2} \approx 1.94$$

The dynamic power consumption is *increased* 94% using the smaller transistors

Solution 3

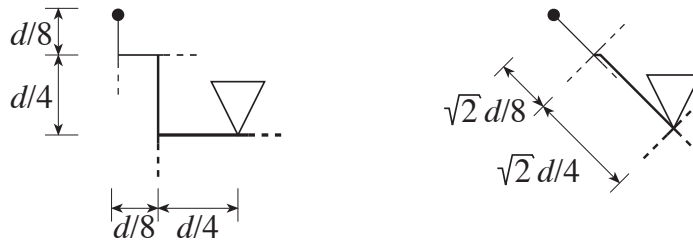
$$t_{d4} = \sum_{j=0}^7 R_{ij}C_j = R_1C_1 + R_1C_2 + R_1C_6 + R_1C_7 + (R_1 + R_3)C_3 + (R_1 + R_3)C_5 + (R_1 + R_3 + R_4)C_4$$

Solution 4

- a) $T_{clk} \geq T_{cq} + t_{logic} + t_{su} - \delta$ gives $T_{clk} \geq T_{cq} + t_{logic} + t_{su} - \delta + t_{margin}$. A positive skew results in a larger time margin. From where is the extra time margin (δ) borrowed?
- b) $t_h \leq T_{cq,cd} + t_{logic,cd} - \delta$ may be violated causing malfunction.

Solution 5

- a) Length of a path in the H tree (left) and X tree (right)



Capacitance of the H tree

$$C_H = \left(2 \cdot \frac{d}{4} + 4 \cdot \frac{d}{4} + 8 \cdot \frac{d}{8} + 16 \cdot \frac{d}{8} \right) w_{const} C_{wire} = 4.5dw_{const} C_{wire}$$

Capacitance of the X tree

$$C_X = \left(4 \cdot \frac{\sqrt{2}d}{4} + 16 \cdot \frac{\sqrt{2}d}{8} \right) w_{const} C_{wire} = 3\sqrt{2}dw_{const} C_{wire}$$

Relative savings by using X tree

$$\left| \frac{E_X - E_H}{E_H} \right| = \frac{4.5 - 3\sqrt{2}}{4.5} \approx 5.7\%$$

- b) Width of a path in the H tree (left) and X tree (right)



Capacitance of the H tree

$$C_H = \left(2 \cdot \frac{d}{4} \cdot 8w_{leaf} + 4 \cdot \frac{d}{4} \cdot 4w_{leaf} + 8 \cdot \frac{d}{8} \cdot 2w_{leaf} + 16 \cdot \frac{d}{8} \cdot w_{leaf} \right) C_{wire} = 12dw_{leaf} C_{wire}$$

Capacitance of the X tree

$$C_X = \left(4 \cdot \frac{\sqrt{2}d}{4} \cdot 4w_{leaf} + 16 \cdot \frac{\sqrt{2}d}{8} \cdot w_{leaf} \right) C_{wire} = 6\sqrt{2}dw_{leaf} C_{wire}$$

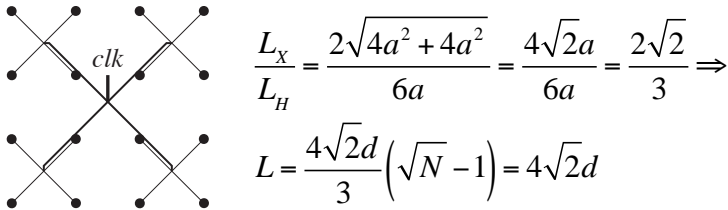
Relative savings by using X tree

$$\left| \frac{E_X - E_H}{E_H} \right| = \frac{12 - 6\sqrt{2}}{12} \approx 29\%$$

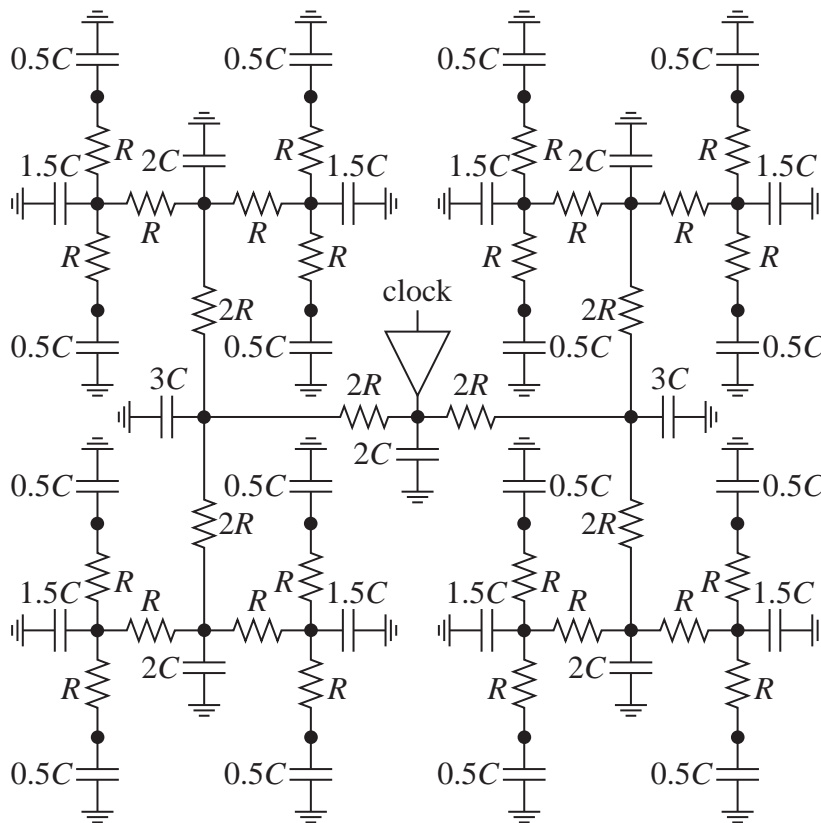
Solution 6

a)
$$L = \sum_{i=0}^{n-1} 6a2^i = 6a(2^n - 1) = 6a(4^{0.5n} - 1) = 2d(\sqrt{N} - 1) = \{N = 16\} = 6d$$

b) Replace the H structures with X structures



c) Model of the H tree with $C = k_1 2^{0.5} d$, $R = R_{\square} \cdot 2^{0.5} d / (3w)$



d) No. The wires should be sized. The lower limit of the wire width of a branch is determined by the current through that branch.

e) By inserting buffers with different delays.

Solution 7

a) Advantages and disadvantages with using clock gating:

- + Large dynamic power savings in gated mode
- Clock skew need to be considered during design
- Circuit overhead

- b) When the registers are dynamic the current state will eventually be lost due to parasitics. This leads to that the state must be stored if it should be used later on.
- c) Main problem is that the clock is enabled while it is high. This leads to a too short time between adjacent rising edges (assuming positive-edge triggered flipflops).
- d) Introduce a latch that only propagates a high enable signal to the AND-gate if the input clock is low.

Solution 8

Clock power of the N -bit asynchronous counter

$$P_{a,clk} = \sum_{i=0}^{N-1} 2^{-i} f_{clk} C_c V_{DD}^2 = (2 - 2^{1-N}) f_{clk} C_c V_{DD}^2 = 2(1 - 2^{-N}) f_{clk} C_c V_{DD}^2$$

Clock power of the N -bit synchronous counter

$$P_{s,clk} = \sum_{i=0}^{N-1} f_{clk} C_c V_{DD}^2 = N f_{clk} C_c V_{DD}^2$$

Output power of the counters

$$P_o = \sum_{i=0}^{N-1} a_i f_{clk} C_o V_{DD}^2 = \sum_{i=0}^{N-1} 2^{-i-1} f_{clk} C_o V_{DD}^2 = (1 - 2^{-N}) f_{clk} C_o V_{DD}^2$$

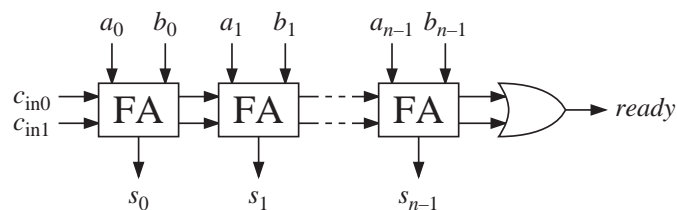
Relative power dissipation

$$\frac{P_a}{P_s} = \frac{P_{a,clk} + P_o}{P_{s,clk} + P_o} = \frac{2(1 - 2^{-N})C_c + (1 - 2^{-N})C_o}{NC_c + (1 - 2^{-N})C_o} = \frac{2C_c + C_o}{\left(\frac{N}{1 - 2^{-N}}\right)C_c + C_o}$$

Solution 9

- a) Represent internal carry with two bits and three states

c_1	c_0	state
0	0	not ready
0	1	carry = 0
1	0	carry = 1
1	1	unused



- b) Advantages are that no safety margin is needed in the delay since the actual completion is output, and the completion signal is data-dependent yielding a better average delay. Disadvantages are the extra overhead in circuitry and more nodes that switches that are needed to produce the dual-rail signals, and it is not possible to reuse a conventional RCA in the design.
- c) It is easier to design a system with an adaptive supply voltage since there is no clock speed that needs to be adjusted. The clock net does not consume power. It is more easy to implement sleep functionality since there is no clock to stop.