Exercise 1

The two parallel interconnects in Figure 1 are separately driven by one buffer each. The parasitic capacitances of the interconnects can be modeled as in Figure 2.
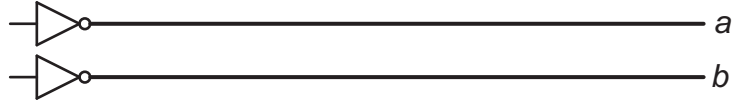

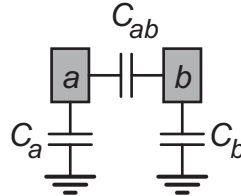
Figure 1. Two parallel interconnects driven by buffers.

Figure 2. Model of the two interconnects.

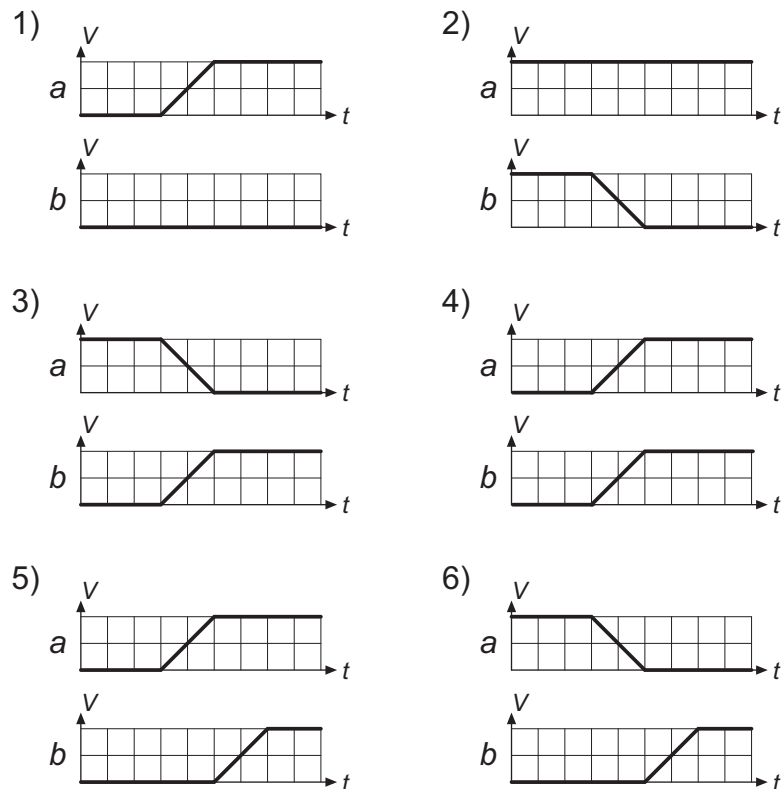a) Determine the dissipated energy due to C_a, C_b, and C_{ab} for the six scenarios shown in Figure 3.

Figure 3. Six scenarios.

b) Why do the energy dissipation in scenario 4 and 5 differ?

c) Why do the energy dissipation in scenario 3 and 6 differ?

d) The two buffers are explicit shown in Figure 4. Determine where the energy is dissipated for the time slots $t_1 < t < t_2$ and $t_2 < t < t_3$, respectively.
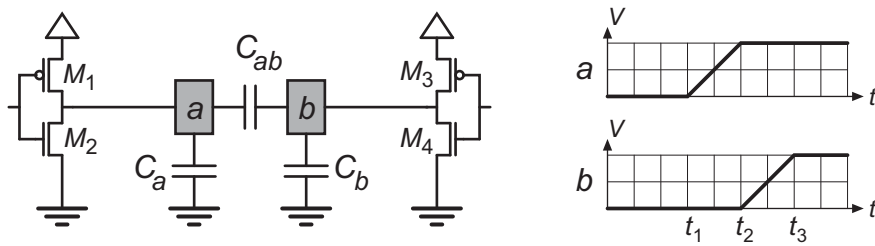

Figure 4. Two interconnects driven by buffers.

e) Determine the amount of energy which is taken from the power supply in the scenarios above (Figure 3). Why do these results differ from the results in a)?

Exercise 2

a) Encode the sequence <0, 1, 2, 3, 4, 5, 6, 7, 0> with both Gray and Binary code. Compare the number of transitions.

b) Determine the number of transitions in a general counting sequence. For a large counter, what is the ratio between the two different encodings?

Exercise 3

A specific control unit cycles through the states shown in Figure 5. By simulation over a large number of different input signals the probability for change of state has been estimated. The probabilities for the different branches is also shown in Figure 5.

a) What is the average number of logic transitions/cycle using the state coding of the FSM in Fig. 5? (one cycle = "A complete cycle from state 000 and back to state 000")

b) Suggest another state coding with fewer transitions/cycle.
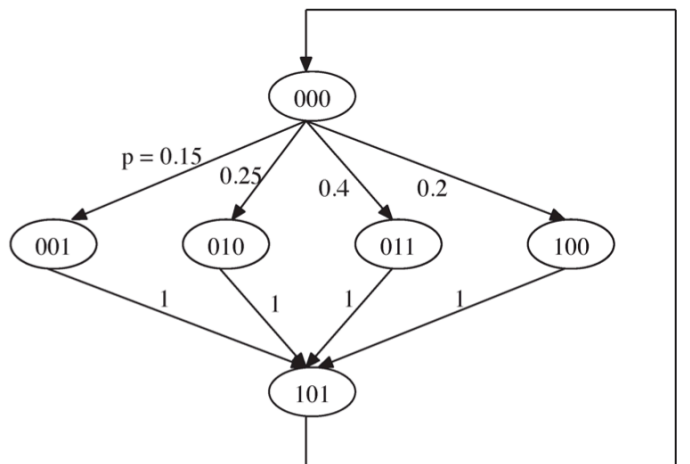

Figure 5. State transition diagram with transition probability.

Exercise 4

In Figure 6 the behavior of a state machine is shown. Before coding the states a statistical measurement of the two input signals, x2 and x1 is performed. The following results where found: The input value of 00 is found in 10% of the cases, 01 in 40%, 10 in 30% and 11 in 20%. How should the states be coded to minimize switching nodes in the resulting circuit? Assume that the input signals are independent of the current state.
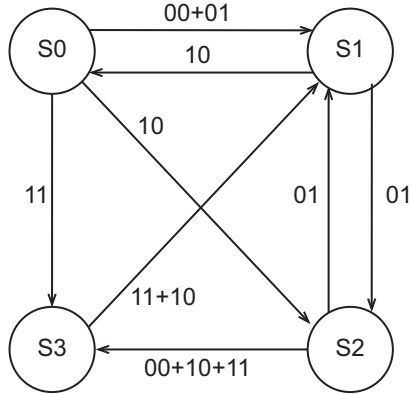

Figure 6. State machine.

Exercise 5

A circuit realizing a simple finite state machine is shown in Figure 7. The input signals a, b, and c are random and have equal probability of being low or high. They are further glitch free and make their transitions simultaneously.
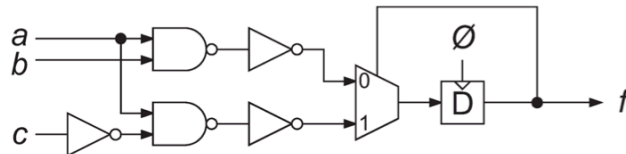

Figure 7. Simple state machine.

a) Determine the transition activity in the output node f. Also, determine the probability of f being high. Neglect glitches and motivate your assumptions.

b) In what nodes are there a risk of glitches? Motivate your answer.

c) Redesign the circuit for a reduced power consumption. Identify the nodes that may have glitches in your redesigned circuit. Motivate your decisions.

Exercise 6

a) What is bus invert encoding and how can it be used to lower the power consumption of a bus?

b) Encode the data sequence 0010, 1101, 0001, 0000, 1100, 0101, 1011 with bus invert encoding. Let the bus invert signal be "0" for the first data.

Exercise 7

a) In a logic function the input signal a has a lower transition activity than the other input signals (b, c, d, and e). Rewrite the logic function f with the use of Shannon expansion. Let a be the load-enable signal.

$$f = \bar{a}\bar{b}c + \bar{a}b\bar{c} + ac\bar{d}e + ac\bar{e}$$

b) Sketch the architecture of the circuit, where you show explicit which circuit the input and output signals are connected to. (Hint: Use registers with a load-enable input)

Exercise 8

a) What is the essence of precomputational logic?

b) Consider an n-bit comparator. How can precomputational logic be used to reduce power consumption?

Exercise 9

In a circuit the complement of each signal is required. A model of a bus consisting of $2(N+1)$ bit lines is shown in Figure 8(a) ($N \geq 1$). The transition activity of x_j ($0 \leq j \leq N$) is α. The bit lines x_j and x_k are independent when $j \neq k$. The probability of x_j being equal to one is one half (the signal may be correlated). The clock frequency is f. Assume that all signals have the same rise and fall time and that all transitions starts simultaneously.
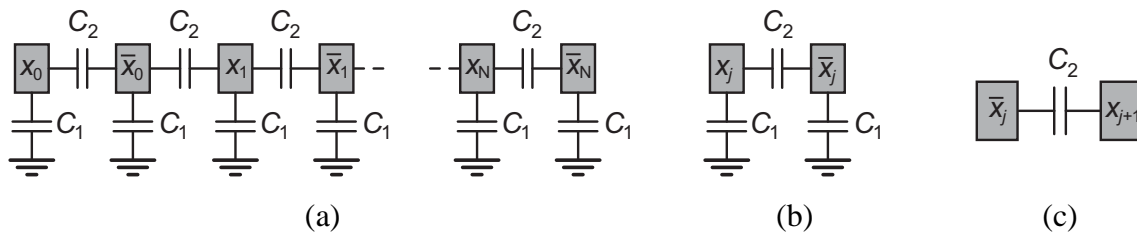

Figure 8. (a) *Bus consisting of 2(N+1) bit lines,* (b) *two complementary bit lines, and* (c) *two uncorrelated bit lines.*

a) Calculate the power consumption for the complementary bit lines shown in Fig. 8 (b).

b) Calculate the power consumption due to the parasitic capacitance C_2 for the two uncorrelated bit lines in Figure 8 (c).

c) Use the results from a) and b) to calculate the power consumption for the bus in Figure 8 (a).

d) The signal order is changed to: $x_0, x_1, \overline{x_0}, \overline{x_1}, x_2, x_3, \overline{x_2}, \overline{x_3}, \ldots, x_{N-1}, x_N, \overline{x_{N-1}}, \overline{x_N}$. Calculate the power consumption.

e) Calculate the power consumption in c) and d) when $C_1 = 50$ fF, $C_2 = 100$ fF, $N = 15$, $f = 1000$ MHz, $\alpha = 0.25$ and $V_{DD} = 1.2$ V. Compare the results.

Solution 1

a)

1) $\dfrac{(C_a + C_{ab})V_{DD}{}^2}{2}$ 　　2) $\dfrac{(C_b + C_{ab})V_{DD}{}^2}{2}$ 　　3) $\dfrac{(C_a + C_b + 4C_{ab})V_{DD}{}^2}{2}$

4) $\dfrac{(C_a + C_b)V_{DD}{}^2}{2}$ 　　5) $\dfrac{(C_a + C_b + 2C_{ab})V_{DD}{}^2}{2}$ 　6) $\dfrac{(C_a + C_b + 2C_{ab})V_{DD}{}^2}{2}$

c) The voltage over the capacitance C_{ab} is never changed in scenario 4.

c) In case 3, C_{ab} is charged from V_{DD} to $-V_{DD}$ where all charges ($2C_{ab}V_{DD}$) are taken from the power supply voltage. In case 6, C_{ab} is first charged from V_{DD} to 0 V where no charges are taken from the power supply voltage. Then, C_{ab} is charged from 0 V to $-V_{DD}$ where the charges ($C_{ab}V_{DD}$) are taken from the power supply voltage.

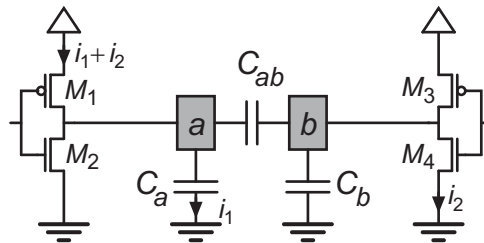d) For $t_1 < t < t_2$, the energy is dissipated in M_1 and M_4.

Figure 9. Time slot $t_1 < t < t_2$.

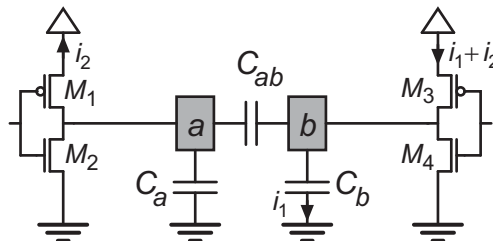For $t_2 < t < t_3$, the energy is dissipated in M_1 and M_3.

Figure 10. Time slot $t_2 < t < t_3$.

e)

1) $(C_a + C_{ab})V_{DD}{}^2$ 　　　2) $C_{ab}V_{DD}{}^2$ 　　　3) $(C_b + 2C_{ab})V_{DD}{}^2$

4) $(C_a + C_b)V_{DD}{}^2$ 　　　5) $(C_a + C_b + C_{ab})V_{DD}{}^2$ 　6) $(C_b + C_{ab})V_{DD}{}^2$

In a, the energy which is dissipated as heat is considered.
In e, the energy which is taken from the power supply is considered.
(These two values of energy may differ since energy may be stored in the circuit.)

Solution 2

a)

Binary	No. transitions (from previous state to current)	Gray	No. transitions
000	**3**	**000**	**1**
001	**1**	**001**	**1**
010	**2**	**011**	**1**
011	**1**	**010**	**1**
100	**3**	**110**	**1**
101	**1**	**111**	**1**
110	**2**	**101**	**1**
111	**1**	**100**	**1**

Table 1. Binary code and Gray code respectively.

When counting from a complete cycle from 0 to 0, binary code makes 14 transitions and Gray code makes only 8 transitions.

b) Consider a counter of magnitude 2^n.

Gray code: 2^n transitions.

Binary code: $2^n \sum_{j=0}^{n-1} 2^{-j} = 2^{n+1} - 2$ transitions.

Binary code/Gray code: $\dfrac{2^{n+1} - 2}{2^n} \approx 2.0$ for n larger than 5.

Solution 3

a) Using the original state coding the average number of transitions/cycle T_{avg} can be found as $T_{avg} = 0.15 \times 4 + 0.25 \times 6 + 0.4 \times 6 + 0.2 \times 4 = 5.3$ transitions/cycle.

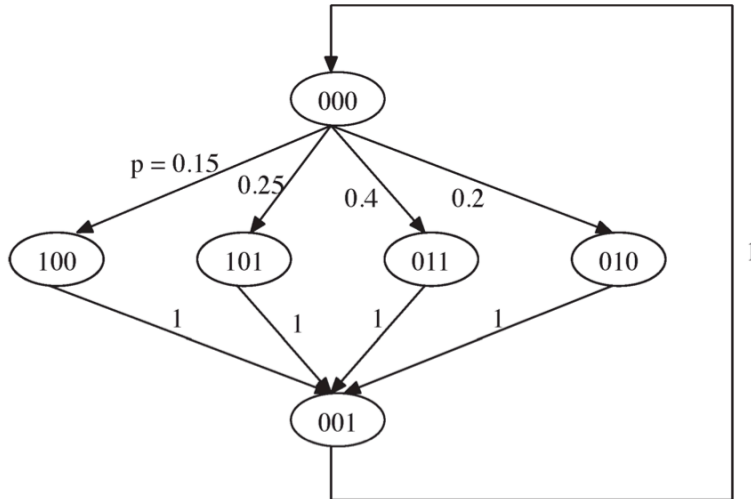b) Another coding is shown on next page.

Figure 11. An FSM with another state coding.

The new value is given by $T_{avg} = 0.15 \times 4 + 0.25 \times 4 + 0.4 \times 4 + 0.2 \times 4 = 4$

Solution 4

To minimize switching power the most likely switching between states must be determined. The probability for different signal changes in all stages give the probability graph shown in Figure 12. The probability that the circuit is in a certain state can be computed by setting up the following relations.

$p(S0) = 0.0p(S0)+0.3p(S1)+0.0p(S2)+0.0p(S3)$
$p(S1) = 0.5p(S0)+0.3p(S1)+0.4p(S2)+0.5p(S3)$
$p(S2) = 0.3p(S0)+0.4p(S1)+0.0p(S2)+0.0p(S3)$
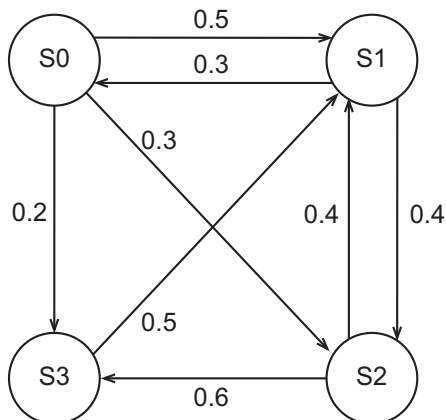$p(S3) = 0.2p(S0)+0.0p(S1)+0.6p(S2)+0.5p(S3)$
$p(S0)+p(S1)+p(S2)+p(S3) = 1$

Figure 12. Probability graph.

Solving (exclude for example $p(S1)$) yields:

$p(S0) = 0.120$
$p(S1) = 0.400$
$p(S2) = 0.196$
$p(S3) = 0.283$

Now the probability of a switching between two states can be determined

$p(S0–S1) = 0.5p(S0)+0.3p(S1) = 0.180$
$p(S0–S2) = 0.3p(S0) = 0.036$
$p(S0–S3) = 0.2p(S0) = 0.024$
$p(S1–S2) = 0.4p(S1)+0.4p(S2) = 0.239$
$p(S1–S3) = 0.5p(S3) = 0.142$
$p(S2–S3) = 0.6p(S2) = 0.118$

The most common switching is between S1 and S2 and thus this change of state should consume a minimum of power i.e. as few changing bits as possible. The second most common switching is between S0 and S1, and should therefore also be coded so that the haming distance is small in between.
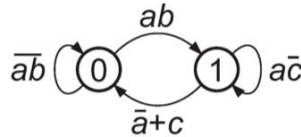
Examples of codings
S0 = 10, S1 = 00, S2 = 01, S3 = 11 or
S0 = 100, S1 = 000, S2 = 001, S3 = 010 (requires one more memory element, less activity in the bits representing the state, but the load for the clock signal is higher)

Solution 5

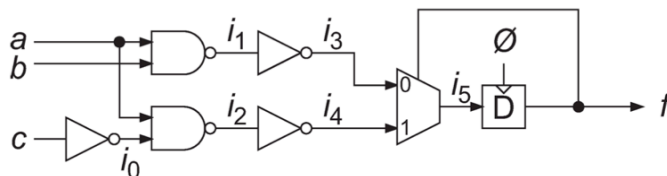a) The circuit realizes the state machine

where the probability of a state output is obtained from the following relations

$$\begin{vmatrix} p(0) + p(1) = 1 \\ p(1) = P_{ab}p(0) + P_{\overline{ac}}p(1) \\ P_{ab} = P_{\overline{ac}} = 1/4 \end{vmatrix} \Rightarrow \begin{cases} p(0) = 3/4 \\ p(1) = 1/4 \end{cases}$$

The transition activity becomes $\alpha = p(0)p(1) + p(1)p(0) = 3/8$ and the probability of an $f = 1$ is $p(1) = 1/4$.

b) Consider the following labeling i_j of the internal nodes

Node i_1 should be glitch free since the inputs to the preceeding NAND gate are glitch free. Node i_2 may on the other hand have glitches, since the inputs to the preceeding NAND gate have different delays. The inverters may propagate but do not add glitches, hence nodes i_0 and i_3 should be glitch free while there is a risk of glitches in node i_4. The multiplexer both have differently delayed inputs and may propagate node i_4 to its output, making glitches possible at the output i_5. Even if i_3 and i_4 are without glitches, there is still a risk of glitches in node i_5. For example, consider the case where $f=0$, $i_3=1$, $i_4=0$. In the next state, f will change value from 0 to 1. If i_4 change value to 1 in the same clock cycle, there is a risk of a glitch due to that the i_4 can be propagated to i_5 before the value of i_4 is settled. The circuit output f is on the other hand synchronized with the clock by a D flip-flop, and should hence be glitch free.

c) The inversion of i_1 and i_2 could be shared by postponing the inversion until after the multiplexer operation and, if the timing of f allows, until after the D flip-flop operation. In the original circuit there are three inverters; one with transition activity 1/2, one with transition activity 3/8, and one with transition activity 3/8 + transition activity due to glitches. In the redesigned circuit there are two inverters; one with transition activity 1/2, and one with transition activity 3/8. Hence, the redesigned circuit will have one glitchy node less. The redesigned circuit is shown in the figure below.
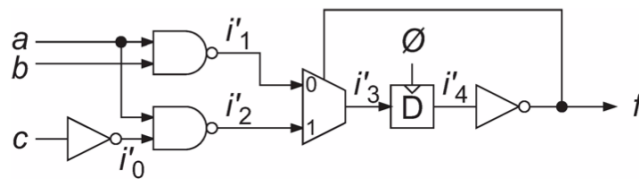
In the redesigned circuit, the nodes i'_2 and i'_3 may have glitches.

Solution 6

a) See corresponding paper.

b) Original: 0010, 1101, 0001, 0000, 1100, 0101, 1011
   With bus-invert encoding: 0 0010, 1 0010, 1 1110, 1 1111, 1 0011, 1 1010, 0 1011

Solution 7
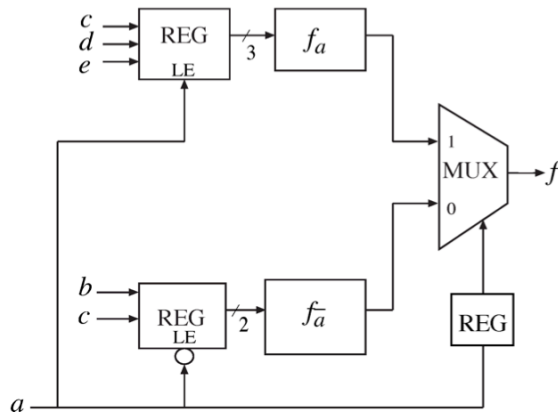
a) $f = \bar{a}(\bar{b}c + b\bar{c}) + a(c\bar{d}e + \bar{c}e)$

   We define two new functions $f_{\bar{a}} = \bar{b}c + b\bar{c}$, $f_a = c\bar{d}e + \bar{c}e$.

   The function f can now be written as $f = \bar{a}f_{\bar{a}} + af_a$.

b) The architecture of the new circuit is shown below.

Architecture of the new circuit

Solution 8

a) Make a smaller computation first where the result is used to decide if further computation is necessary and which resources that should be used.

b) For example, check the two most significant bits of the input signals. Only if they do not differ, the other n–2 bits need to be considered.

Solution 9

a) $P_a = \alpha f V_{DD}^2 (C_1 + 2C_2)$

b) Let $P(a, b)$ denote the probability for state (a, b).
Let $P((a, b) \rightarrow (c, d))$ denote the probability for state (c, d) in the next clock cycle given that the state is (a, b) in the current clock cycle.

$P(0, 0) = 1/4$ *Dissipated energy*

$P((0, 0) \rightarrow (0, 0)) = (1 - \alpha)^2$ $E = 0$

$P((0, 0) \rightarrow (0, 1)) = (1 - \alpha)\alpha$ $E = \dfrac{C_2 V_{DD}^2}{2}$

$P((0, 0) \rightarrow (1, 0)) = \alpha(1 - \alpha)$ $E = \dfrac{C_2 V_{DD}^2}{2}$

$P((0, 0) \rightarrow (1, 1)) = \alpha^2$ $E = 0$

$P(0, 1) = 1/4$ *Dissipated energy*

$P((0, 1) \rightarrow (0, 0)) = \alpha(1 - \alpha)$ $E = \dfrac{C_2 V_{DD}^2}{2}$

$P((0, 1) \rightarrow (0, 1)) = (1 - \alpha)^2$ $E = 0$

$P((0, 1) \rightarrow (1, 0)) = \alpha^2$ $E = 2C_2 V_{DD}^2$

$P((0, 1) \rightarrow (1, 1)) = \alpha(1 - \alpha)$ $E = \dfrac{C_2 V_{DD}^2}{2}$

$P((a, b) \rightarrow (c, d)) = P((a, b) \rightarrow (c, d))$

$$P_b = f\left\{ \frac{1}{4}\left(2\alpha(1-\alpha)\frac{C_2 V_{DD}^2}{2}\right) + \frac{1}{4}\left(2\alpha(1-\alpha)\frac{C_2 V_{DD}^2}{2} + 2\alpha^2 C_2 V_{DD}^2\right) + \right.$$

$$\left. \frac{1}{4}\left(2\alpha(1-\alpha)\frac{C_2 V_{DD}^2}{2}\right) + \frac{1}{4}\left(2\alpha(1-\alpha)\frac{C_2 V_{DD}^2}{2} + 2\alpha^2 C_2 V_{DD}^2\right)\right\}$$

$$P_b = (\alpha(1-\alpha) + \alpha^2)f C_2 V_{DD}^2 = \alpha f C_2 V_{DD}^2$$

c) $P_c = (N+1)P_a + NP_b$

$P_c = \{(N+1)(C_1 + 2C_2) + NC_2\}\alpha f V_{DD}^2 = \{(N+1)C_1 + (3N+2)C_2\}\alpha f V_{DD}^2$

d) $P_d = \{(N+1)C_1 + (2N+1)C_2\}\alpha f V_{DD}^2$

e) $P_c = \{(N+1)C_1 + (3N+2)C_2\}\alpha f V_{DD}^2$

$P_c = \{16 \cdot 50 \cdot 10^{-15} + 47 \cdot 100 \cdot 10^{-15}\}0.25 \cdot 10^9 \cdot 1.2^2 \approx 1.980\,\text{mW}$

$P_d = \{(N+1)C_1 + (2N+1)C_2\}\alpha f V_{DD}^2$

$P_d = \{16 \cdot 50 \cdot 10^{-15} + 31 \cdot 100 \cdot 10^{-15}\}0.25 \cdot 10^9 \cdot 1.2^2 \approx 1.404\,\text{mW}$

With the given parameters 29% power is saved in d) compared to c).

Power may be saved if the complements of the signals are internally created in the receiver. Another way to reduce the power consumption is to increase the distance between the interconnects, which results in a decreased C_2 and a slightly increased C_1. In a certain 0.35 μm CMOS-process a bus consisting of 16 uncorrelated bit lines, a power reduction of 36% could be achieved when the distance between the interconnects were increased from 0.7 μm to 1.4 μm. The cost is the additional area, but on the other hand, the propagation delay of the bus decreases (why?).