Exercise 1

Why is there a need for low power designs in microelectronics?

Exercise 2

In Figure 1, a capacitor is shown. The energy of a nonmoving particle in an electric field is $E = qV$, where q is the electrical charge and V is the electrical potential.

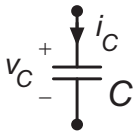


Figure 1. Capacitor.

a) What is the relation between the current I_C and the voltage V_C of the capacitor?

b) Calculate the energy that is stored in the capacitor for $V_C = V_1$.

c) How much energy is taken from the power supply when the capacitor is charged from 0 V to V_{DD}?

d) For how many Ah can a capacitor of 1 F supply a voltage larger than 0.8 V when the initial voltage of the capacitor is 1.4 V? Neglect leakage currents in the capacitor. (Note that 1 F is a large value of capacitance)

Exercise 3

Due to limited gain for static CMOS logic, the minimum supply voltage V_{min} that can be used for a static CMOS inverter is about 0.1 V at room temperature 300 K.

a) What is the fundamental limit on circuit gain?

b) Given that V_{min} is proportional to the temperature expressed in K, how much would V_{min} increase if the temperature is raised to 70°C?

Exercise 4

A square wave with a period of T is connected to an inverter.

a) Derive an expression for the average dynamic power consumption $P_{d,avg}$ due to charging and discharging of a capacitive output load C.

b) How much will the power consumption decrease if the power supply voltage is reduced to the half of the original power supply voltage?

c) How is the propagation time of the inverter affected if the power supply voltage is reduced? Assume saturation region while discharging and find an expression that the drain current is in proportion to.

Exercise 5

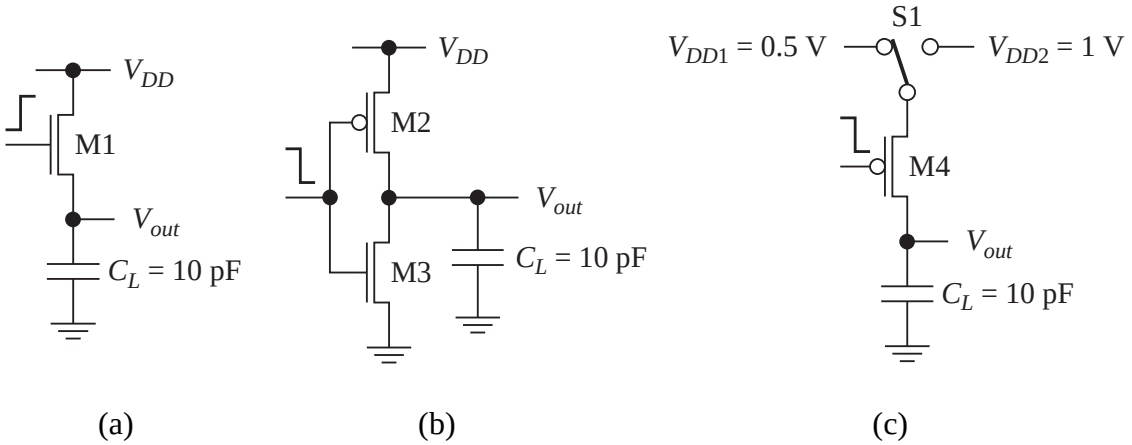
A large load capacitor C_L = 10 pF needs to be charged to 1 V using three different circuits given below. Assume that the capacitor is fully discharged initially and ignore leakage currents. Also assume that the input pulses are ideal and ignore short circuit currents. For each case, compute the following:

i. Derive the expression and determine the total energy taken from the supply during the charging process.

ii. Proportion of this energy (in percentage) that gets stored in the capacitor.

iii. Proportion of the energy that is dissipated during the process. Also indicate where this energy is dissipated.

iv. The efficiency of the charging process.



(a) (b) (c)

Figure 2. (a) *NMOS charging a capacitor*, (b) *CMOS inverter charging a capacitor, and* (c) *PMOS charging a capacitor in two steps.*

a) An NMOS transistor charging the capacitor from a 1.5 V supply, shown in Figure 2 (a). The transistor M1 turn off due to a voltage $V_{out} \geq 1$ V.

b) A CMOS inverter working at 1 V supply as shown in Figure 2 (b).

c) A two-level charging circuit as shown in Figure 2 (c). Assume that the ideal switch S1 is initially connected to a 0.5 V supply. After CL charges to 0.5 V, S1 switches to a 1 V supply.

Exercise 6

The transition activity α of a signal is the average number of "0 to 1" and "1 to 0" transitions in one clock cycle. The signals *a* and *b* below are both outputs of registers.

a) Determine the transition activity α_a of a bit *a* which is random where P(a = 1) = 0.5.

b) Determine the transition activity α_b of a bit *b* which is random where P(b = 1) = p_1.

c) The transition activity α_a calculated in a) is often seen as an upper limit of the transition activity of data bits in digital circuits. Give two examples of signals which may have a higher transition activity.

Exercise 7

Consider a static CMOS XOR gate $F = a \oplus b \oplus c$ where $P(a = 1) = 0.55$, $P(b = 1) = 0.23$ and $P(c = 1) = 0.62$.

a) Determine the probability that the output *F* is 1.

b) Determine the transition activities $\alpha_{F(01)}$, $\alpha_{F(10)}$ and α_F.

Exercise 8

Consider a two input NAND gate (in static CMOS) where the parasitic capacitances are modelled with the capacitors C_A and C_B on the inputs (*A*, *B*) and one capacitor C_F on the output (*F*). The input signals are glitch free and random. $P(A) = P(B) = 0.5$.

a) Determine the transition activities α_A, α_B and α_F.

b) Determine the switch activity *a* of the circuit.

c) Determine the switched capacitance.

d) Determine the power consumption assuming a power supply voltage of V_{DD}.

Solution 1

Portable equipment as laptops, cellular phones, handhelds, hearing aids etc. requires low weight, small dimensions, and long operation time between charging the battery. Low power designs are needed to allow the product to be power supplied by a relatively small and light weighted battery. If the power consumption for a microprocessor is lowered it may be possible to use a cheaper package of the chip and it may also be possible to use a less expensive power supply with smaller maximal current. With a lower power consumption the need for cooling aids is lower which may result in lower manufacturing costs. With a lower power consumption the temperature of the chip can be lowered which gives a longer life time of the circuit.

Solution 2

a) $C = Q/V_C$, $I = dQ/dt \Rightarrow i_c = dQ/dt = d(CV_C)/dt = CdV_C/dt$
$i_c = CdV_C/dt$

b) $dE = VdQ = \frac{Q}{C}dQ$, $E = \int_0^{Q_1} \frac{Q}{C}dQ = \frac{{Q_1}^2}{2C} = \frac{CV_1^2}{2}$

c) $E = CV_{DD}^2$

d) $1\text{Ah} = 3600\text{As} = 3600\frac{\text{Coulomb}}{\text{s}}\text{s} = 3600\text{Coulomb}$

$V_0 = 1.4V$, $V_1 = 0.8V$

$Q_0 = CV_0$

$Q_1 = CV_1$

$Q_0 - Q_1 = C(V_0 - V_1) = 1 \cdot 0.6\ \text{Coulomb} = \frac{0.6}{3600}\text{Ah} \approx 0.167\text{mAh}$

Solution 3

a) The gain of a gate has to be larger than one to restore the logic levels in a cascade of circuits.

b) The minimum voltage is given by $V_{DD,\min} = \gamma\frac{kT}{q} = k_0 T$

Assuming room temperature ≈ 300 K $\Rightarrow k_0 = \frac{V_{DD,\min}}{T} = \frac{0.1}{300}$ V/K

At 70°C we have $T = 343$ K $\Rightarrow V_{DD,\min} = \frac{0.1}{300} \cdot 343\ \text{V} \approx 0.114\ \text{V}$

Hence the minimum supply voltage requirement increases with 14 mV.

Solution 4

a) $C = Q/v_C$ and $i = dQ/dt$ gives us the current i_c in Figure 3:

$i_c = dQ/dt = d(Cv_C)/dt = Cdv_C/dt$

Joule's law for thermal power: $p = vi$ (The power is dissipated in the transistors)

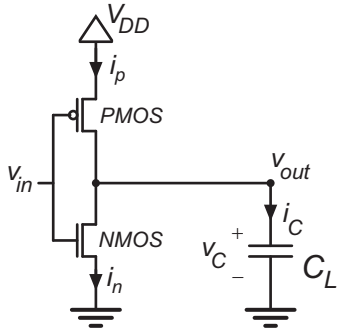


Figure 3. CMOS inverter with a capacitive load.

Assuming that the output capacitance is fully charged and fully discharged during one period T and that the input signal is ideal (no short circuit currents), and that $i_c = i_p$ when $0 \le t < T/2$ and $i_c = -i_n$ when $T/2 \le t \le T$. We get, since $i_p dt = C_L dv_{out}$ and $i_n dt = -C_L dV_{out}$.

$$P_{d,\,avg} = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^{T/2}(V_{DD} - v_{out})i_p dt + \frac{1}{T}\int_{T/2}^{T} v_{out} i_n dt$$

$$= \frac{1}{T}\int_0^{V_{DD}} C_L(V_{DD} - v_{out})dv_{out} + \frac{1}{T}\int_{V_{DD}}^{0} (-C_L v_{out})dv_{out}$$

$$= \frac{C_L}{T}\left(\left[V_{DD}v_{out} - \frac{v_{out}^2}{2}\right]_{v_{out}=0}^{v_{out}=V_{DD}} + \left[-\frac{v_{out}^2}{2}\right]_{v_{out}=V_{DD}}^{v_{out}=0}\right) = \frac{C_L}{T}V_{DD}^2$$

b) 75%

c) Assuming saturation region of the charging (or discharging) transistor, the propagation delay is in proportion to $V_{DD}/(V_{DD}-V_t)^2$.

Solution 5

a-i) The energy taken from the supply during the charging process is

$$E_{supply} = \int_0^{\infty} V_{DD} i_D dt$$

where i_D is the current taken from supply, which is same as the capacitor current given by $i_C = C_L dV_{out}/dt$. Therefore

$$E_{supply} = \int_0^{\infty} V_{DD} C_L \left(\frac{dV_{out}}{dt}\right) dt = V_{DD} C_L \int_0^{1\text{V}} dV_{out} = V_{DD} C_L \cdot 1\text{V} = 15\text{ pJ}$$

a-ii) The energy that is stored in the capacitor is

$$E_C = \int_0^{\infty} V_{out} i_C dt = \int_0^{\infty} V_{out} C_L \left(\frac{dV_{out}}{dt} \right) dt = C_L \int_0^{1\text{V}} V_{out} dV_{out} = C_L \left[\frac{V_{out}^2}{2} \right]_0^{1\text{V}} = 5 \text{ pJ}$$

a-iii) The energy is dissipated in transistor M1. Dissipated amount is

$$E_{diss} = E_{supply} - E_C = 10 \text{ pJ}$$

a-iv) Charging efficiency is $E_C / E_{supply} \approx 0.33 = 33\%$

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b-i) The energy taken from the supply is

$$E_{supply} = \int_0^{\infty} V_{DD} C_L \left(\frac{dV_{out}}{dt} \right) dt = V_{DD} C_L \int_0^{1\text{V}} dV_{out} = V_{DD} C_L \cdot 1\text{V} = 10 \text{ pJ}$$

b-ii) The energy that is stored in the capacitor is

$$E_C = \int_0^{\infty} V_{out} i_C dt = C_L \int_0^{1\text{V}} V_{out} dV_{out} = 5 \text{ pJ}$$

b-iii) The energy is dissipated in transistor M2. Dissipated amount is

$$E_{diss} = E_{supply} - E_C = 5 \text{ pJ}$$

b-iv) Charging efficiency is $E_C / E_{supply} \approx 0.5 = 50\%$

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c-i) Assume first phase of charging finishes at time t_1. The energy taken from the 0.5 V supply during this phase is

$$E_{supply1} = \int_0^{t_1} V_{DD1} C_L \left(\frac{dV_{out}}{dt} \right) dt = V_{DD1} C_L \int_0^{0.5\text{V}} dV_{out} = V_{DD1} C_L \cdot 0.5\text{V} = 2.5 \text{ pJ}$$

Assume second phase of charging finishes at time t_2. The energy taken from the 1 V supply during this phase is

$$E_{supply2} = \int_{t_1}^{t_2} V_{DD2} C_L \left(\frac{dV_{out}}{dt} \right) dt = V_{DD2} C_L \int_{0.5\text{V}}^{1\text{V}} dV_{out} = V_{DD2} C_L \left(1\text{V} - 0.5\text{V} \right) = 5 \text{ pJ}$$

Total energy taken from both supplies is

$$E_{supply} = E_{supply1} + E_{supply2} = 7.5 \text{ pJ}$$

c-ii) The energy that is stored in the capacitor is

$$E_C = \int_0^{t_2} V_{out} i_C dt = C_L \int_0^{1\text{V}} V_{out} dV_{out} = 5 \text{ pJ}$$

c-iii) The energy is dissipated in transistor M4. Dissipated amount is

$$E_{diss} = E_{supply} - E_C = 2.5 \text{ pJ}$$

c-iv) Charging efficiency is $E_C / E_{supply} \approx 0.66 = 66\%$

Solution 6

a) $\alpha_a = 0.5$

b) The sum of the probabilities of the scenarios $(b_j, b_{j+1}) = (0, 1)$ and $(b_j, b_{j+1}) = (1, 0)$ is the answer.
$P\{(b_j, b_{j+1}) = (0, 1)\} = (1 - p_1)p_1$
$P\{(b_j, b_{j+1}) = (1, 0)\} = p_1(1 - p_1)$
$\alpha_b = 2p_1(1 - p_1)$

c) The transition activity of a clock signal is 2. The transition activity of LSB of a binary coded counter is 1 (if it counts clock cycles).

Solution 7

a) $P(F) = P(a)(P(b)P(c) + P(b)P(c)) + P(a)(P(b)P(c) + P(b)P(c)) = 0{,}4935$

b) $\alpha_{F(01)} = (1 - P(F))P(F)$, $\alpha_{F(10)} = P(F)(1 - P(F))$, $\alpha_F \approx 0.500$

Solution 8

a) $\alpha_A = \alpha_B = 0.5$, $\alpha_F = 3/8$

b) $a = \sum_i \alpha_{i(01)} C_i / \sum_i C_i = \frac{1}{16} \frac{(4C_A + 4C_B + 3C_F)}{(C_A + C_B + C_F)}$

c) $C_{sw} = \frac{(4C_A + 4C_B + 3C_F)}{16}$

d) $P = \frac{(4C_A + 4C_B + 3C_F)}{16} f V_{DD}^2$