Interleaving of a First In First Out (FIFO) register

Description

This document is intended to serve as a manual for laboratory 2 exercises of the course TSTE85, low power electronics, provided at the division of Integrated Circuits and Systems, dept. of Electrical Engineering, Linköping University.

Contents

1 SPICE/HSPICE

SPICE stands for Simulation Program with Integrated Circuit Emphasis. SPICE or SPICE-like tools gives the most accurate simulation results, but they require huge computer time when large integrated circuits are simulated. In this laboratory, the hierarchical description of circuits is used to describe the FIFO register.

1.1 Hierarchical description

A simple example with an inverter chain is shown in Fig. 1 together with the SPICE list description.

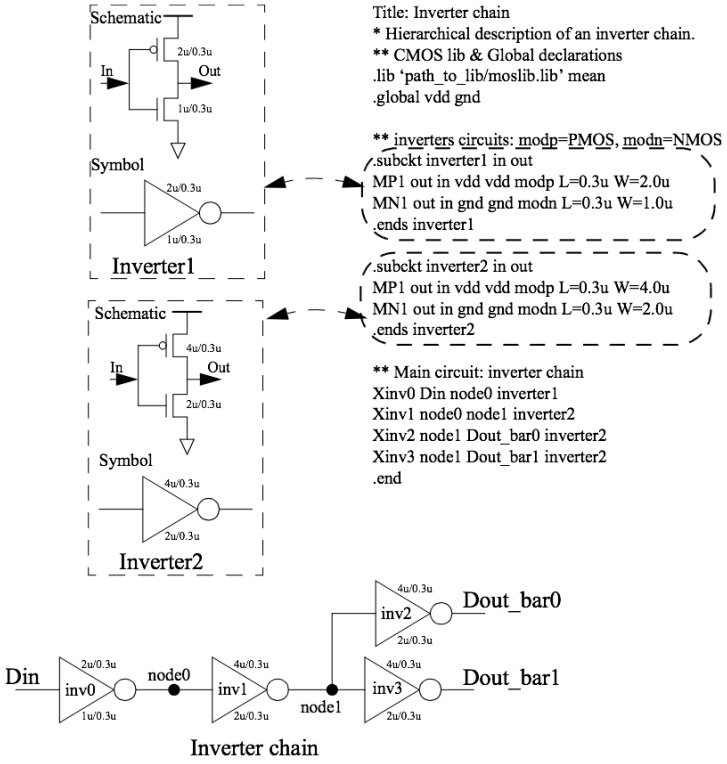


Figure 1: SPICE netlist example.

2 Setting up the laboratory

1. Open a terminal window and start by logging onto the server naum via the intermediate server ssh with the commands

   ssh -X ssh.edu.liu.se
   ssh -X naum.ad.liu.se

2. Set up your working directory and copy the needed files:

   ```
   cd TSTE85
   mkdir lab2
   cd lab2
   ```

   Place your own `My_Cells.sp` in this directory.

   ```
   cp -r /coop/e/eks/course/TSTE85/lab2/files/VoltageScaling .
   cp /coop/e/eks/course/TSTE85/lab2/files/cfg .
   cp /coop/e/eks/course/TSTE85/lab2/files/fifo* .
   cp /coop/e/eks/course/TSTE85/lab2/files/test* .
   ```

3. Load the synopsys module:

   ```
   module load synopsys
   ```

3 FIFO design with interleaving

Interleaving is a way to increase the throughput. Consider an algorithm with two independent sequential processes P1 and P2, the completion time can be written as $T_{\text{comp}} = T_{\text{P1}} + T_{\text{P2}}$, where T_{P1} and T_{P2} are the execution times for process P1 and P2, respectively. The throughput can be increased by alternating the inputs to two processors as illustrated in Fig. 2. With two process elements, the throughput can be increased by a factor of two.

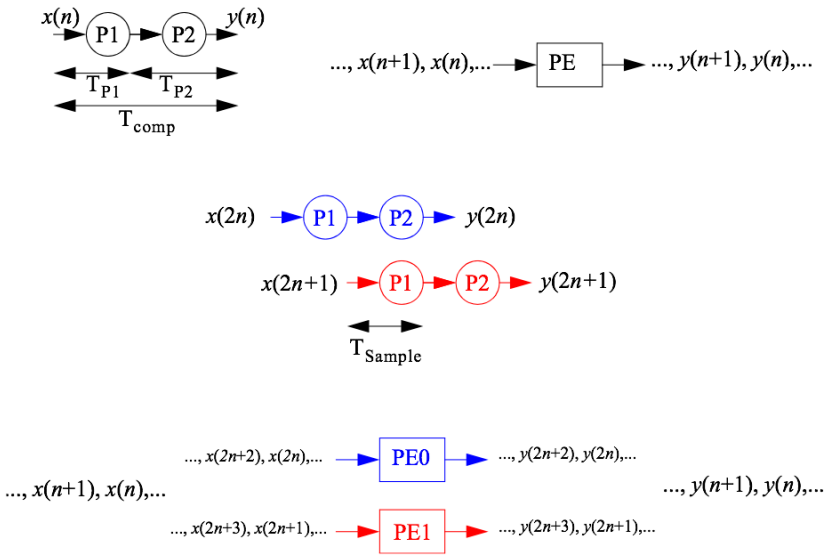


Figure 2: Interleaving.

In this laboratory, you are going to construct a FIFO (First In First Out) register with a delay depth of 64 and a word length of 1 bit. The straightforward way to implement the FIFO is to use 64 serial-coupled D flip-flops. With interleaving the data stream is divided into several data streams which are executed in parallel.

4 Preparations

In this laboratory, four different cases will be tested:

- Serial-coupled 64-D flip-flops.
- Two serial-coupled 32-D flip-flops (Interleaving with factor of 2).
- Four serial-coupled 16-D flip-flops (Interleaving with factor of 4).
- Eight serial-coupled 8-D flip-flops (Interleaving with factor of 8).

4.1 SPICE netlists

A sub circuit for a D flip-flop is given in `/coop/e/eks/course/TSTE85/lab2/files/Cells.sp` (see Appendix A). First and last row of the SPICE netlist for this sub circuit are shown below.

```
.subckt DFF CLK D Q VDD VGND
...
...
.ends DFF
```

The first word after `".subckt"` is the name of the sub circuit. The rest of the first row gives the input signals (CLK, D), the output signal (Q) and the power supply (VDD, VGND). The netlist of the sub circuit ends with ".ends DFF".

You must write four netlists (see section 4.1.1) in a SPICE file before the start of the laboratory. The top-level circuit is illustrated in Fig. 3. The template file `/coop/e/eks/course/TSTE85/lab2/files/My_Cells.sp` can be found in Appendix B. Copy this file and fill in the missing parts. A copy of the file must be handed in to the laboratory assistant by email. Deadline and further information of the names are found on the course web page.

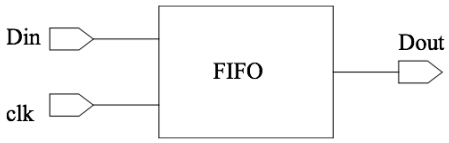


Figure 3: The I/O ports for the FIFO.

4.1.1 Instructions for writing the SPICE netlists

1. First, write a SPICE netlist for a sub circuit `DFF_8` consisting of 8 DFFs in series. Then write a netlist for sub circuit `DFF_8x8` consisting of 8 parallel `DFF_8` with the input signals `Din0, Din1, Din2, ..., Din7`. We give you some help to get started:

   The sub circuit `DFF_8` can be written as:
   (All "?" must be substituted...)

   ```
   .subckt DFF_8 CLK Din Dout VDD VGND

   X_DFF0 CLK Din Q0 VDD VGND DFF
   X_DFF1 CLK Q0  Q1 VDD VGND DFF
   X_DFF2 CLK ?   ?  VDD VGND DFF
   ```

```
X_DFF3 CLK ?   ?  VDD VGND DFF
X_DFF4 CLK ?   ?  VDD VGND DFF
X_DFF5 CLK ?   ?  VDD VGND DFF
X_DFF6 CLK ?   ?  VDD VGND DFF
X_DFF7 CLK ? Dout VDD VGND DFF

.ends DFF_8
```

In sub circuit `DFF_8` we use the sub circuit DFF. The names of the instances of the sub circuits must start with an x(X). For an example, `X_DFF0` is the name of the first D flip-flop (DFF) in the chain of 8 D flip-flops. The data input of `X_DFF0` is Din which is also the input of the sub circuit `DFF_8`. The output Q0 of the first D flip-flop is connected to the input of the next D flip-flop `X_DFF1`.

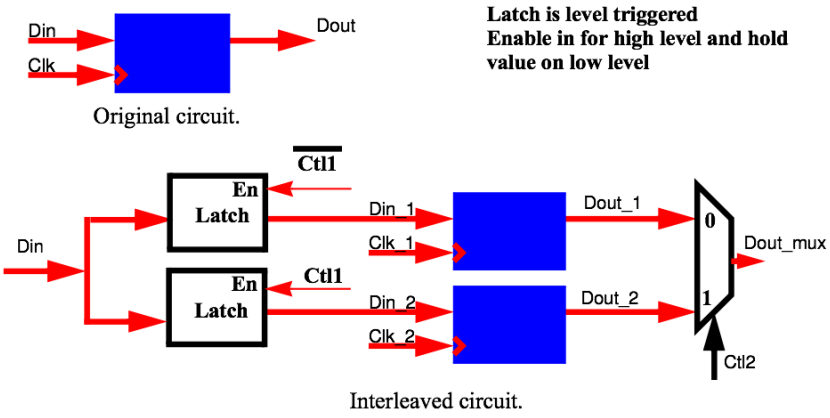
Hints for `DFF_8x8`:
(the plus sign (+) is used to continue a row)

```
.subckt DFF_8x8 CLK Din0 Din1 Din2 Din3 Din4 Din5 Din6 Din7
+ Dout0 Dout1 Dout2 Dout3 Dout4 Dout5 Dout6 Dout7 VDD VGND

X_DFF_80 CLK ? ? ?   ?    DFF_8
X_DFF_81 ?   ? ? ?   ?    ?
.
.
.
X_DFF_87 ?   ? ? VDD VGND DFF_8

.ends DFF_8x8
```

2. First, write a SPICE netlist for a sub circuit `DFF_16` consisting of 2 `DFF_8` in series. Use the `.subckt` command to define `DFF_16`. Then write a netlist for sub circuit `DFF_16x4` consisting of 4 parallel `DFF_16` with the input signals Din0, Din1, Din2, Din3 and the output signals Dout0, Dout1, Dout2, Dout3.
3. First, write a SPICE netlist for a sub circuit `DFF_32` consisting of 2 `DFF_16` in series. Then write a netlist for sub circuit `DFF_32x2` consisting of 2 parallel `DFF_32` with the input signals Din0 and Din1.
4. Write a SPICE netlist for a sub circuit `DFF_64` consisting of 2 `DFF_32` in series with the input signal Din.

4.2 Interleaving

We interleave a circuit `A` with a factor of 2. `A_1` and `A_2` are identical to `A`. Determine the signals: `Din_1`, `Din_2`, `Dout_1`, `Dout_2`, `Clk_1`, `Clk_2`, `Ctl1`, and `Ctl2`. **Sketch the waveforms!**



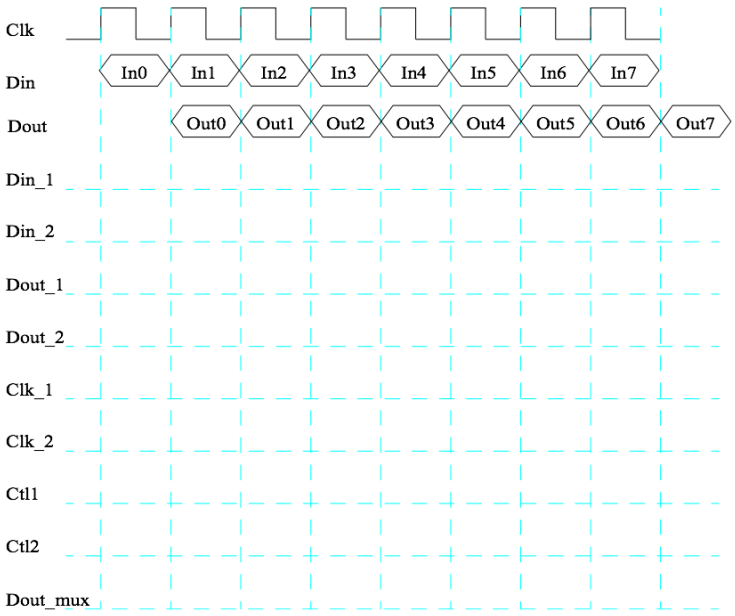


Figure 4: Exercise on interleaving.

A copy of this page is found at the end of this manual.
The page must be handed in to the laboratory assistant.
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5 Power estimation using Nanosim

Here you shall simulate the power consumption of a FIFO for four different cases of architectures. The first case is the original FIFO consisting of 64 D flip-flops in series where the sample rate is 100 Msamples/s and the clock frequency is 100 MHz. The other cases are interleaved versions of the original FIFO (see Table 1).

5.1 Extremely Correlated input data

The four cases below all have extremely correlated input data.
Case A, Din is a data signal with the pattern: 01010101010101010101...
Case B, Din is a data signal with the pattern: 00110011001100110011...
Case C, Din is a data signal with the pattern: 000011110000111100001111...
Case D, Din is a data signal with the pattern: 00000000111111110000000011111111...

1. Which are the frequencies of the corresponding square waves that can represent the data for the respective case? (Hint: What is the period of the different data signals?)

   Case A Case B Case C Case D
   ---

2. Which clock frequencies should be used internally when the interleaving factor is 2, 4 and 8, respectively?

   ---

3. Assume that Din is divided into two streams Din0 and Din1. Write the patterns of the two data streams for the different cases of input data. Also determine the frequency a squarewave should have, to represent each data stream. Hint: The data stream in case A can be represented by a 50 MHz squarewave.

   Case A

   Din0

   Din1

   Case B

   Din0

   Din1

   Case C

   Din0

   Din1

   Case D

   Din0

   Din1
   ---

4. Assume that Din is divided into four data streams din0, din1, din2, din3. Write the patterns of the four data streams for the different cases of input data. Also note the corresponding frequency of the respective data signals.

   Case A

   Din0

   Din1

   Din2

   Din3

   Case B

   Din0

   Din1

   Din2

   Din3

   Case C

   Din0

   Din1

   Din2

   Din3

   Case D

   Din0

   Din1

   Din2

   Din3

   The following files should be used together with Nanosim.

   ```
   fifo_1x64dff.sp
   fifo_2x32dff.sp
   fifo_4x16dff.sp
   fifo_8x8dff.sp
   ```

   You must do some changes in each file for (almost) each case! Hint: Use the previous pages. Make sure that the right circuit is simulated with the right input signal(s).

   With the command below, the average power supply current can be found for the 64 D flips-flops in

series:

```
nanosim -n fifo_1x64dff.sp -c cfg -t 4000
```

Fill in the power consumption in Table 1:

Table 1: Power consumption

Data rate	**Din-Case**	64 D flip-flops	2 x 32 D flip-flops	4 x 16 D flip-flops	8 x 8 D flip-flops
100	**A**				
100	**B**				
100	**C**				
100	**D**				

Considering the last alternative, i.e., interleaving with a factor 8, why is the power consumption smaller in case C than in case D?

5.2 Random input data

The data files test1.vec, test2.vec, test3.vec, and test4.vec contains random input data which were generated with Matlab. Use a sampling frequency of 100 MHz and simulate all alternatives. Note that the data input in the SPICE-file must here be disabled (use a star * for each row) since test vectors are used. Fill in your results in Table 2.

Example:

```
nanosim -n fifo_1x64dff.sp -nvec test1.vec -c cfg -t 4000
```

(Look into the test1.vec, test2.vec, test3.vec, and test4.vec files to determine which one to use in which case)

Table 2: Power consumption for random data

	64 D flip-flops	2 x 32 D flip-flops	4 x 16 D flip-flops	8 x 8 D flip-flops
Power consumption				

Note: The throughput must be maintained.

5. How is the power consumption affected by interleaving?

5.3 FIFO-register with a computation block

Voltage scaling is an efficient method to reduce the power consumption. The basic idea is to reduce the supply voltage as much as possible without violating the throughput requirement.

Now we consider a case where the supply voltages are the same for the FIFO register and a computation block. The computation block is placed in the FIFO register. The critical path is through the computation block and one register. The propagation delay in the critical path is 8 ns for $V_{\mathrm{dd}} = 3.3$ V. The throughput should fulfill 100 Msamples/s. When the FIFO register is interleaved, the computation block is interleaved with the same factor. What is the lowest supply voltage (with one decimal precision) that meets the throughput requirement for the different cases of interleaving?

To answer this question we will use circuit simulation results generated using HSPICE-simulations. Here the circuit is implemented in the AMS 0.35 μm process. Use CosmosScope to display results from the HSPICE-simulation. Start CosmosScope from the terminal window:

```
scope &
```

Select File/Open/Graphs..., select the file ./VoltageScaling/graph.def, and click open. A graph containing three curves will appear as in Fig. 5. Adjust the windows in size so that you see all the curves. In the lower most curve the power supply voltage (myvdd) can be seen. In the middle curve we see how the power consumption scales when the power supply voltage is reduced. In the upper most curve you see how the propagation delay scales with the supply voltage. Both the propagation delay and the power consumption curves are normalized to 1 for $V_{\mathrm{dd}} = 3.3$ V.

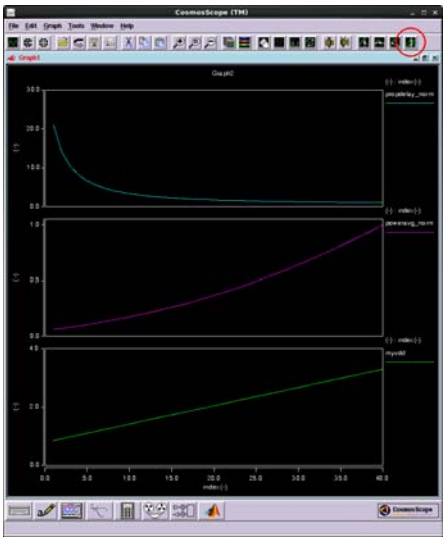


Figure 5: CosmoScope window.

Click on the x-axis labeled index (-), and then click on the "Vertical Marker Measurement" button (see Fig. 5). Now you should see a cursor that you can grab and move along the x-axis.

6. How much would the propagation delay be increased if V_{dd} is reduced from $V_{dd} = 3.3$ V to $V_{dd} = 1.65$ V?

   ----

7. Consider the case where the original power supply voltage is $V_{dd} = 3.3$ V and the propagation delay can be increased with 10%. What should the new power supply voltage be in order to save power?

   ----

8. As mentioned above a computation block is placed in the FIFO register and the critical path is through the computation block and one register. The propagation delay of that path is 8 ns for $V_{dd} = 3.3$ V. The throughput should still be 100 Msamples/s. Fill in the internal clock period time and the lowest possible power supply voltages for the different cases in Table 3.

Table 3: Supply voltage reduction for interleaved implementations.

	64 D flip-flops	2 x 32 D flip-flops	4 x 16 D flip-flops	8 x 8 D flip-flops
Internal clock period				
Lowest supply voltage				

9. Redo the random data simulations with the lowest possible supply voltage from Table 3. Fill in the power consumption of the FIFO register (excluding the computational block) in Table 4.

Table 4: Random data with different supply voltage.

	64 D flip-flops	2 x 32 D flip-flops	4 x 16 D flip-flops	8 x 8 D flip-flops
Power consumption				

Comments and conclusions:

5.4 Final Design

A SPICE netlist of a FIFO with interleaving of factor 2, where multiplexers, demultiplexers, clock generation, and clock buffers are taken into account is found in the file `INT2X32Dffs.sp`. In `fifo_final_2x32.sp` this netlist is included together with the original clock signal which is used to generate the two internal clocks.

```
nanosim -n fifo_final_2x32.sp -nvec test1.vec -c cfg -t 4000
```

10. Simulate the power consumption. Compare with earlier simulations. Comments?

    ---

6 Appendix A

/coop/e/eks/course/TSTE85/lab2/file/Cells.sp

```
* Title : Some cells from a standard cell library

*****************************************************
** X1
*****************************************************
.SUBCKT INV1 IN OUT INH_VDD INH_GND
MN1 OUT IN INH_GND INH_GND  MODN  L=300E-9 W=1E-6 AD=+1.50000005E-12
+AS=+1.50000005E-12 PD=+4.00000011E-06 PS=+4.00000011E-06 NRD=+8.00000009E-01
+NRS=+8.00000009E-01 M=1.0
MP1 OUT IN INH_VDD INH_VDD  MODP  L=300E-9 W=2E-6 AD=+3.00000011E-12
+AS=+3.00000011E-12 PD=+5.00000011E-06 PS=+5.00000011E-06 NRD=+4.00000005E-01
+NRS=+4.00000005E-01 M=1.0
.ENDS INV1

*****************************************************
** CLINVR
*****************************************************
.SUBCKT CLINVR CLK XCLK IN OUT INH_VDD INH_GND
MN2 OUT CLK NET18 INH_GND  MODN  L=300E-9 W=1E-6 AD=+1.50000005E-12
+AS=+1.50000005E-12 PD=+4.00000011E-06 PS=+4.00000011E-06 NRD=+8.00000009E-01
+NRS=+8.00000009E-01 M=1.0
MN1 NET18 IN INH_GND INH_GND  MODN  L=300E-9 W=1E-6 AD=+1.50000005E-12
+AS=+1.50000005E-12 PD=+4.00000011E-06 PS=+4.00000011E-06 NRD=+8.00000009E-01
+NRS=+8.00000009E-01 M=1.0
MP1 NET10 IN INH_VDD INH_VDD  MODP  L=300E-9 W=2E-6 AD=+3.00000011E-12
+AS=+3.00000011E-12 PD=+5.00000011E-06 PS=+5.00000011E-06 NRD=+4.00000005E-01
+NRS=+4.00000005E-01 M=1.0
MP2 OUT XCLK NET10 INH_VDD  MODP  L=300E-9 W=2E-6 AD=+3.00000011E-12
+AS=+3.00000011E-12 PD=+5.00000011E-06 PS=+5.00000011E-06 NRD=+4.00000005E-01
+NRS=+4.00000005E-01 M=1.0
.ENDS CLINVR

*****************************************************
** INVR_DFA
*****************************************************
.SUBCKT INVR_DFA  IN OUT INH_VDD INH_GND
MN1 OUT IN INH_GND INH_GND  MODN  L=300E-9 W=1E-6 AD=+1.50000005E-12
+AS=+1.50000005E-12 PD=+4.00000011E-06 PS=+4.00000011E-06 NRD=+8.00000009E-01
+NRS=+8.00000009E-01 M=1.0
MP1 OUT IN INH_VDD INH_VDD  MODP  L=300E-9 W=1.5E-6 AD=+2.25000008E-12
+AS=+2.25000008E-12 PD=+4.50000011E-06 PS=+4.50000011E-06 NRD=+5.33333340E-01
+NRS=+5.33333340E-01 M=1.0
.ENDS INVR_DFA

*****************************************************
** DFF
*****************************************************
.SUBCKT DFF CLK D Q VDD VGND
XIN_4  NET22 NET11 VDD VGND INVR_DFA
XIN_3  NET26 NET25 VDD VGND INVR_DFA
XIN_5  NET11 Q VDD VGND INV1
XIN_6  NET22 QN VDD VGND  INV1
XIN_2  CN CI VDD VGND INV1
```

```
XIN_1  CLK CN VDD VGND INV1
XCIN_3 CI CN  NET26 NET22 VDD VGND CLINVR
XCIN_2 CI CN  NET25 NET26 VDD VGND CLINVR
XCIN_4 CN CI  NET11 NET22 VDD VGND CLINVR
XCIN_1 CN CI  D NET26 VDD VGND CLINVR
.ENDS DFF

.end
```

7 Appendix B

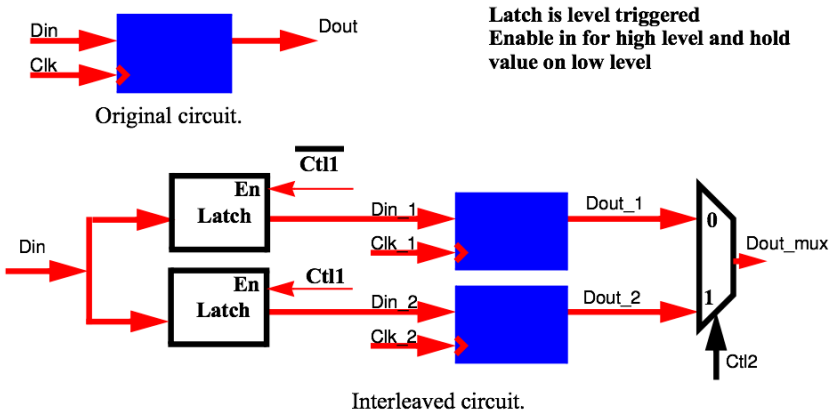
/coop/e/eks/course/TSTE85/lab2/file/My_Cells.sp

```
* Title: My_Cells (Template)

* DFF_8 consists of one  chain of  8 D flip-flops
* DFF_8x8  consists of 8 parallel chains of  8 D flip-flops
* DFF_4x16 consists of 4 parallel chains of 16 D flip-flops
* DFF_2x32 consists of 2 parallel chains of 32 D flip-flops
* DFF_64 consists of one chain of 64 D flip-flops


************************************************************
* Include Cells.cp
************************************************************
.include '/coop/e/eks/course/TSTE85/lab2/files/Cells.sp'


************************************************************
**                Sub circuits                            **
************************************************************


************************************************************
* Sub Circuit  DFF_8
************************************************************

.subckt DFF_8 CLK Din Dout VDD VGND

* Modify this cell (Substitute all "?")

X_DFF0 CLK Din  Q0     VDD VGND DFF
X_DFF1 CLK Q0   Q1     VDD VGND DFF
X_DFF2 CLK ?    ?   VDD VGND DFF
X_DFF3 CLK ?    ?   VDD VGND DFF
X_DFF4 CLK ?    ?   VDD VGND DFF
X_DFF5 CLK ?    ?       VDD VGND DFF
X_DFF6 CLK ?    ?   VDD VGND DFF
X_DFF7 CLK ?    Dout  VDD VGND DFF

.ends DFF_8


************************************************************
* Sub Circuit  DFF_8x8
************************************************************

.subckt DFF_8x8 CLK Din0 Din1 Din2 Din3 Din4 Din5 Din6 Din7
+ Dout0 Dout1 Dout2 Dout3 Dout4 Dout5 Dout6 Dout7 VDD VGND

X_DFF_8_0 CLK ?   ? ?   ?    DFF_8
X_DFF_8_1 CLK ?   ? ?   ?    ?

* ...
* Fill in your netlist for DFF_8x8 here
* ...
```

```
X_DFF_8_7 CLK ?   ? VDD VGND ?

.ends DFF_8x8


************************************************************
* Sub Circuit  DFF_16x4
************************************************************

.subckt DFF_16x4 CLK Din0 Din1 Din2 Din3 Dout0 Dout1 Dout2 Dout3 VDD VGND

* Fill in your netlist for DFF_16x4 here

.ends DFF_16x4


************************************************************
* Sub Circuit  DFF_32x2
************************************************************

.subckt DFF_32x2 CLK Din0 Din1 Dout0 Dout1 VDD VGND

* Fill in your netlist for DFF_32x2 here

.ends DFF_32x2


************************************************************
* Sub Circuit  DFF_64
************************************************************

.subckt DFF_64 CLK Din Dout VDD VGND

* Fill in your netlist for DFF_64 here

.ends DFF_64
```

Preparatory exercise: Interleaving

We interleave a circuit `A` with a factor of 2. `A_1` and `A_2` are identical to `A`. Determine the signals: `Din_1`, `Din_2`, `Dout_1`, `Dout_2`, `Clk_1`, `Clk_2`, `Ctl1`, and `Ctl2`. **Sketch the waveforms!**



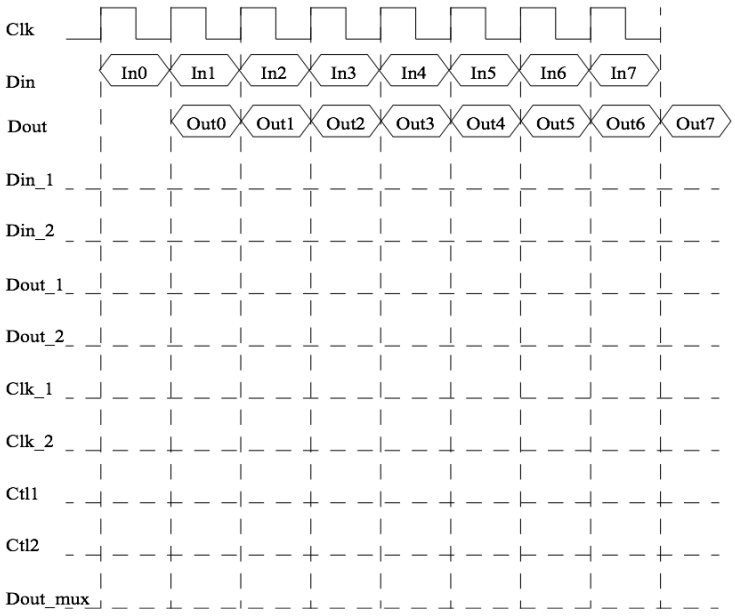


Figure 6: Preparatory exercise: Interleaving.

The page must be handed in to the laboratory assistant.
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