Lectures

1. Introduction
2. System level
3. Algorithm level
4. Architecture level
5. Register transfer level
6. Logic level
7. Circuit level
8. Synchronization
9. Low power components
10. Analog circuits (Guest lecturer: J Jacob Wikner)
11. Radio circuits (Guest lecturer: Ted Johansson)
12. Special techniques

Outline today’s lecture

- Analog CMOS low power
- Power efficiency
- Techniques to meet analog low power
- Experimental results

Today's paper

Extract from book:

"Designing Low Power Digital Systems, Emerging Technologies (1996)"

CMOS Low-Power Analog Circuit Design

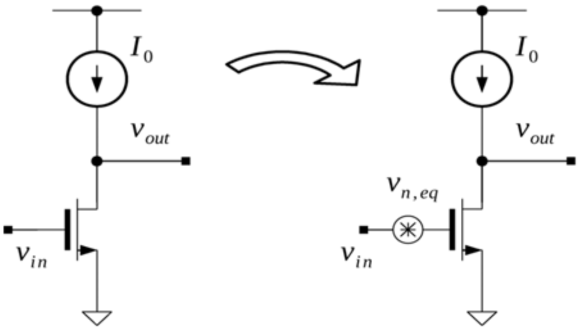
by Enz and Vittoz, Switzerland

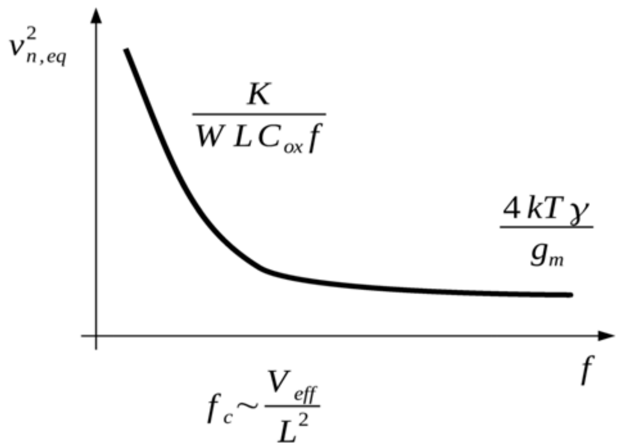
Book is from 1996, but theory uses fundamental limits, and also touches upon "modern" processes. The book, and especially the research group, is well-cited.

Introduction

- There are some different questions arising:
  - How much current do we need to operate an analog circuit?
  - How much voltage do we need to operate an analog circuit?
- A common figure of merit is:
  power required to realize a single pole given a certain gain
  - Applicable to for example comparators too

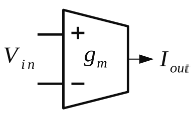
Noise in a CMOS transistor

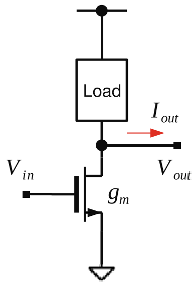


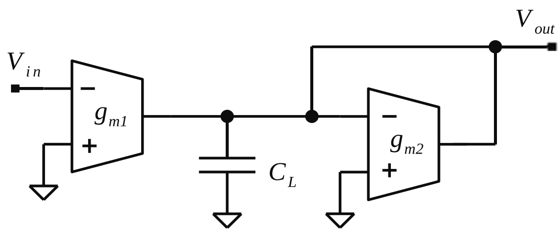


Simple filter

- Single-pole realization

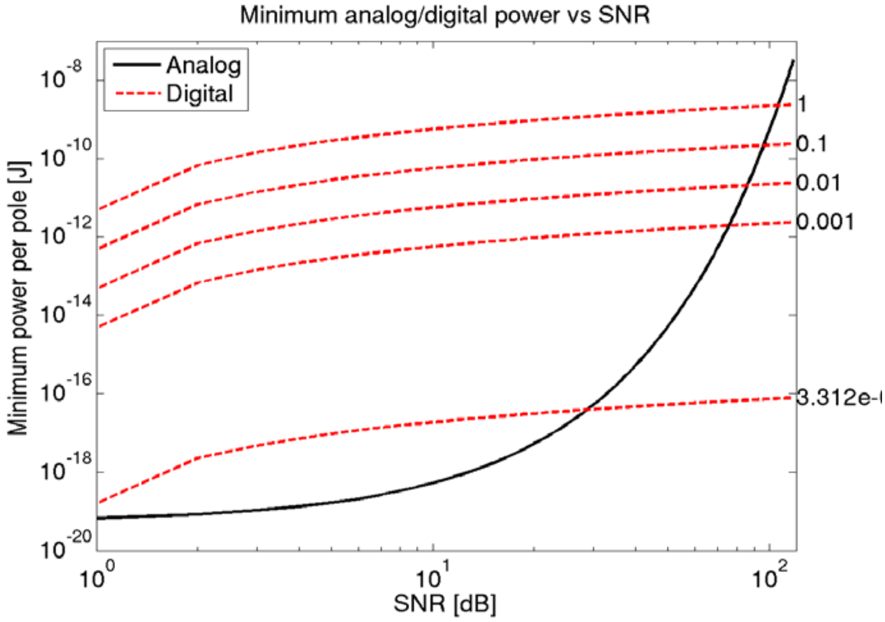






[Sve'10] **Fig. 10** **Fig. 12** **Fig. 11**

Min power for analog and digital circuits



Practical power limits

- Technology dependent limitations
  - Capacitors increase *P*
  - *P* in bias circuit is “wasted”
  - Signal $V_{pp} < V_{dd}$ increases *P*
  - Additional noise sources increase *P*
  - Low transconductance-to-current ratio g_m/I increases *P* for *C* loads
  - Precision devices are large, increasing parasitic *C* and *P*
  - The clock in switched capacitor circuits may be dominant
- Ways to reduce *P* is found at all levels of analog design

Historical and psychological obstacles

- Analog blocks are taken from existing libraries not compatible with low voltage and/or current
  - Less important today, technology scaling is so fast so it is difficult to maintain databases with pre-designed circuits.
- Use of very low bias currents are discarded due to inadequate transistor models
  - “New” models are constantly being developed, BSIM4 and EKV
- Fear of breaking the microampere barrier
  - “Microampere is too small to make sense”
- Requirements on power supply and ground rejection are exaggerated and mistaken for insensitivity to general noise
  - E.g. a differential circuit is less sensitive than a single-ended

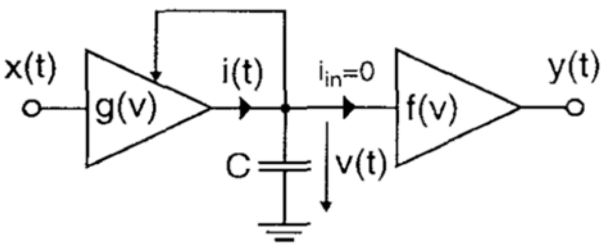
Power efficient analog circuits

- Voltage is not critically related to power
  - Use sleep modes
  - Use voltage multipliers when the supply voltage is very low
    - charge pump, boosting…
- High-frequency requires much power
  - Select architecture with few devices operating
  - Amplify signals early in the signal chain
  - Use subsampling if possible
- And ... go to digital domain A.S.A.P!

Special techniques

- Companding
- Analog floating point
- Divide and conquer

Instantaneous companding



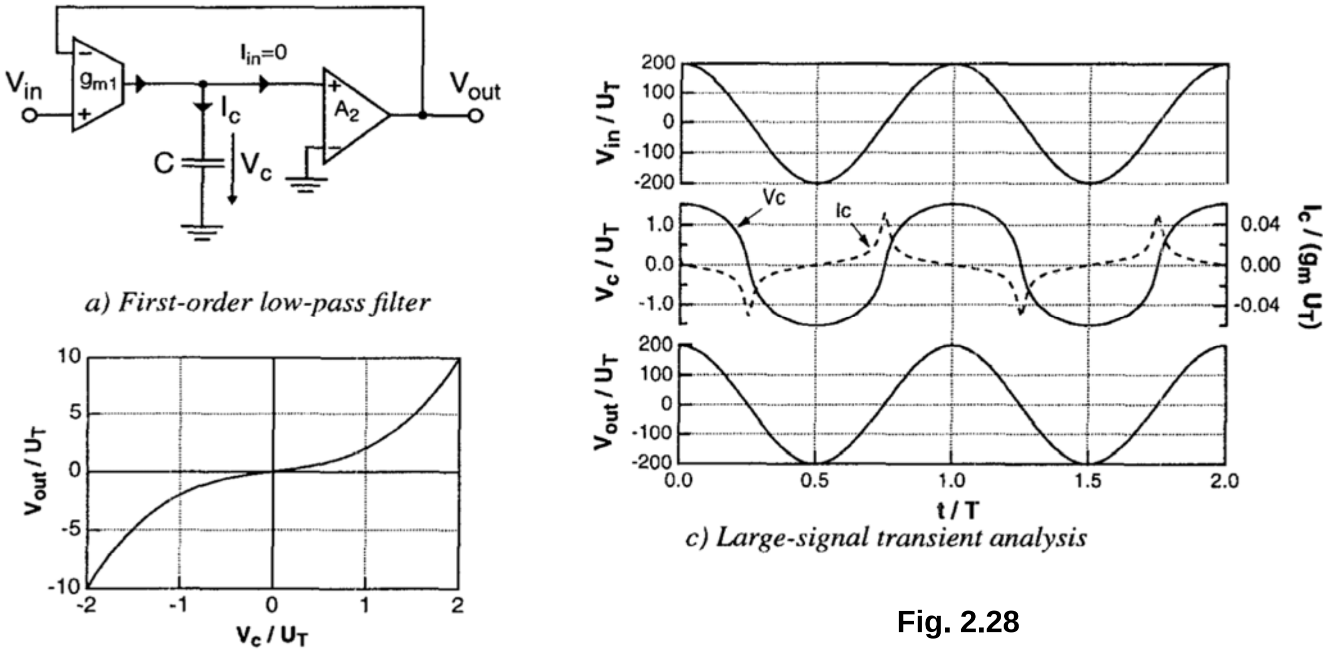
expanding function: $y = f(v)$

companding function: $i = g(v) \cdot x$

linear capacitor: $i = C \cdot \dfrac{dv}{dt}$

Figure 2.27 Basic integrator illustrating the principle of instantaneous companding

Cubic expansion example



a) First-order low-pass filter

b) Expansion characteristic

c) Large-signal transient analysis

Fig. 2.28

Log-domain filter design

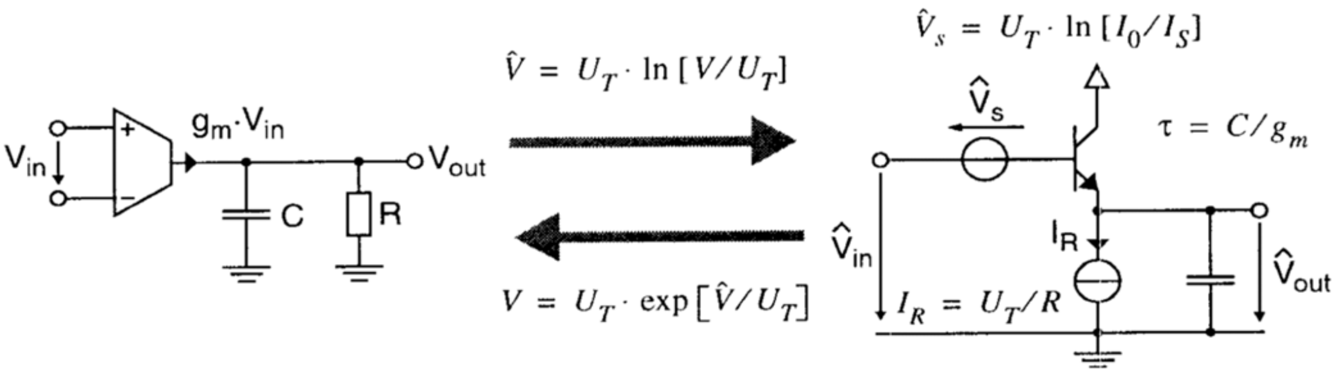


Figure 2.30 Mapping between linear- and log-domain [53][63][64]

References

12.pdf **CMOS low-power analog circuit design**

C.C. Enz and E.A. Vittoz

Designing Low Power Digital Systems, Emerging Technologies, 1996, pages 79-86 and 116-133

[Sve10] **Power consumption of analog circuits: a tutorial**

C. Svensson and J.J. Wikner

Analog Integrated Circuits and Signal Processing, volume 65, issue 2, Springer, 2010, pages 524-543