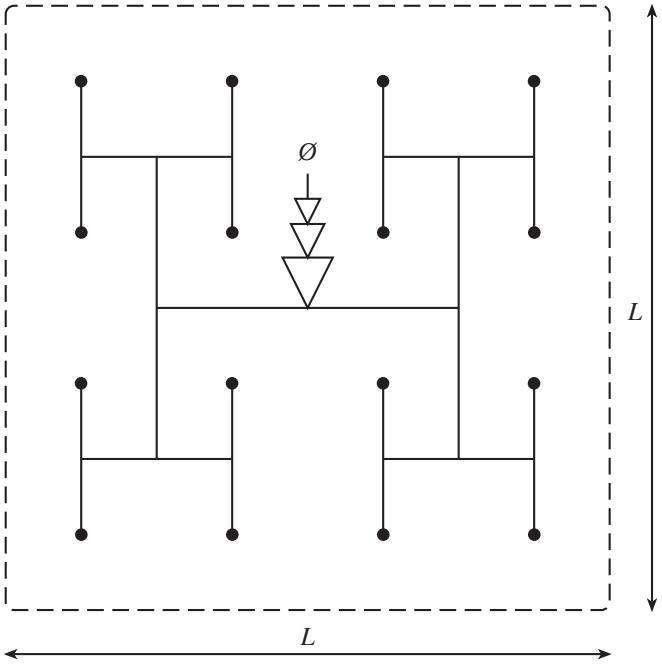
Clock tree design

- H tree with N = 16 nodes
- Asymptotic wire length

$$l = 1.5L\sqrt{N}$$



RC model of an H tree

- Shorten symmetrical tree branches to estimate Elmore delay

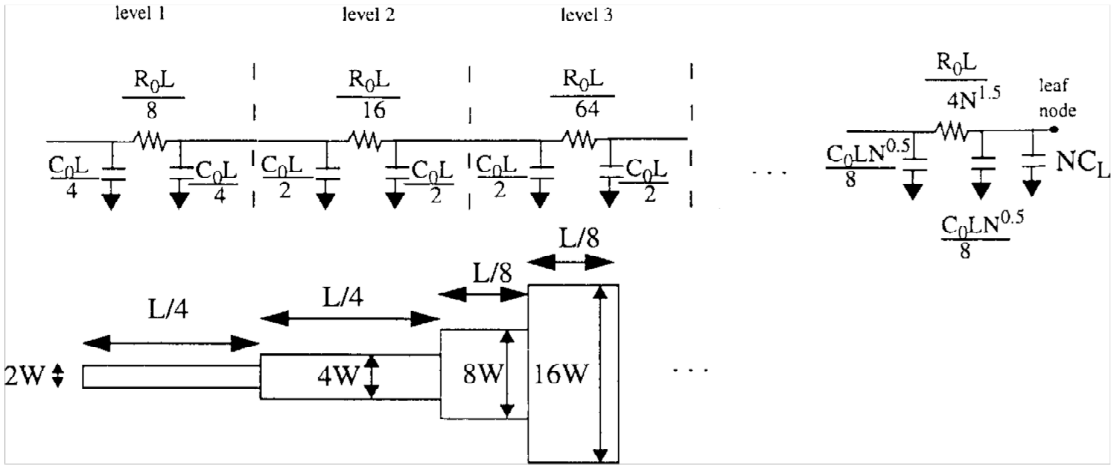


Fig. 4. RC line equivalent of the H tree

Intentional skew insertion

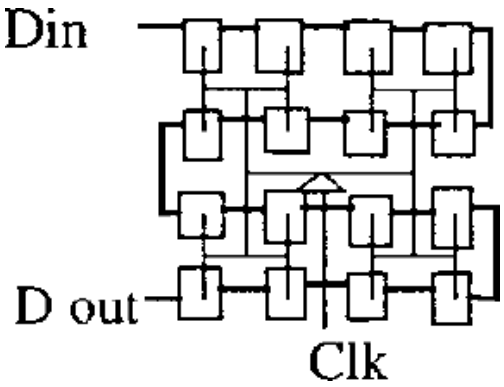


Fig. 15. H tree wire clock layout

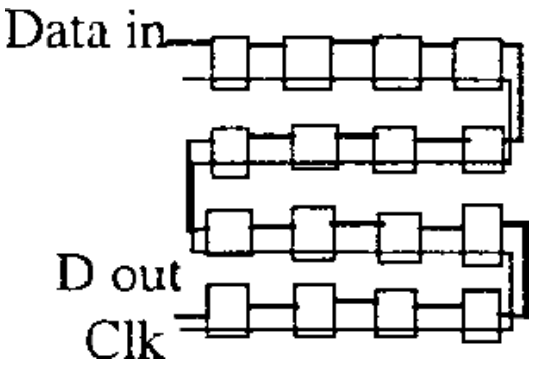


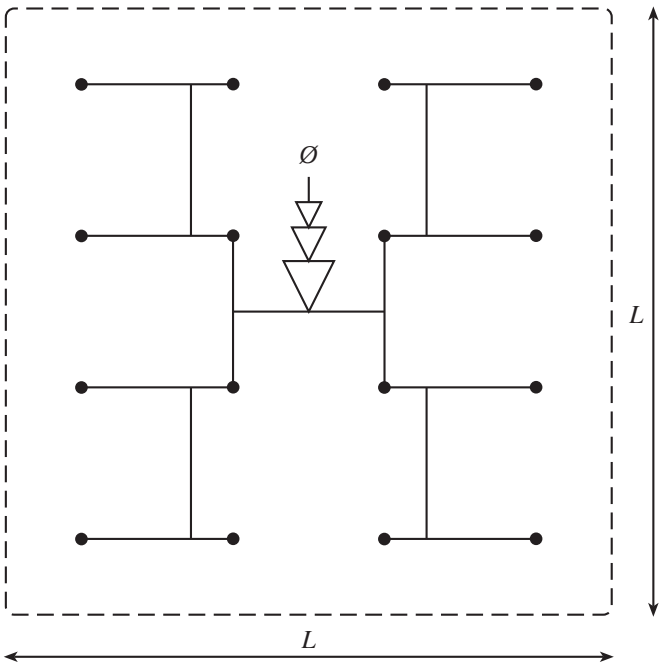
Fig. 16. P optimum clock layout

Low power tree

- Steiner tree
- Asymptotic wire length

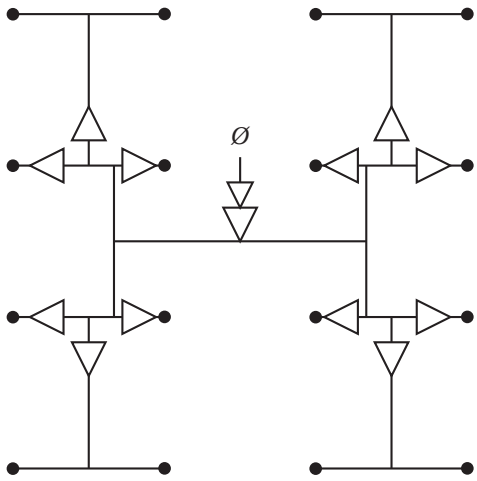
$$l = L\sqrt{N}$$

- However clock is skewed



Adjust skew

- Use buffers as variable delay elements
  - Adjust to zero skew



Results from buffer insertion

TABLE III
0.5 μm CMOS RESULTS

Benchmark	Power (mW)		Buffer area		# buffers	
	GRIN	ROOT	GRIN	ROOT	GRIN	ROOT
R1	8.8	19	5	32	3	4
R2	18	24	13	32	4	4
R3	21	50	13	86	4	5
R4	37	63	15	86	6	5
R5	54	139	17	235	8	6

Considerations

- Clock gating can be assigned to a subtree
- Use of unit-sized buffers placed in the same orientation minimizes variations in buffer characteristics
- The buffers may be used to solve rise and fall time constraints
  - Clock period needs to be at least three times the rise time

Ultra LP sensor systems

- Major requirements
  - Power management
    - Trade-off *P* vs. processing capability
    - Multiple power domains
    - Control of leakage currents
  - Energy harvesting
- Sub-V_T logic will likely play a key role in *E* efficient designs, but
  - Current drive variations increase by 10x
    - Gate delay varies 300% of nominal
  - 10-100x loss in throughput needs to be addressed
    - Parallelism
    - Architectural changes
    - Multivoltage operation

Asynchronous design

- Benefits
  - Power management with low latency
  - Simple *V* and *f* scaling
  - Low EMI and crosstalk
  - Robust operation across PVT variations
    - Easier to handle variations in sub-V_T designs
- Drawbacks
  - Complicated design approach
  - Lack of CAD support
  - Area/performance penalty

Bundled data

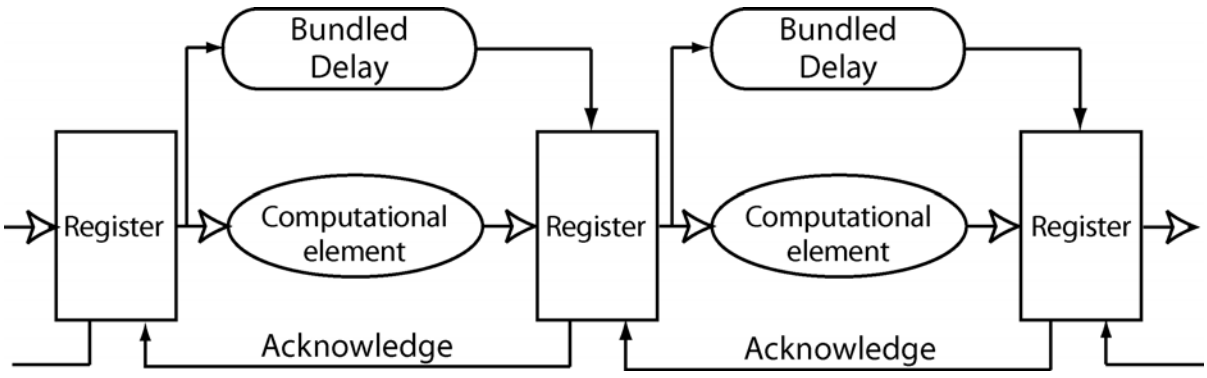


Fig. 2 Bundled data design

Timing in synchronous/asynchronous

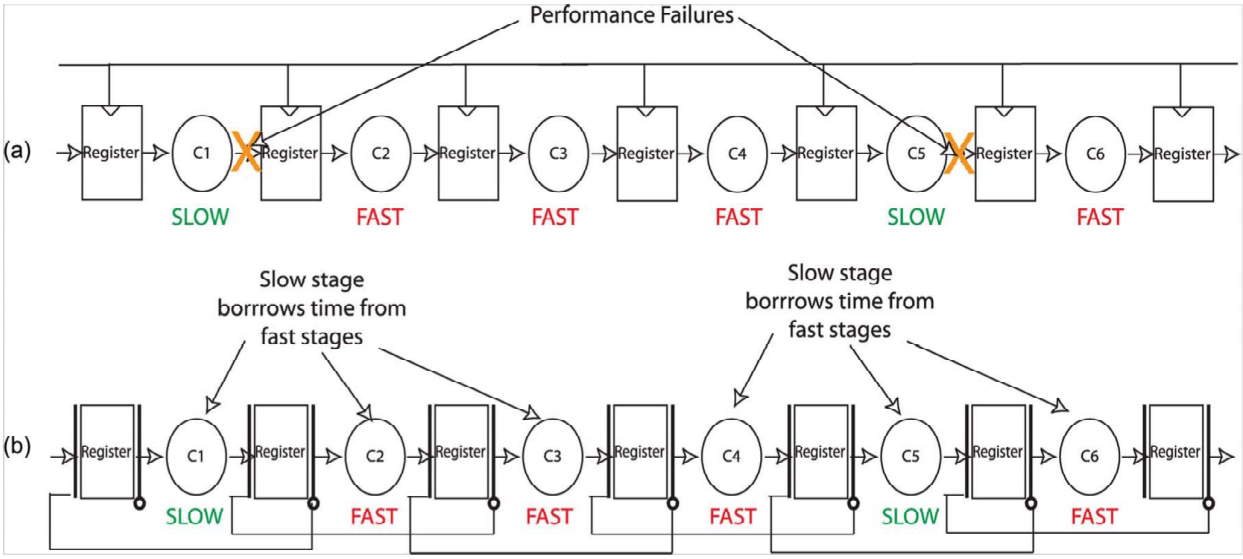
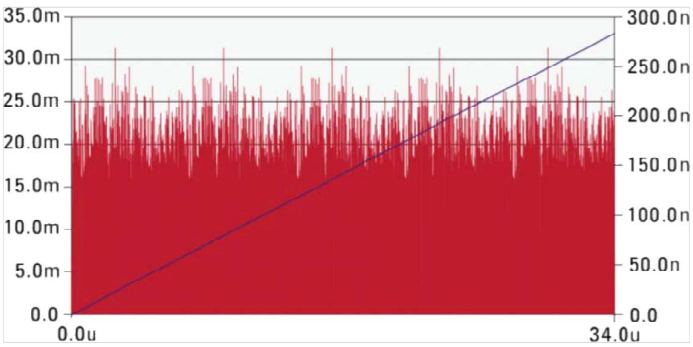


Fig. 5 Slow stages in (a) synchronous logic, (b) asynchronous logic

I and *E* of ARM9

Synchronous



Asynchronous

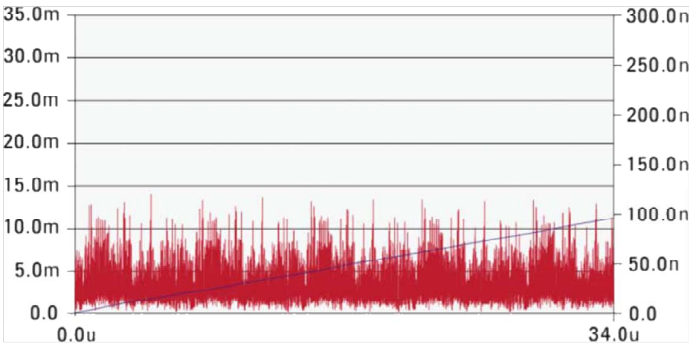
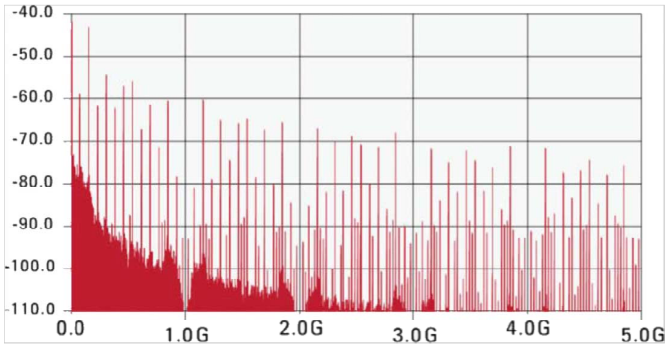


Fig. 3 *I* and *E*

Electromagnetic emission of ARM9

Synchronous



Asynchronous

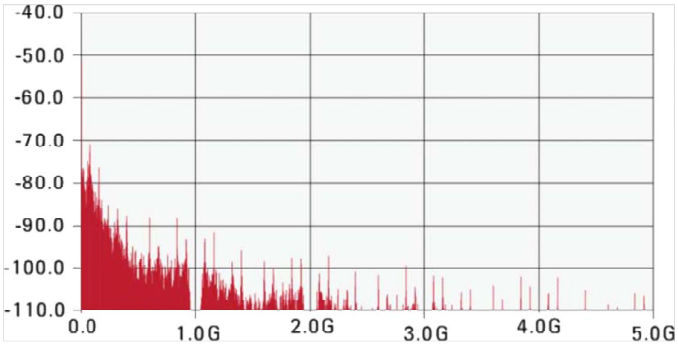


Fig. 3 EMI

Null convention logic (NCL)

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

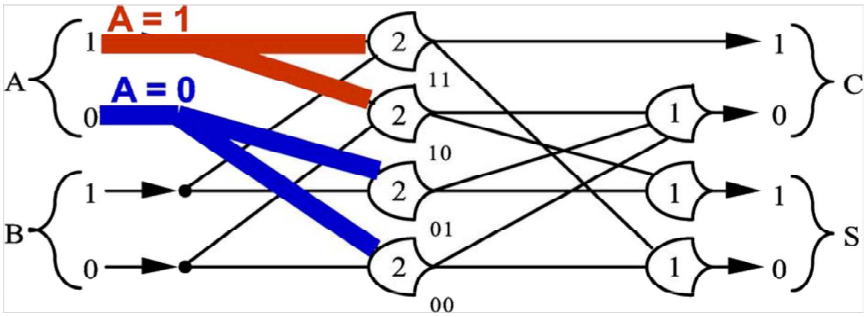


Fig. 4 NCL half adder

NCL uses dual-rail encoding of the signals

Microcontroller designs

Design	Area (mm2)		# of Cell Types	Total Cells	Total Transistors	Energy (mW/ MHz)	Processor Speed
	Cells	Routed					
NCL8051	249,679	295,935	162	5,698	58,753	47	36.5 MHz (effective)
DW8051A	153,867	179,772	72	3,410	51,482	157.4	36.5 MHz (actual)
DW8051B	145,699	169,740	123	3,305	48,482	182.4	36.5 MHz (actual)

(Energy and performance results were simulated with PowerMill™)

Table 1 Comparison of NCL and two conventional microcontrollers

Subthreshold operation

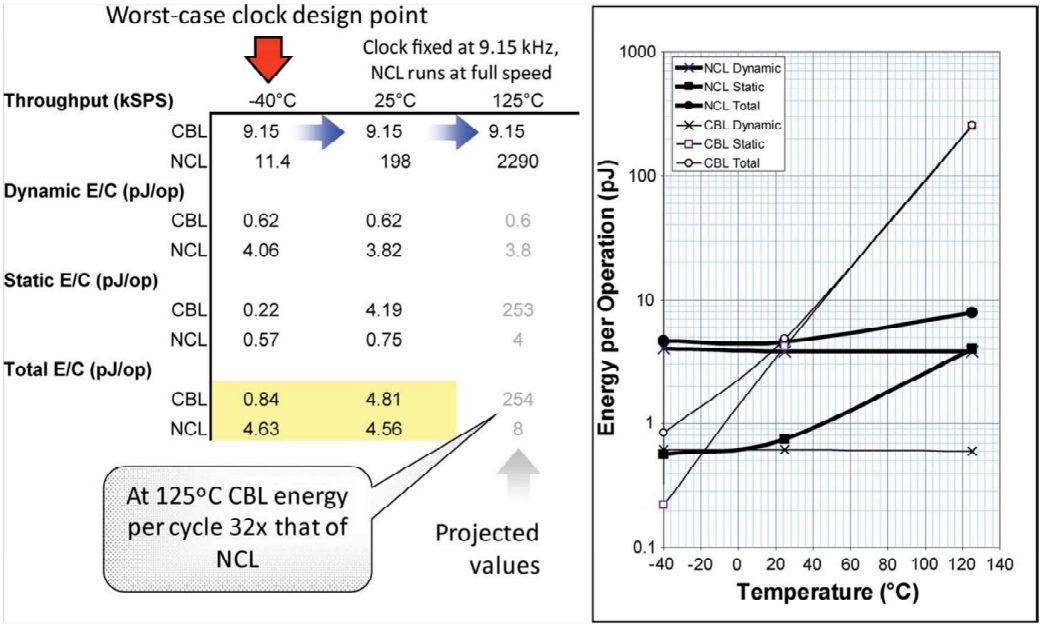


Fig. 10 Comparison of conventional and NCL 5-tap FIR filter

References

08.pdf **Low-power buffered clock tree design**

A. Vittal and M. Marek-Sadowska

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, volume 16, issue 9, Sept. 1997, pages 965-975

09.pdf **Ultralow-power operation in subthreshold regimes applying clockless logic**

R.D. Jorgenson, L. Sorensen, D. Leet, M.S. Hagedorn, D.R. Lamb, T.H. Friddell, and W.P. Snapp

Proceedings of the IEEE, volume 98, issue 2, Feb. 2010, pages 299-314