# Transition probabilities for different topologies

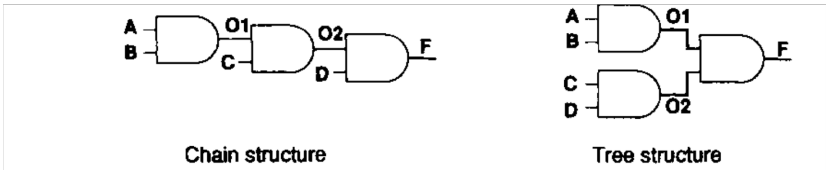


**Fig. 4.** Simple example to demonstrate the influence of circuit topology on activity.

**Table 1** Probabilities for Tree and Chain Topologies

| | O1 | O2 | F |
|---|---|---|---|
| $P_1$ (chain) | 1/4 | 1/8 | 1/16 |
| $P_0 = 1 - P_1$ (chain) | 3/4 | 7/8 | 15/16 |
| $\alpha_{01} = P_0P_1$ (chain) | 3/16 | **7/64** | 15/256 |
| $P_1$ (tree) | 1/4 | 1/4 | 1/16 |
| $P_0 = 1 - P_1$ (tree) | 3/4 | 3/4 | 15/16 |
| $\alpha_{01} = P_0P_1$ (tree) | 3/16 | **3/16** | 15/256 |



# Glitching in a ripple-carry adder

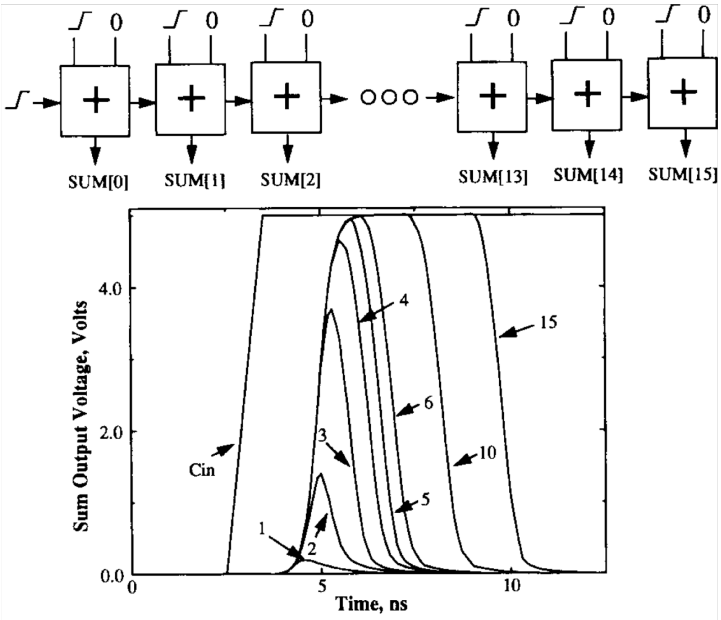


**Fig. 6.** Waveforms for a 16-b adder demonstrating glitching behavior.

# Data correlation

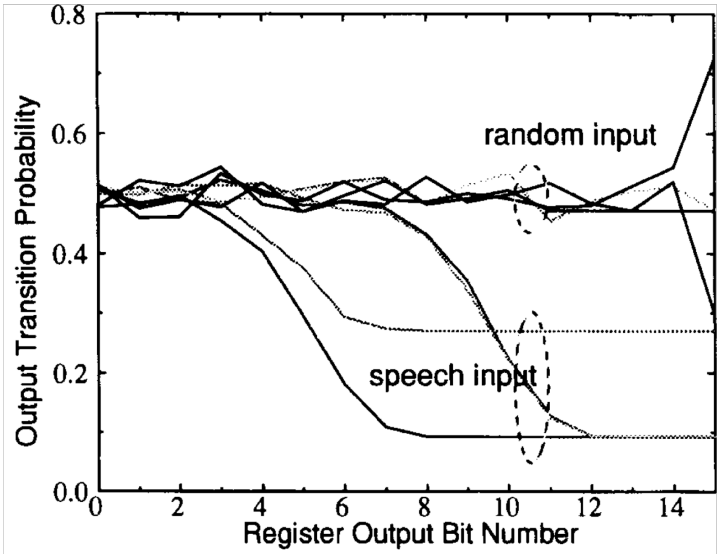


**Fig. 1.** Dependence of activity on statistics: Correlated versus random input.



# Transition activity of different bits

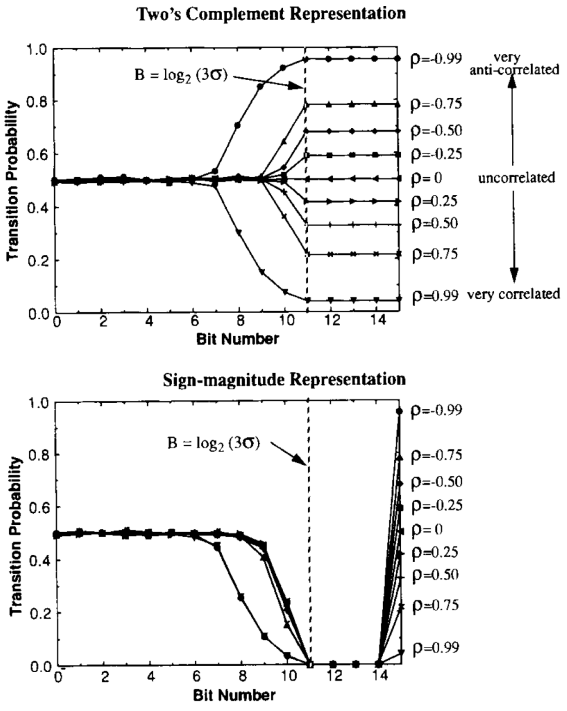


**Fig. 23.** Transition activity for different number representations.

# Arithmetic computation

**Table 3** Number Representation Tradeoff for Arithmetic

| Input Pattern (1024 cycles) | Two's Complement Power, 3V | Sign Magnitude Power, 3V |
|---|---|---|
| Constant (IN=7) | 1.97 mW | 2.25 mW |
| Ramp (-7,-6,...7,-7) | 2.13 mW | 2.43 mW |
| Random | 3.42 mW | 2.51 mW |
| Min -> Max -> Min (-7, +7,-7,+7,...) | 5.28 mW | 2.46 mW |

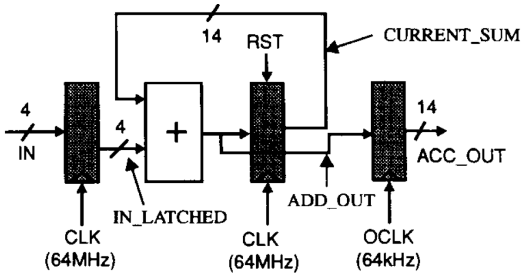


**Fig. 26.** Two's complement implementation of an accumulator.

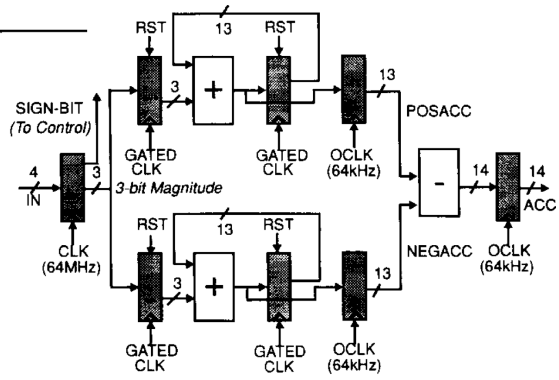


**Fig. 29.** Sign magnitude implementation of an accumulator.



# Bus sharing

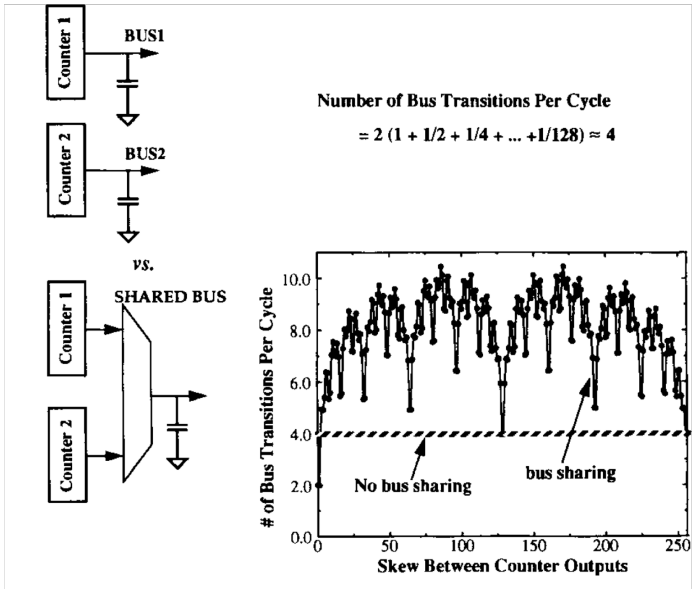


**Fig. 33.** Activity tradeoff for time-multiplexed hardware: Bus-sharing example.

# Sharing hardware

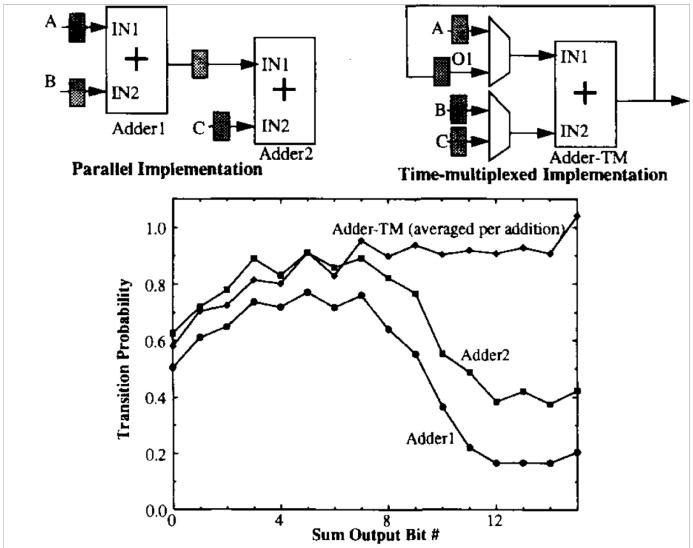


**Fig. 34.** Activity tradeoff for time-multiplexed hardware: Adder example.



# Reference

**03.pdf** **Minimizing power consumption in digital CMOS circuits**

*A.P. Chandrakasan and R.W. Brodersen*

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