SOLUTIONS TO EXAM IN TSEI03 DIGITAL CIRCUITS 2020-01-07

1 a) For a saturated MOSFET with $V_{DS} > V_{GS}-V_T$, the electrical field is not strong enough to create a channel close to the drain. This effect is called 'pinch-off', and it counteracts further increase in drain current for increasing V_{DS} due to an increasing region without channel.

b) A static CMOS inverter has lower V_{OL} than an NMOS inverter, yielding higher noise margins and a lower static power dissipation.

c) A *noise margin* is defined as the difference between the best output voltage and the worst input voltage that can be accepted. It measures the amount of noise that can be added to a node between two cascaded, identical gates without ruining the function.

d) Given a fixed thickness and material of a wire, the resistance is constant per square of the wire area.

2 a) V_D is given by the voltage drop over the resistor due to constant current

$V_D = V_{DD} - RI$

$V_D = V_{DD} - RI = 2.5 - 10 \cdot 10^3 \cdot 50 \cdot 10^{-6}\ \text{V} = \underline{2.0\ \text{V}}$

A small R causes a small voltage drop over R, and a large over the MOSFET. Try with saturated operating mode and solve for V_{GS}

$$I_D = \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 = 50\ \mu\text{A} \Rightarrow$$

$$V_{GS} = \sqrt{I_D \frac{2}{k'}\frac{L}{W}} + V_T = \sqrt{50 \cdot 10^{-6}\frac{2}{115 \cdot 10^{-6}}\frac{0.25}{2.0}} + 0.43\ \text{V} \approx 0.76\ \text{V}$$

Find V_S

$V_S = V_G - V_{GS} = \underline{1.24\ \text{V}}$

Check operation mode

$V_{\min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(0.76 - 0.43, 2.0 - 1.24, 0.63\right) = V_{GT}$

The MOSFET is <u>saturated</u>.

b) V_D is given by the voltage drop over the resistor due to constant current

$V_D = V_{DD} - RI = 2.5 - 30 \cdot 10^3 \cdot 50 \cdot 10^{-6}\ \text{V} = \underline{1.0\ \text{V}}$

A large R causes large voltage drop over R, and a small over MOSFET. Try with linear operating mode and solve for V_S

$$I_D = k'\frac{W}{L}V_{DS}\left(V_{GT} - \frac{V_{DS}}{2}\right) \Leftrightarrow V_S^2 - 2\left(V_G - V_T\right)V_S + 2\left(V_G - V_T\right)V_D - V_D^2 - \frac{2I_D L}{k'W} = 0 \Leftrightarrow$$

$$V_S = V_G - V_T \pm \sqrt{\left(V_G - V_T\right)^2 - 2\left(V_G - V_T\right)V_D + V_D^2 + \frac{2I_D L}{k'W}} \approx 1.57 \pm 0.66\ \text{V}$$

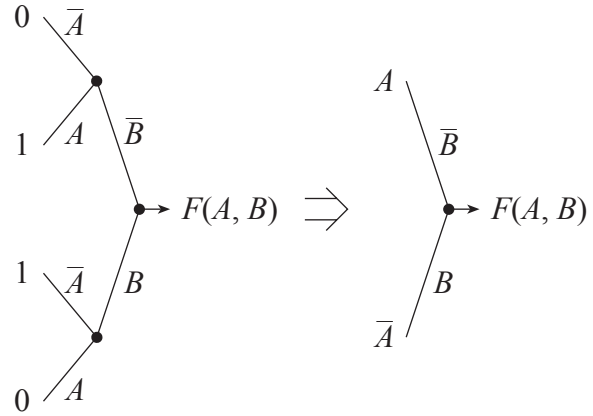
$V_S < V_D \Rightarrow V_S \approx \underline{0.91\ \text{V}}$

Check operation mode

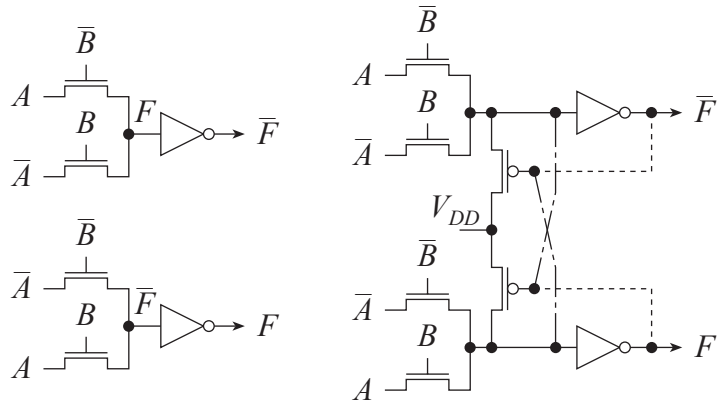
$V_{\min} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right) = \min\left(2.0 - 0.91 - 0.43, 1.0 - 0.91, 0.63\right) = V_{DS}$

The MOSFET is <u>linear</u>.

3 a) Realize e.g. as a binary tree and simplify



Replace the branches with NMOSFETs and add an inverter to the output. The complementary output can e.g. be realized by inverting the inputs to the tree like resulting in the circuit shown to the left below.

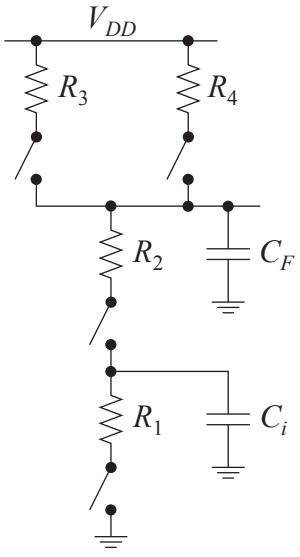


b) Add keepers to the nodes with reduced swing before the inverters as shown above to the right. The gates of the keepers can be connected in two ways:

i) to the inverter output as shown with the dashed line

ii) to the complementary net as shown with the dot-dashed line.

4 a) An *RC* switch model of a NAND gate is shown to the right.



b) As we can see from equivalent *RC* model, the case in which both inputs transition go low ($A = 1 \rightarrow 0$, $B = 1 \rightarrow 0$) results in a smaller delay because of two R_p in parallel makes the total resistance to be $R_p/2$.

c) The reason for the different delay involves the internal node capacitance of the pull-down net (i.e. in the connection M_1—M_2). For the case in which $A = 1$ and B transitions from $1 \rightarrow 0$, the pull-up PMOS device only has to charge up the output node capacitance (M_2 is turned off). On the other hand for the case in which $B = 1$ and A transits from $1 \rightarrow 0$, the pull-up PMOS device has to charge both the output and the internal node capacitances, which slows down the transition.

5 a) The static latch is shown in a) and the dynamic latch is shown in b).

b) First consider the static latch. When the clock is high the bottom transmission gate is on and the latch is transparent, copying the *D* input to the *Q* output. During this phase, the feedback loop is open since the top transmission gate is off. When the clock signal is low the bottom transmission gate is off and the top transmission gate is on and we have a positive feedback loop with two cross coupled inverters. The feedback holds the output stable during this phase.

Now consider the dynamic latch. When the clock is low the input data is sampled on the storage node with the capacitance *C*, mainly consisting of the gate capacitances of the transmission gate. When the clock is high the transmission gate is off and the charge stored on the capacitance will remain for a limited time during which the logic value is latched.

c) The signal must be kept stable a time before (*setup time*) and a time after (*hold time*) the clock edge that initiates the memory state.

6 a) Derive logic function $F = G'$ from the switch net function S_n of the precharged circuit

$$S_n = A(B+C) \Rightarrow G = \overline{S_n(A,B,C)} = \overline{A(B+C)} \Rightarrow F = \overline{G} = A(B+C)$$

b) The clocked PMOSFET is used to precharge *G* high, which will be the output value if the logic net does not conduct. The clocked NMOSFET is used to evaluate the logic function by connecting the logic net to ground. If the net conducts, *G* will be discharged to 0.

c) Charge sharing may occur according to the following example. If $F(A, B, C)$ is evaluated with $F(0, 1, 0)$, $F(0, 0, 1)$, or $F(0, 1, 1)$, capacitance C_x is discharged. Then if $F(1, 0, 0)$ is evaluated next, the voltage of node *G* should remain at V_{DD}, but is instead reduced due to sharing of C_G's charge with C_x. Depending on how much the output voltage is reduced, we may need to redesign the circuit to ensure proper operation.

d) Charge leakage can become a problem if the evaluation phase is long and the logic net is not conducting. Then the subthreshold leakage of the net discharges *G* partially, causing the inverter to consume a large static current and leaving less margin for noise.

e) Use same (minimum) *L* for all MOSFETs
The PMOSFET pull-ups consist of single transistors $\Rightarrow W_{P,inv} = 5$
The inverter NMOSFET consists of a single transistor $\Rightarrow W_{N,inv} = 3$
Design all NMOSFETs in a single path to have same width

$$R_{on} \propto \frac{L}{W} \Rightarrow \begin{cases} \frac{L}{W_{N,A}} + \frac{L}{W_{N,B}} + \frac{L}{W_{N,\emptyset}} = \frac{L}{3} \\ \frac{L}{W_{N,A}} + \frac{L}{W_{N,C}} + \frac{L}{W_{N,\emptyset}} = \frac{L}{3} \end{cases}$$

$$\Rightarrow \begin{cases} W_{N,A} = W_{N,B} = W_{N,\emptyset} = 9 \\ W_{N,A} = W_{N,C} = W_{N,\emptyset} = 9 \end{cases}$$

The circuit with aspect ratios indicated is shown in the schematic to the right.