# DIGITAL CIRCUITS

## Exam

TSEI03

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|---|---|
| Time: | Monday 21 October 2019, 14:00–18:00 |
| Place: | U4 |
| Teacher: | Mark Vesterbacka, phone 013-281324 |
| Allowed aid: | Calculator |
| Max score: | 60 points |
| Grades: | 45 points for 5<br>35 points for 4<br>25 points for 3 |
| Solutions: | Posted on the course web |
| Result: | Posted through LADOK by Wednesday 6 November 2019 |

1 a) What is the maximal value on the *gate capacitance* of a MOSFET? (2 p)

b) What is the *voltage transfer characteristic* (VTC) of a digital circuit? (2 p)

c) Explain how the *resistance of a conducting transmission gate* can be designed to be approximately constant. (2 p)

2 Given the data in Figure 1 for a short channel NMOS transistor with $V_{DSAT}$ = 0.58 V and $k'$ = 122 μA/V$^2$, calculate the parameters below.

a) $V_{T0}$ (3 p)

b) $\gamma$ (3 p)

c) $2|\phi_F|$ (3 p)

b) $W/L$ (3 p)

| Data set | $V_{GS}$ (V) | $V_{DS}$ (V) | $V_{BS}$ (V) | $I_D$ (μA) |
|---|---|---|---|---|
| 1 | 2.5 | 1.8 | 0 | 1812 |
| 2 | 2 | 1.8 | 0 | 1297 |
| 3 | 2 | 2.5 | 0 | 1361 |
| 4 | 2 | 1.8 | –1 | 1146 |
| 5 | 2 | 1.8 | –2 | 1039 |

Figure 1. Measured NMOS transistor data.

3 A metal wire have resistance $R_{wire}$ = 2 Ω, sheet resistance $R_{sq}$ = 0.07 Ω/square, width $W_{wire}$ = 3 μm, capacitance per area $C_{area}$ = 0.019 fF/μm$^2$, and capacitance per length $C_{edge}$ = 0.025 fF/μm.

a) Why is sheet resistance measured in Ω/square? (2 p)

b) Calculate the length of the wire. (4 p)

c) Calculate the total capacitance of the wire. (4 p)

4 The function $F = AB + \overline{CD}$ shall be implemented. Complements to the inputs are *not* available.

a) Implement the function with a static CMOS gate and static CMOS inverters. (5 p)

b) Size all transistors so that the worst-case output resistance of the gate and inverters is the same as that of an inverter with an NMOS $W/L$ = 3 and PMOS $W/L$ = 5. (5 p)

5 A precharged 2-input NAND gate shall be designed.

a) Draw the transistor schematic of the gate. (4 p)

b) Explain the operation of the gate. (4 p)

c) Explain how charge sharing may occur. (4 p)

6 A negative edge-triggered master-slave D flip-flop shall be designed.

a) Use inverters and transmission gates to design a D flip-flop that transfers the logical value at the input *D* to the output *Q* when the clock falls from high to low. (5 p)

b) Sketch a timing diagram that illustrates the transfer of both a low and a high logical value from *D* to *Q*. Include the clock, input, and output nodes, as well as the intermediate node between the two latches. Define the *setup time*, *hold time* and *clock-to-output delays* (high-to-low and low-to-high). What can happen if the setup time or hold time is violated? (5 p)

## Equations for the MOS transistor


**Definition of source (*S*) and drain (*D*)**

NMOS: $V_S \le V_D$ PMOS: $V_S \ge V_D$

**Voltage notations**

$$V_{GS} = V_G - V_S,\ V_{DS} = V_D - V_S,\ V_{SB} = V_S - V_B,\ V_{GT} = V_{GS} - V_T$$

**Threshold voltage**

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\Phi_F|} - \sqrt{2|\Phi_F|}\right)$$

**Unified model**

NMOS: $V_{GT} \le 0$ (PMOS: $V_{GT} \ge 0$) $\Rightarrow$ Subthreshold region ($I_D \approx 0$)

NMOS: $V_{GT} \ge 0$ (PMOS: $V_{GT} \le 0$) $\Rightarrow I_D = k'\frac{W}{L}V_{min}\left(|V_{GT}| - \frac{V_{min}}{2}\right)(1 + \lambda V_{DS})$

$V_{min} = min(|V_{GT}|, |V_{DS}|, |V_{DSAT}|)$

$V_{min} = |V_{GT}|$ $\Rightarrow$ saturation region

$V_{min} = |V_{DS}|$ $\Rightarrow$ resistive (linear, triode) region ($\lambda = 0$)

$V_{min} = |V_{DSAT}|$ $\Rightarrow$ velocity saturation region

***$V_{DSAT}$* dependency on channel length**

$$V_{DSAT} = L\xi_c$$

**Subthreshold region**

NMOS: $V_{GT} \le 0 \Rightarrow I_{Dn} = I_{0n}\frac{W}{L}e^{\frac{q(V_{GSn} - V_{Tn})}{nkT}}\left(1 - e^{-\frac{qV_{DSn}}{kT}}\right)(1 + \lambda_n V_{DSn})$

PMOS: $V_{GT} \ge 0 \Rightarrow I_{Dp} = I_{0p}\frac{W}{L}e^{\frac{q(V_{SGp} - |V_{Tp}|)}{nkT}}\left(1 - e^{-\frac{qV_{SDp}}{kT}}\right)(1 + \lambda_p V_{DSp})$

## Model parameters for 0.25 μm CMOS devices

**Parameters for drain current calculations**

| | $V_{T0}$ [V] | $\gamma$ [$\sqrt{\text{V}}$] | $V_{DSAT}$ [V] | $k'$ [μA/V$^2$] | $\lambda$ | $\Phi_F$ [V] |
|---|---|---|---|---|---|---|
| NMOS | 0.43 | 0.40 | 0.63 | 115 | 0.06 | –0.30 |
| PMOS | –0.40 | –0.40 | –1.00 | –30 | –0.10 | 0.30 |

**Parameters for capacitance calculations**

| | $C_{ox}$ [fF/μm$^2$] | $C_O$ [fF/μm] | $C_j$ [fF/μm$^2$] | $m_j$ | $\phi_b$ [V] | $C_{jsw}$ [fF/μm] | $m_{jsw}$ | $\phi_{bsw}$ [V] |
|---|---|---|---|---|---|---|---|---|
| NMOS | 6 | 0.31 | 2.0 | 0.50 | 0.9 | 0.28 | 0.44 | 0.9 |
| PMOS | 6 | 0.27 | 1.9 | 0.48 | 0.9 | 0.22 | 0.32 | 0.9 |

## Gate capacitance

**Overlap capacitance**

$$C_{GSO} = C_{GDO} = C_{ox}x_d W = C_O W$$

**Channel capacitance**

$$C_{GC} = C_{GCB} + C_{GCS} + C_{GCD}$$

| Condition | $C_{GCB}$ | $C_{GCS}$ | $C_{GCD}$ |
|---|---|---|---|
| $V_{GTn} \le 0,\ V_{GTp} \ge 0$ | $C_{ox}WL$ | 0 | 0 |
| $V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{DS}\| \le \|V_{GT}\|$ | 0 | $C_{ox}WL/2$ | $C_{ox}WL/2$ |
| $V_{GTn} > 0,\ V_{GTp} < 0,\ \|V_{GT}\| \le \|V_{DS}\|$ | 0 | $2C_{ox}WL/3$ | 0 |

## Junction capacitance

**Junction capacitance as function of voltage**

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi_0)^m}$$

**Average capacitance during transition from $V_1$ to $V_2$**

$$C_{eq} = K_{eq} C_{j0} = \frac{-\phi_0^m}{(V_2 - V_1)(1-m)}[(\phi_0 - V_2)^{(1-m)} - (\phi_0 - V_1)^{(1-m)}]C_{j0}$$

## Dynamic power consumption

$$P = afC_{tot}V_{dd}^2$$

## Switch functions

$$S_N = \overline{F(A, B, \ldots)},\ S_P = F(\bar{A}, \bar{B}, \ldots)$$

## Boolean algebra

**De Morgans' theorem**

$$\overline{X + Y + Z + \ldots} = \bar{X}\bar{Y}\bar{Z}\ldots, \qquad \overline{XYZ\ldots} = \bar{X} + \bar{Y} + \bar{Z} + \ldots$$

**Expansion in sum**

$$f(X, Y, Z, \ldots) = Xf(1, Y, Z, \ldots) + \bar{X}f(0, Y, Z, \ldots)$$

**Expansion in product**

$$f(X, Y, Z, \ldots) = [X + f(0, Y, Z, \ldots)][\bar{X} + f(1, Y, Z, \ldots)]$$

## Transmission line

**Characteristic impedance**

$$Z_0 = \sqrt{l/c}$$

**Velocity of wave**

$$\upsilon = 1/\sqrt{lc}$$

**Reflection coefficient for a transmission line ($Z_0$) terminated by a load ($Z_L$)**

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0)$$

## Elmore delay

$P_i$ = "the path between node $0$ and $i$".

$P_{ij} = P_i \cap P_j$ = "the common part of the paths $P_i$ and $P_j$".

$R_{ij}$ = "the sum of all resistances in $P_{ij}$".

Time constant from node $0$ to $i$: $\tau_{di} = \sum_{j=0}^{n} R_{ij}C_j$. Propagation delay: $t_{pi} \approx 0.69\tau_{di}$.

## Sizing of cascaded inverters

For minimal propagation delay find the best solution to $1 = e^{(1+\gamma/k)}/k$, where $k$ = "tapering factor", $N$ = "number of inverters", $F = C_L/C_{g1} = k^N$ and $\gamma = C_{int1}/C_{g1}$.